MICRO NETWORKS

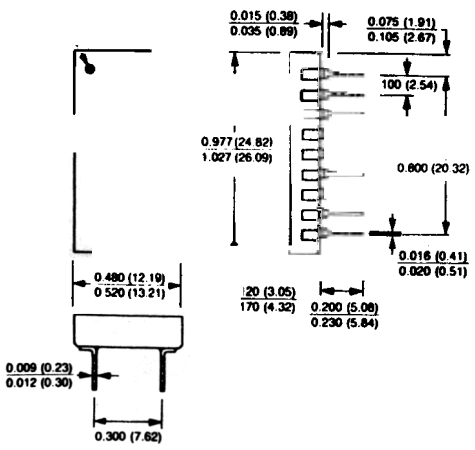
MN2020

DIGITALLY CONTROLLED PROGRAMMABLE-GAIN AMPLIFIER

FEATURES

- **Programmable Gain 1 to 128 in 8 Steps**
- **Gain Selected with a 3-Bit TTL Word**
- **Excellent Gain Accuracy: ±0.002% @ G=1 ±0.1% @ G=128**
- **Low Offset Voltage Drift ±5μV/°C**
- **High Input Impedance 1000 MΩ**
- **Small 18-Pin DIP**
- **Full Mil Operation −55°C to +125°C**
- **MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility**

18 PIN DIP



Dimensions in Inches (millimeters)

DESCRIPTION

MN2020 is a precision hybrid amplifier whose gain can be set to any one of 8 levels (1 to 128) with the application of a single 3-bit digital word (TTL logic levels) to its gain control inputs. This programmable-gain amplifier may be operated under direct computer or microprocessor control to provide fully automated, gain-range data acquisition.

The use of internal, laser-trimmed thin-film resistors result in excellent gain accuracy, linearity and drift characteristics. In addition, MN2020 has 100kHz of full power bandwidth and 5MHz of small signal bandwidth resulting in a rapid settling time of 5μsec for a 20 volt step (@G=1).

The MN2020 Programmable-Gain Amplifier is packaged in a hermetically sealed, 18-pin dual-in-line package. The standard device is fully specified for either 0°C to +70°C or −55°C to +125°C ("H" model) operation. For military/aerospace or harsh-environment commercial/industrial applications, MN2020H/B CH is fully screened to MIL-H-38534 in Micro Networks MIL-STD-1772 qualified facility.

MN2020 is an excellent choice for requirements where stable accurate gains are necessary. Typical applications include microprocessor-based data acquisition systems that have to handle a wide dynamic range of analog inputs. MN2020 may be combined with Micro Networks MN7130 Multiplexed Track-Hold Amplifier and MN574A Microprocessor Interfaced A/D Converter to create a 16-channel, 12-bit, microprocessor-interfaced data acquisition system capable of accepting analog inputs from ±78mV to ± 10V full scale (19-bit dynamic range). Additional applications can be found in autoranging analog-to-digital conversion systems requiring wide dynamic ranges and in systems that autorange under program control.

MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

MN2020 DIGITALLY CONTROLLED PROGRAMMABLE-GAIN AMPLIFIER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature	−55°C to +125°C
Specified Temperature	0°C to +70°C
	−55°C to +125°C ("H" Model)
Storage Temperature	−65°C to +150°C
+15V Supply (Pin 16)	−0.5 to +18 Volts
−15V Supply (Pin 6)	+0.5 to −18 Volts
+5V Supply (Pin 5)	−0.5 to +18 Volts
Analog Input (Pin 10)	±15 Volts
Digital Inputs (Pins 2-4)	0 to +Logic Supply (Note 1)

ORDERING INFORMATION

PART NUMBER — MN2020/H/B CH

Standard part is specified for 0°C to +70°C operation.

Add "H" for specified −55°C to +125°C operation.

Add "/B" to "H" models for Environmental Stress Screening.

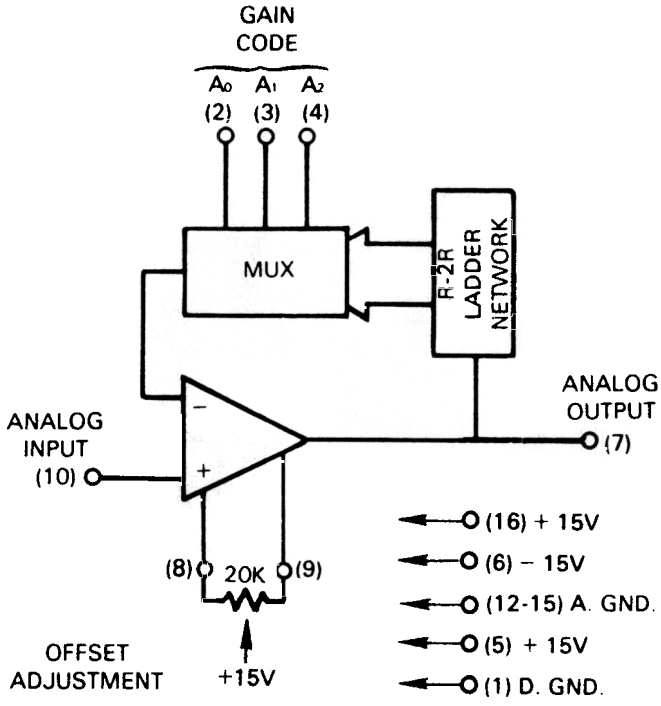
Add "CH" to "/B" models for 100% screening according to MIL-H-38534.

SPECIFICATIONS (T_A=+25°C, Supply Voltages ±15V, unless otherwise specified).

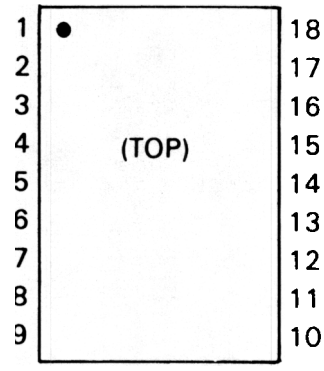
GAIN	MIN.	TYP.	MAX.	UNITS
Fixed Gain Settings		1, 2, 4, 8, 16, 32, 64, 128		
Gain Nonlinearity (Note 2): G = 1		±0.002	±0.005	% FSR (Note 3)
G = 128		±0.04	±0.08	% FSR
Gain Accuracy (Note 4) G = 1: +25°C		±0.002	±0.005	%
0°C to +70°C		±0.003	±0.008	%
−55°C to +125°C		±0.004	±0.01	%
G = 128: +25°C		±0.1	±0.2	%
0°C to +70°C		±0.1	±0.2	%
−55°C to +125°C		±0.2	±0.4	%
INPUT CHARACTERISTICS				
Input Impedance		1000		MΩ
Input Voltage Range (@G=1)		±12		V
Offset Voltage (RTI) (Notes 5 and 6)				
Initial 25°C		100		μV
Drift vs. Temperature −55°C to +125°C		5		μV/°C
Input Bias Current: +25°C		± 20	±200	pA
0°C to +70°C		± 3	± 10	nA
−55°C to +125°C ("H" Model)		±150	±500	nA
Voltage Noise (RTI)				
G=128 (0.1 to 10 Hz)		5		μVp-p
OUTPUT CHARACTERISTICS				
Output Voltage Swing	±10	±12		V
Output Current			5	mA
DYNAMIC CHARACTERISTICS				
Small Signal Bandwidth				
G=1		5		MHz
G=128		40		KHz
Full Power Bandwidth (@G=1)		100		KHz
Slew Rate		12		V/μSec
Output Settling Time to ±0.1% 20V Step (Note 7)				
G=1		5	7.5	μSec
G=128		65		μSec
GAIN SWITCHING				
Gain Control Logic Inputs				
Logical 1	+4.0			V
Logical 0			+0.8	V
Loading		1		μA
Gain Switching Time (Note 8)		0.6		μSec
POWER SUPPLY REQUIREMENTS (V_{OUT}=0)				
Power Supply Range		±15	±18	V
Current Drain (Analog Supply)		±9.2	±18	mA
Power Consumption		275	540	mW

Note 1: Digital inputs should not exceed logic supply level. Logic supply (pin 5) must be at least +5V to maintain logic levels.
Note 2: See definition of gain nonlinearity on Page 3.
Note 3: FSR = Full Scale Range. If output swing = ±12V, FSR = 24V.
Note 4: Measured between endpoints of input (output) range in order to negate the effects of the offset voltage.
Note 5: RTI = Referred to Input.
Note 6: Externally adjustable to zero.
Note 7: For each gain value, the magnitude of the input step was chosen to make the output step 20V.
Note 8: Between any two gain values.

BLOCK DIAGRAM



PINNING



1. DIGITAL GND.
2. A_0
3. A_1
4. A_2
5. +15 VOLTS (DIGITAL)
6. −15 VOLTS
7. ANALOG OUTPUT
8. OFFSET ADJ.
9. OFFSET ADJ.
10. ANALOG INPUT
11. NO CONNECTION
12. ANALOG GND.
13. ANALOG GND.
14. ANALOG GND.
15. ANALOG GND.
16. +15 VOLTS (ANALOG)
17. NO CONNECTION
18. NO CONNECTION

PROGRAMMABLE GAIN AMPLIFIER
SPECIFICATION DEFINITIONS

GAIN—The ratio of the amplitude of output signal voltage to the amplitude of input signal voltage.

GAIN ACCURACY—Either the percentage that actual gain differs from ideal gain (%) or the amount that the output, at a certain gain and input level, differs from the ideal value (volts, % FSR).

GAIN NONLINEARITY—Maximum deviation of the input-output voltage transfer function from the ideal, expressed as a percentage of the full output voltage range (FSR).

GAIN SWITCHING TIME—The time necessary for the amplifier gain to settle to within 0.1% of its new value following the appearance of a new digital code at its gain coding terminals.

INITIAL OFFSET VOLTAGE (Referred to Input)—The collection of internal voltage offsets summed and treated as a single offset voltage source appearing in series with the input. This offset, multiplied by the programmed gain, will appear at the amplifier output, even when the input signal is zero. This offset voltage can normally be zeroed out with an external trimpot.

INITIAL OFFSET VOLTAGE (RTI) DRIFT vs TEMPERATURE—Drift in initial offset voltage resulting from temperature variations. Usually expressed as V/°C or ppm of FSR /°C.

INPUT BIAS CURRENT—The current drawn into (or out of) the input terminals of the amplifier when the amplifier is turned on and the input signal is zero (input grounded).

INPUT IMPEDANCE—Total impedance seen looking into the amplifier input terminal (with the load connected) with respect to analog ground.

LOADING—The apparent load that the digital gain coding inputs of the amplifier present to their driving circuits. Usually expressed as standard logic loads (e.g. 3 TTL Loads) or in terms of the current sourced or sank when the input is a logic "0" or "1".

OUTPUT DRIVE CURRENT—Current that the amplifier will source or sink to the load while remaining within specification.

OUTPUT VOLTAGE SWING—Maximum allowable output excursion for faithful reproduction of the input signal. This is limited to several volts less than the associated power supply voltage range.

SETTLING TIME—The interval from the application of either an input step at a fixed gain or a new gain code at a fixed input level to the output's settling within a specified error band (usually 0.1%) of its final value.

SMALL SIGNAL BANDWIDTH—Frequency at which the amplifiers gain drops 3 dB from its D.C. value.

SLEW RATE—Maximum rate of change (V/Sec) in the output in response to a step change at the input or a gain change.

VOLTAGE NOISE (RTI) — Sum of the internal noise sources treated as a single source appearing in series with the input signal. The noise, multipled by the programmed gain, will appear at the amplifier output. Voltage noise is dependent upon bandwidth and may be reduced by using the minimum bandwidth necessary for a given application.

TYPICAL CHARACTERISTICS
(T_A=25°C, Supplies ±15V)

GAIN CODES AND SETTLING TIMES

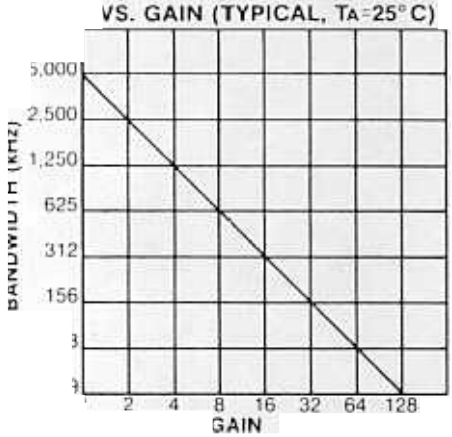
GAIN	DIGITAL CODE A_2	A_1	A_0	OUTPUT SETTLING TIME* (±0.1% 20V Step)
1	0	0	0	2.5 μSec
2	0	0	1	3 μSec
4	0	1	0	4 μSec
8	0	1	1	6 μSec
16	1	0	0	8 μSec
	0	1		17 μSec
	1	0		33 μSec
	1	1		65 μSec

GAIN ACCURACIES

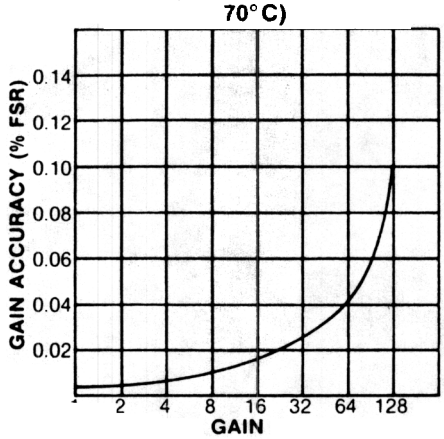
GAIN	ACCURACY (%)					
	25°C		0°C to 70°C		−55°C to +125°C	
	TYPICAL	MAX.	TYPICAL	MAX.	TYPICAL	MAX.
1	0.002	0.005	0.003	0.008	0.004	0.010
2	0.005	0.015	0.005	0.020	0.008	0.020
4	0.005	0.015	0.005	0.020	0.015	0.040
8	0.010	0.020	0.015	0.040	0.020	0.080
16	0.020	0.030	0.020	0.040	0.025	0.080
32	0.020	0.040	0.020	0.040	0.040	0.100
64	0.040	0.100	0.040	0.100	0.100	0.300
128	0.100	0.200	0.100	0.200	0.200	0.400

For each gain value the magnitude of the input step was chosen to make the output step 20V.

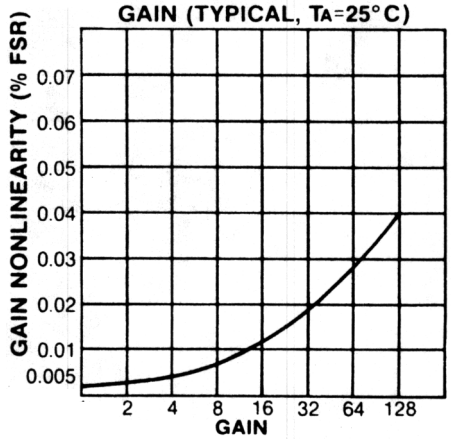
SMALL SIGNAL BANDWIDTH VS. GAIN (TYPICAL, T_A=25°C)



GAIN ACCURACY VS. GAIN (TYPICAL, T_A=0°C to 70°C)



GAIN NONLINEARITY VS. GAIN (TYPICAL, T_A=25°C)

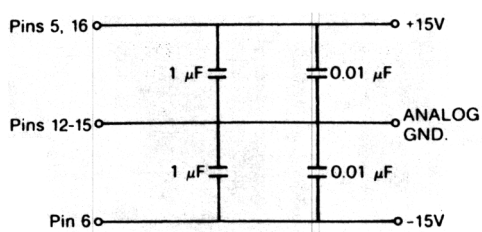


APPLICATIONS INFORMATION:

OFFSET ADJUSTMENT:
The MN2020 meets all specifications without adjustment. However, the initial offset voltage may be adjusted to zero with the addition of a trimpot between pins 8 and 9 as shown in the block diagram. A 20K, 10 turn, <100 ppm/°C TC trimpot should be used to minimize drift with temperature.

LAYOUT CONSIDERATIONS:
Proper attention to layout and decoupling is necessary to obtain specified accuracies. Analog and digital grounds are not connected internally. The four (4) analog commons (pins 12-15) and the digital common (pin 1) should be tied together as close to the package as possible, preferably to a large ground plane underneath the package. If these commons must be run separately, wide conductor runs should be used.

Power supplies should be decoupled with tantalum or electrolytic capacitors located close to the device package. For optimum results, 1μF capacitors paralleled by 0.01 μF ceramic capacitors should be connected as shown in the adjacent diagram.



INTERFACING THE MN2020 TO POPULAR MICROPROCESSORS

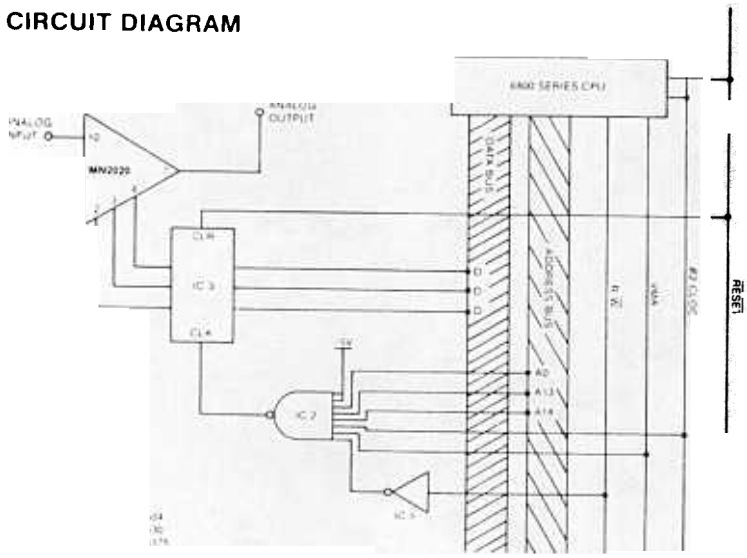
The MN2020 can be easily interfaced to microprocessors for fully automated data acquisition or other applications where it is desirable to change gain under program control. Memory mapped I/O is recommended to take advantage of the powerful memory reference instructions available in most microprocessor instruction sets. Detailed information is provided below for the 6800 Series and 8080 Series processors. Interfacing to other processors would be similar.

INTERFACING TO 6800 SERIES MICROPROCESSORS

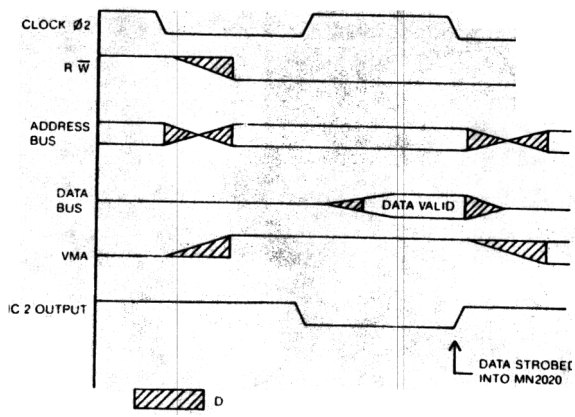
Wiring and Timing Diagrams for interfacing the MN2020 with the 6800 family of microprocessors are shown in Figure 1. In this example, the MN2020's gain control inputs are addressed and written to as a memory location with the gain code in the three lowest order bits (D_0, D_1, D_2) of the accumulator. The address bus connections shown (A14, A13, and A0) correspond to memory address 6001 hexadecimal. Redundant addressing of the MN2020 would occur at any address containing the bit combination A14, A13, A0. The MN2020 may only be written to; attempts to read the memory address assigned to the MN2020 will result in indeterminate (floating CMOS inputs) data.

The connections to the VMA, Ø2 clock and R/$\overline{W}$ lines are used to insure correct timing and to prevent spurious data that may be present on the address bus during non-memory transfer operations from addressing the MN2020. When connected as shown, the MN2020 will be reset to a gain of 1 by a reset pulse from the hardware reset control line of the 6800 System.

CIRCUIT DIAGRAM



TIMING DIAGRAM

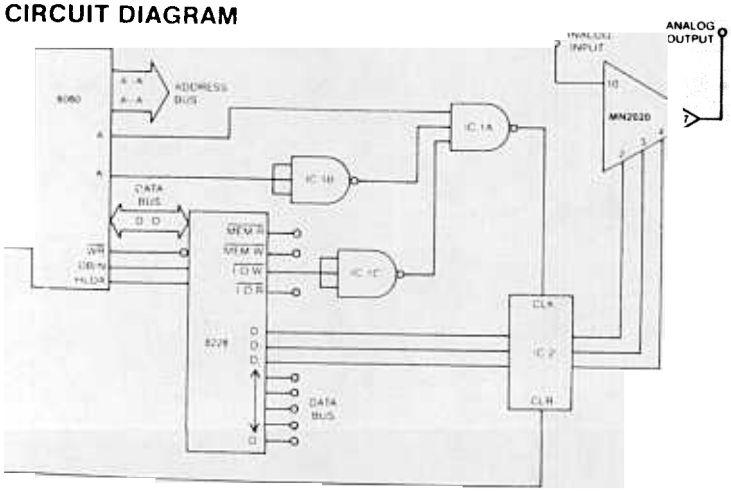


INTERFACING TO 8080 SERIES MICROPROCESSORS

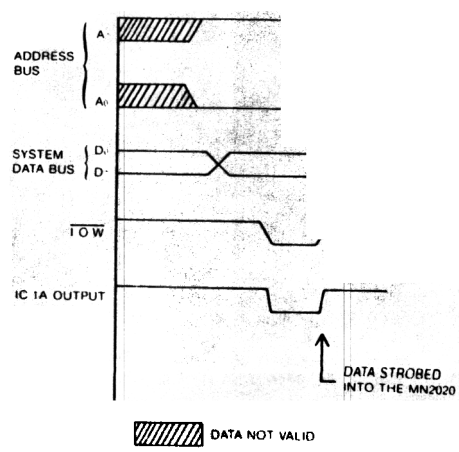
Wiring and Timing Diagrams for interfacing the MN2020 with the 8080 family of microprocessors are shown in Figure 2. In this example, an 8228 system controller is used, and the MN2020 is treated as a standard I/O device. The gain code is written, as an output instruction, to the MN2020 which is located at I/O address 80 hexadecimal.

When the values of A7, A0, and $\overline{\text{I/O W}}$ are "1", "0" and "0" respectively, the output of IC 1A will go to logic zero. When either of the address or $\overline{\text{I/O W}}$ outputs leaves the above state, the output of IC2 is forced to a logic one, with the rising edge triggering the latch IC2 which strobes the gain code information into the MN2020.

CIRCUIT DIAGRAM



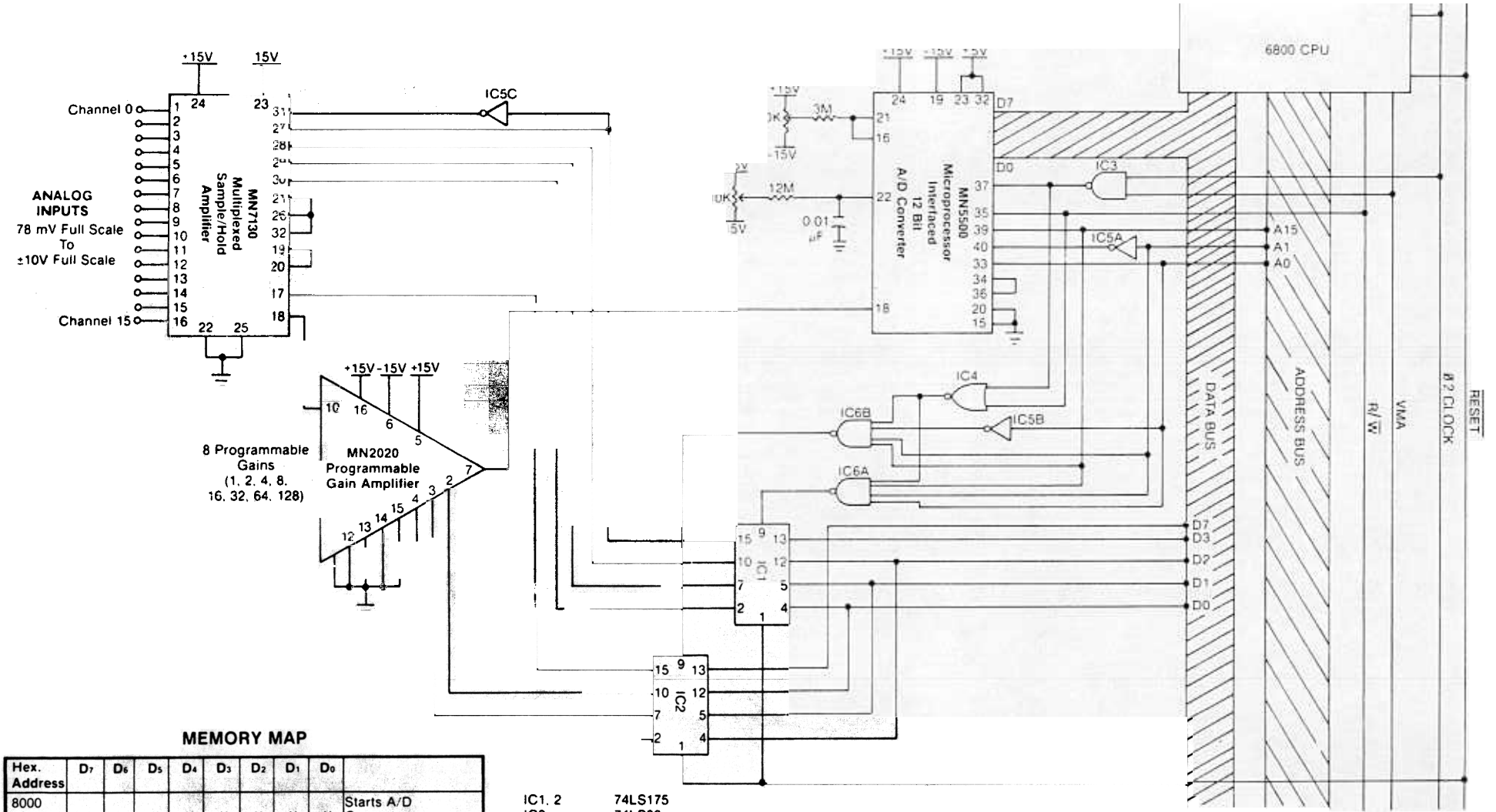
TIMING DIAGRAM



MN2020

12 Bit—16 Channel Data Acquisition System

WITH 19 BITS OF DYNAMIC RANGE AND AUTORANGING CAPABILITY



MEMORY MAP

Hex. Address	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
8000 (Write)	X	X	X	X	X	X	X	X	Starts A/D Converter
8001 (Read)	STATUS	"1"	"1"	"1"	MSB	Bit 2	Bit 3	Bit 4	Digitized Data MSB Byte
8000 (Read)	Bit 5	Bit 6	Bit 7	Bit 8	Bit 9	Bit 10	Bit 11	LSB	Digitized Data LSB Byte
8002 (Write)	S/H	X	X	X	X	A_2	A_1	A_0	PGA Gain S/H Command
8003 (Write)	X	X	X	X	A_4	A_2	A_1	A_0	Multiplexed S/H—Channel Address

IC1, 2	74LS175
IC3	74LS00
IC4	74LS02
IC5	74LS04
IC6	74LS20