LX5506B

InGaP HBT 4 – 6GHz Power Amplifier

PRODUCTION DATA SHEET

DESCRIPTION

The LX5506B is a power amplifier optimized for the FCC Unlicensed National Information Infrastructure (U-NII) band, HyperLAN2 and Japan WLAN applications in the 4.9-5.85 GHz frequency range. The PA is implemented as a three-stage monolithic microwave integrated circuit (MMIC) with active bias, on-chip input matching and output pre-matching. It also features an on-chip output power detector to help reduce BOM cost and PCB board space for system implementations. The device is manufactured with an InGaP/GaAs Heterojunction Bipolar Transistor (HBT) IC process (MOCVD). It operates with a single positive voltage supply of 3.3V (nominal), with +26dBm of P1dB and up to 25dB power gain in the 5.15 - 5.85GHz frequency range with a simple output matching capacitor pair.

LX5506B is available in a 16-pin 3mmx3mm micro-lead package (MLP). The compact footprint, low profile, and excellent thermal capability of the MLP package makes the LX5506B an ideal solution for broadband, high-gain power amplifier requirements for IEEE 802.11a, and HiperLAN2 portable WLAN applications.

IMPORTANT: For the most current data, consult *MICROSEMI*'s website: **http://www.microsemi.com**

KEY FEATURES

- Advanced InGaP HBT
- Single-Polarity Voltage Supply
- EVM ~ 2.5% at Pout=+18dBm, 64QAM/ 54Mbps OFDM (3.3V)
- Power Gain ~ 25dB at 5.25GHz & Pout=+18dBm
- Power Gain ~ 21dB at 5.85GHz & Pout=+18dBm
- P1dB ~ +26dBm across 5.15 – 5.85 GHz
- Total Current ~ 170mA for Pout=+18dBm at 5.25GHz
- Total Current ~ 200mA for Pout=+20dBm at 5.25GHz
- ACPR ~ -48dBc at 30MHz Offset at Pout=+18dBm
- Integrated Power Detector
- Complete On-Chip Input Match
- Simple Output Capacitor Match
- Small Footprint: 3x3mm2
- Low Profile: 0.9mm

PRODUCT HIGHLIGHT

APPLICATIONS/BENEFITS

- FCC U-N11 Wireless
- IEEE 802.11a
- HiperLAN2

PACKAGE ORDER INFO

LQ	**Plastic MLPQ 16-Pin**

LX5506B-LQ

Note: Available in Tape & Reel. Append the letters "TR" to the part number. (i.e. LX5506B-LQTR)

This device is classified as ESD Level 0 in accordance with MIL-STD-883, Method 3015 (HBM) testing. Appropriate ESD procedures should be observed when handling this device.

Rev. 1.0, 2004-05-25

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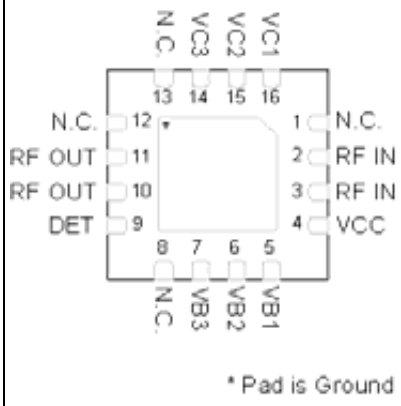
Integrated Products Division
11861 Western Avenue, Garden Grove, CA. 92841, 714-898-8121, Fax: 714-893-2570

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage, RF Off.....6V
Collector Current 500mA
Total Power Dissipation.....3W
RF Input Power.....15dBm
Thermal Resistance (Junction-to-Case, θ_{JC}).....6°C/W
Maximum Junction Temperature (T_J max) ..... 150°C
Operation Ambient Temperature .....-40 to +85°C
Storage Temperature.....-60 to 150°C
Package Peak Temp for Solder Reflow (40 Seconds Maximum Exposure). 255°C (+5, -0)

Note: Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of specified terminal.

PACKAGE PIN OUT



LQ PACKAGE
(Bottom View)

Pb-free 100% Matte Tin Lead Finish

FUNCTIONAL PIN DESCRIPTION

Name	Pin #	Description
RF IN	2, 3	RF input for the power amplifier. This pin is DC-shorted to GND but AC-coupled to the transistor base of the first stage.
VCC	4	Supply voltage for the bias reference and control circuits. This pin can be combined with VC1, VC2 and VC3 pins, resulting in a single supply voltage (referred to as Vc).
VB1 VB2 VB3	5 6 7	Bias control voltage for the first stage. Bias control voltage for the second stage. Bias control voltage for the third stage.
DET	9	Detector output for the third stage PA output power.
RF OUT	10, 11	RF output for the power amplifier. This pin is DC-blocked from the collector of the output stage.
VC1 VC2 VC3	16 15 14	DC supply voltage for the first stage amplifier. DC supply voltage for the second stage amplifier. DC supply voltage for the third stage amplifier.
GND	Center Metal	The center metal base of the MLP package provides both DC/RF ground as well as heat sink for the power amplifier.
NC	1, 8, 12,13	These pins are unused and not connected to the device inside the package. They can be treated either as open (floating) pins, or connected to ground metal.

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ELECTRICAL CHARACTERISTICS

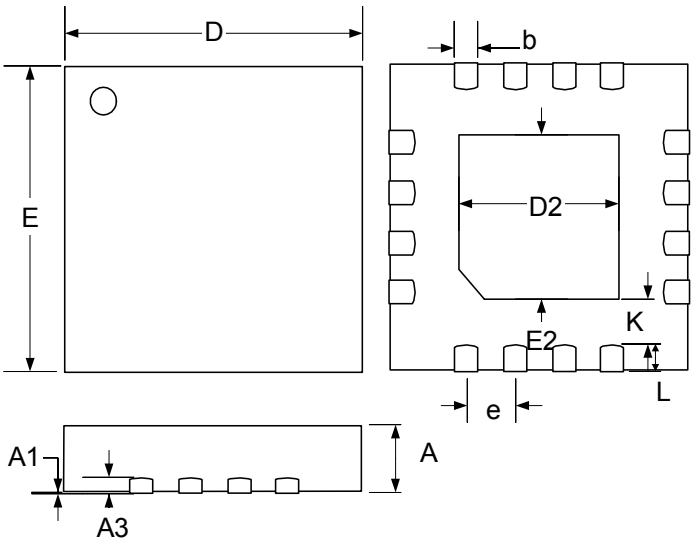
Unless otherwise specified, the following specifications apply over the following test conditions: Vc = 3.3V, Vref=2.9V, Icq = 90mA, and T_A = 25°C

PARAMETER	CONDITION	SYMBOL	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNIT
Frequency Range		f	5.15		5.35	5.7		5.85	GHz
Output Power at 1dB Compression		Pout	25	26		25	26		dBm
Power Gain at Pout=+18dBm		Gp		25			21		dB
EVM at Pout=+18dBm	64QAM/54Mbps			2.5			3		%
Total Current at Pout=+18dBm		Ic_total		170			180		mA
Quiescent Current		Icq		90			90		mA
Bias Control Reference Current	For Icq=90mA	Iref		4.2			4.2		mA
Small-Signal Gain		S21		24			20		dB
Gain Flatness	Over 200MHz	ΔS21		+/-0.5			+/-0.5		dB
Gain Variation Over Temperature	-40 to +85°C	ΔS21		+/-1			+/-0.5		dB
Input Return Loss		S11		-15			-10		dB
Output Return Loss		S22		-8			-10		dB
Reverse Isolation		S12		-40			-40		dB
Second Harmonic	Pout = +18dBm			-40			-40		dBc
Third Harmonic	Pout = +18dBm			-40			-40		dBc
Detector Response	Pout = +18dBm	DET		1.6			2.2		V
Ramp-On Time	10~90%	t_{ON}		100			100		ns

Note: All measured data was obtained on a 10 mil GETEK evaluation board.

PACKAGE DIMENSIONS

LQ 16-Pin MLPQ 3x3 (75 x 75 mil DAP)



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.80	1.00	0.031	0.039
A1	0	0.05	0	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	3.00 BSC		0.118 BSC	
E	3.00 BSC		0.118 BSC	
e	0.50 BSC		0.020 BSC	
D2	1.55	1.80	0.061	0.071
E2	1.55	1.80	0.061	0.071
K	0.2	-	0.008	-
L	0.35	0.50	0.012	0.020

Note:

1. Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm(.006") on any side. Lead dimension shall not include solder coverage.

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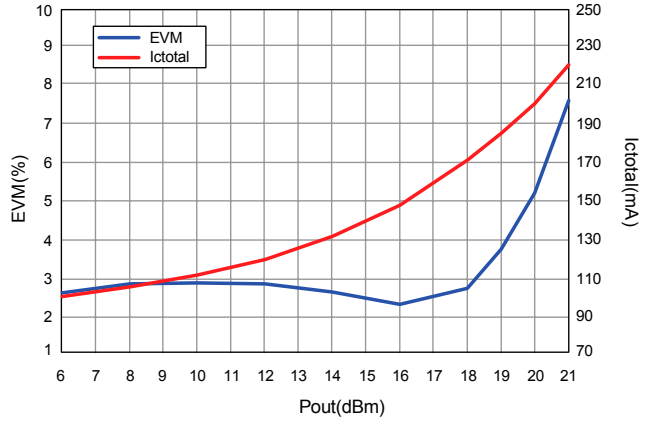
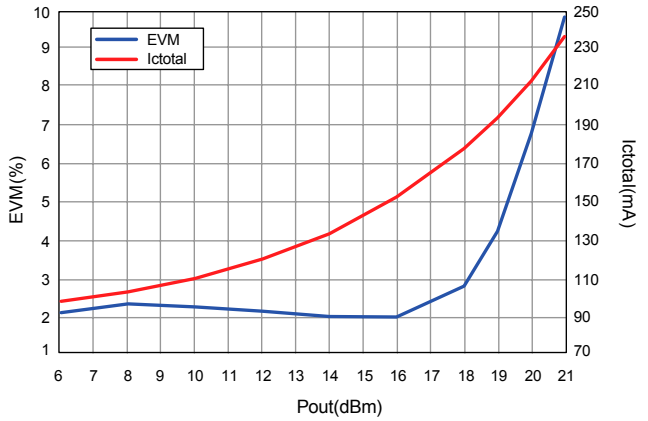
EVM & CURRENT VS POUT @ 5.25GHZ



V_C = 3.3V, V_{REF} = 2.9V, I_{CQ} = 90mA, Frequency = 5.25GHz, 64QAM / 54 Mbps

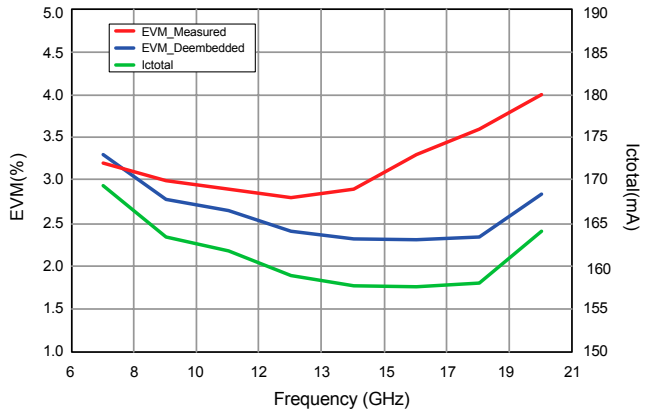
EVM & CURRENT VS POUT @ 5.85GHZ



V_C = 3.3V, V_{REF} = 2.9V, I_{CQ} = 90mA, Frequency = 5.85GHz, 64QAM / 54 Mbps

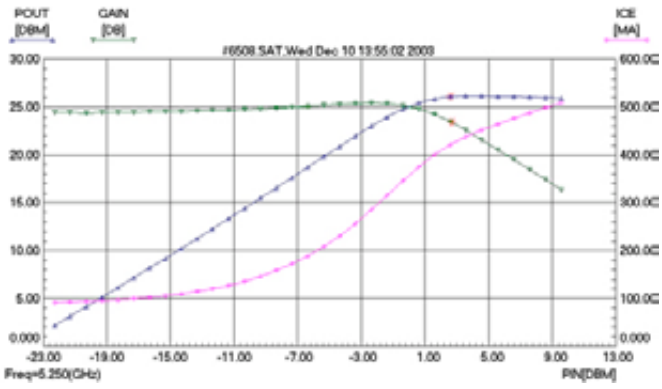
Note: All EVM data are for OFDM signal of 64QAM/54Mbps from Yokogawa VG6000, and are actual measured data without any de-embedding. Source EVM is 1.4 - 1.8% for input power levels for test

EVM & CURRENT VS FREQUENCY



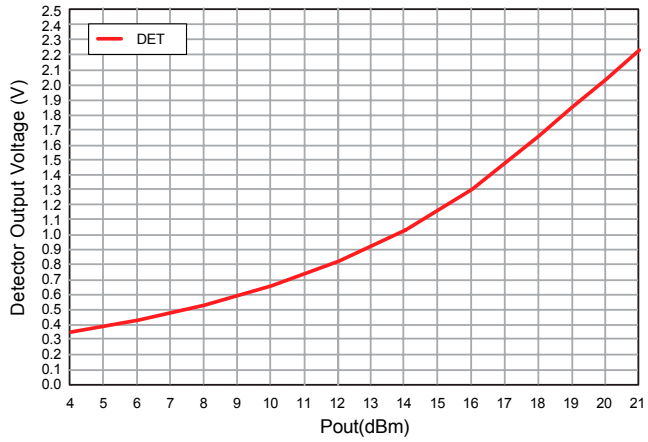
V_C = 3.3V, V_{REF} = 2.9V, I_{CQ} = 90mA, P_{OUT} = +18dBm, 64QAM / 54 Mbps

TYPICAL POWER SWEEP @ 5.25GHZ



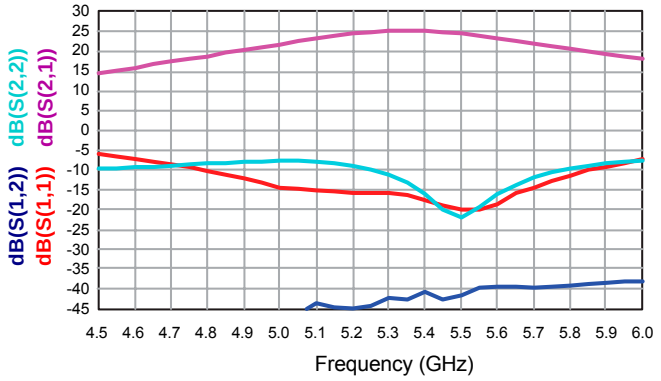
V_C = 3.3V, V_{REF} = 2.9V, I_{CQ} = 90mA, Frequency = 5.25GHz, CW Input

TYPICAL POWER DETECT RESPONSE



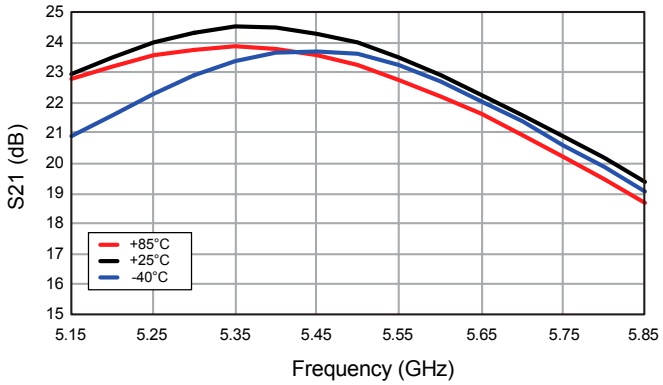
V_C = 3.3V, V_{REF} = 2.9V, I_{CQ} = 90mA, Frequency = 5.25GHz, 64QAM / 54 Mbps

TYPICAL S-PARAMETER @ ROOM TEMP



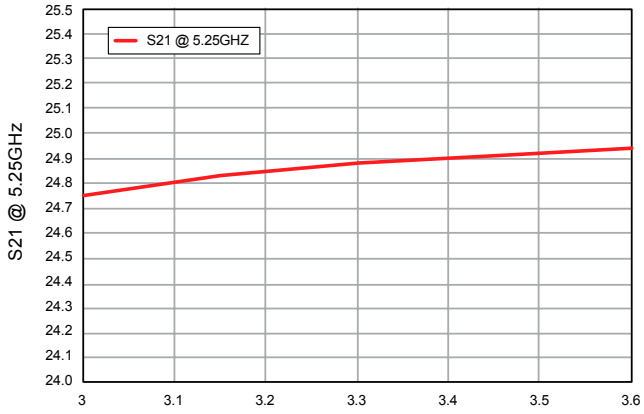
V_C = 3.3V, V_{REF} = 2.9V, I_{CQ} = 90mA

SMALL SIGNAL GAIN OVER TEMP



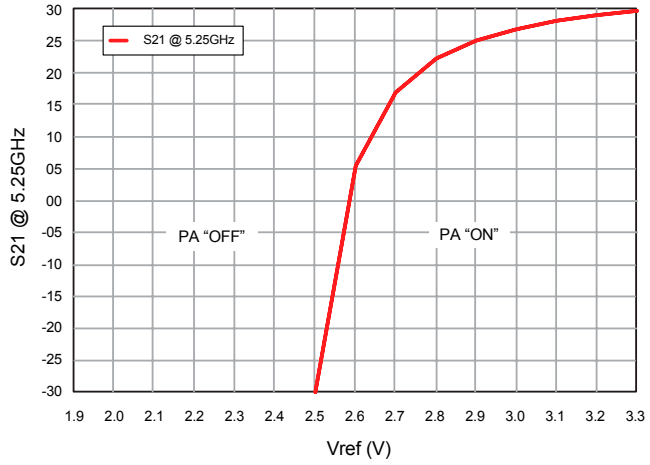
V_C = 3.3V, V_{REF} = 2.9V, I_{CQ} = 90mA @ Room Temperature

SMALL SIGNAL VS SUPPLY VOLTAGE



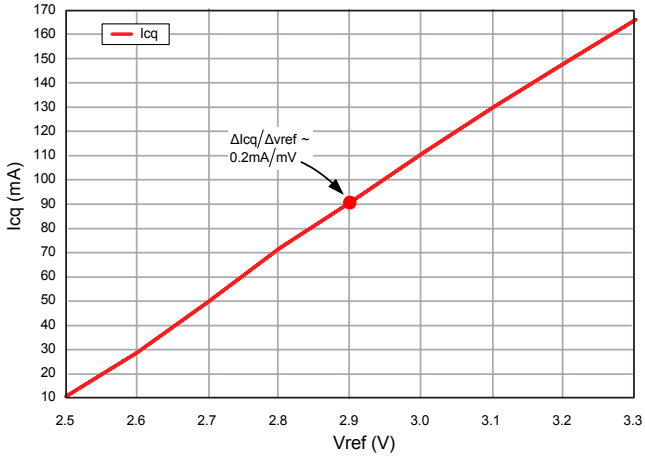
V_{REF} = 2.9V, I_{CQ} = 90mA for Nominal V_C =-3.3V

SMALL SIGNAL VS. REF VOLTAGE



V_C = 3.3V, I_{CQ} = 90mA for Nominal V_{REF} = 2.9V

QUESCENT CURRENT VS. REF VOLTAGE



VC = 3.3V, I_{CQ} = 90mA for Nominal V_{REF} = 2.9V

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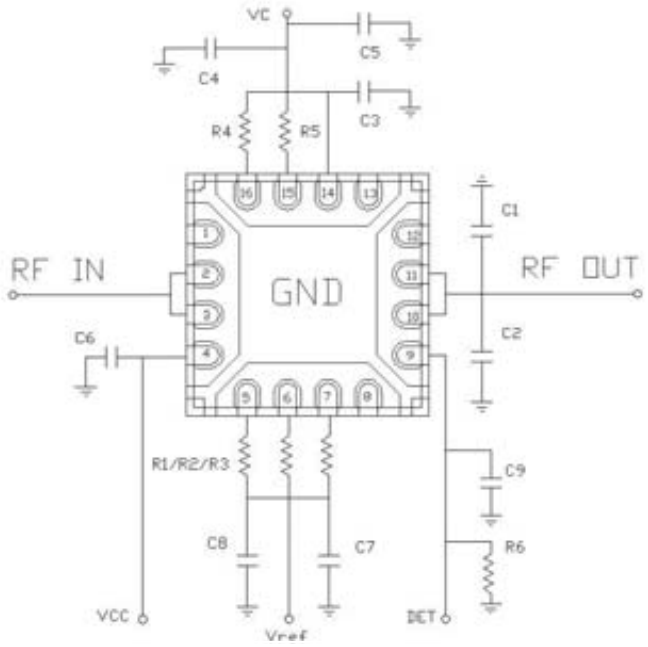
APPLICATION SCHEMATIC & BILL OF MATERIALS



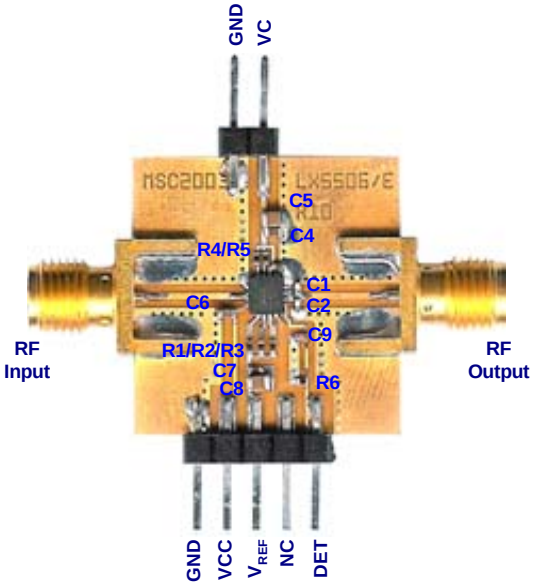
Substrate:
10 mil GETEK
ε_r = 3.9, tan δ = 0.02
50 Ohm microstrip line width = 20 mil

Recommended BOM

Location	Value
C1=C2	0.5 pF (0402)
C3	220 pF (0402)
C4=C6	1 µF (0603)
C5=C8	10 µF (0805)
C7	1 nF (0402)
C9	10 pF (0402)
R1/R2/R3	140/270/560 Ω (0402)
R4/R5	15/15 Ω (0402)
R6	100 KΩ (0402)

Notes:
1) C1/C2 position should be ~40mil from right edge of MLP package.
2) All other component positions are not critical.
3) C4/C5/C6 may not be needed in PA layout if supply voltage is already well filtered on PCB.
4) C7 ensures ~100ns switching time for PA on/off.
5) C8 is for standalone eval board test only. It is not needed in system implementation when the switched bias control voltage is well filtered before reaching the Vref node.

EVALUATION BOARD



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NOTES