

Silicon Power Transistors

The MJ21195 and MJ21196 utilize Perforated Emitter technology and are specifically designed for high power audio output, disk head positioners and linear applications.

- Total Harmonic Distortion Characterized
- High DC Current Gain –
 $h_{FE} = 25 \text{ Min @ } I_C = 8 \text{ Adc}$
- Excellent Gain Linearity
- High SOA: 3 A, 80 V, 1 Second

MAXIMUM RATINGS

Rating	Sym- bol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	250	Vdc
Collector–Base Voltage	V_{CBO}	400	Vdc
Emitter–Base Voltage	V_{EBO}	5	Vdc
Collector–Emitter Voltage – 1.5 V	V_{CEX}	400	Vdc
Collector Current — Continuous Peak (1)	I_C	16 30	Adc
Base Current — Continuous	I_B	5	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate Above 25°C	P_D	250 1.43	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C} \pm 5^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
Collector–Emitter Sustaining Voltage ($I_C = 100 \text{ mAdc}, I_B = 0$)	$V_{CEO(sus)}$	250	—	—	Vdc
Collector Cutoff Current ($V_{CE} = 200 \text{ Vdc}, I_B = 0$)	I_{CEO}	—	—	100	μAdc

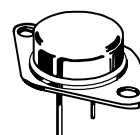
(1) Pulse Test: Pulse Width = 5 μs , Duty Cycle $\leq 10\%$.

(continued)

PNP
MJ21195*
NPN
MJ21196*

*ON Semiconductor Preferred Device

**16 AMPERE
COMPLEMENTARY
SILICON POWER
TRANSISTORS
250 VOLTS
250 WATTS**



**CASE 1-07
TO-204AA
(TO-3)**

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

MJ21195 MJ21196

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
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OFF CHARACTERISTICS

Emitter Cutoff Current ($V_{CE} = 5 \text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	100	μAdc
Collector Cutoff Current ($V_{CE} = 250 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$)	I_{CEX}	—	—	100	μAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased ($V_{CE} = 50 \text{ Vdc}$, $t = 1 \text{ s}$ (non-repetitive)) ($V_{CE} = 80 \text{ Vdc}$, $t = 1 \text{ s}$ (non-repetitive))	$I_{S/b}$	5 2.5	— —	— —	Adc
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ON CHARACTERISTICS

DC Current Gain ($I_C = 8 \text{ Adc}$, $V_{CE} = 5 \text{ Vdc}$) ($I_C = 16 \text{ Adc}$, $V_{CE} = 5 \text{ Vdc}$)	h_{FE}	25 8	— —	75	
Base-Emitter On Voltage ($I_C = 8 \text{ Adc}$, $V_{CE} = 5 \text{ Vdc}$)	$V_{BE(on)}$	—	—	2.2	Vdc
Collector-Emitter Saturation Voltage ($I_C = 8 \text{ Adc}$, $I_B = 0.8 \text{ Adc}$) ($I_C = 16 \text{ Adc}$, $I_B = 3.2 \text{ Adc}$)	$V_{CE(sat)}$	— —	— —	1.4 4	Vdc

DYNAMIC CHARACTERISTICS

Total Harmonic Distortion at the Output $V_{RMS} = 28.3 \text{ V}$, $f = 1 \text{ kHz}$, $P_{LOAD} = 100 \text{ WRMS}$ $h_{FE \text{ unmatched}}$ $h_{FE \text{ matched}}$ (Matched pair $h_{FE} = 50 @ 5 \text{ A/5 V}$)	T_{HD}	— —	0.8 0.08	— —	%
Current Gain Bandwidth Product ($I_C = 1 \text{ Adc}$, $V_{CE} = 10 \text{ Vdc}$, $f_{test} = 1 \text{ MHz}$)	f_T	4	—	—	MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f_{test} = 1 \text{ MHz}$)	C_{ob}	—	—	500	pF

(1) Pulse Test: Pulse Width = 300 μs , Duty Cycle $\leq 2\%$

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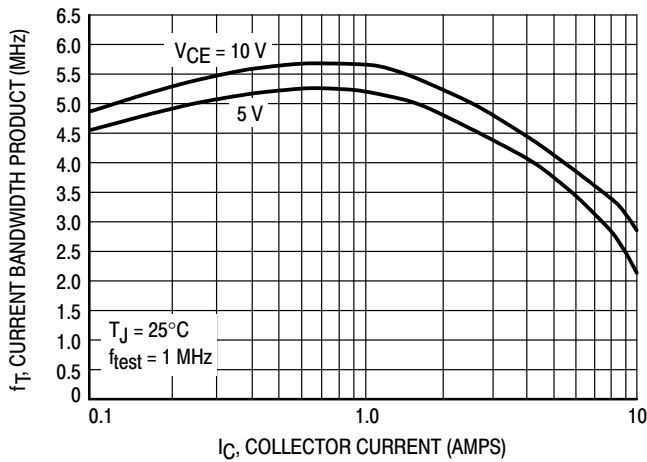


Figure 1. Typical Current Gain Bandwidth Product

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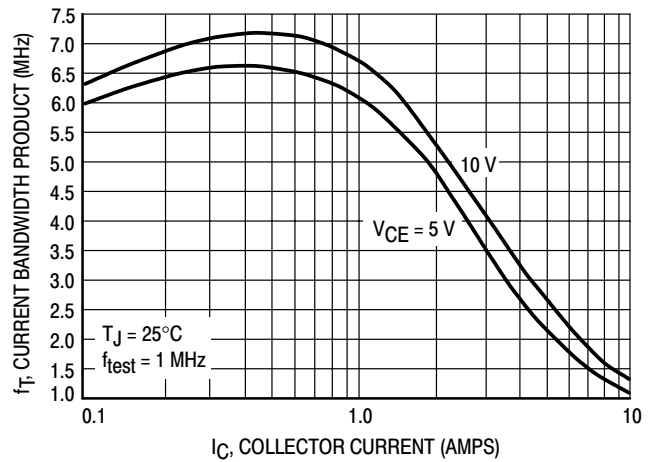


Figure 2. Typical Current Gain Bandwidth Product

TYPICAL CHARACTERISTICS

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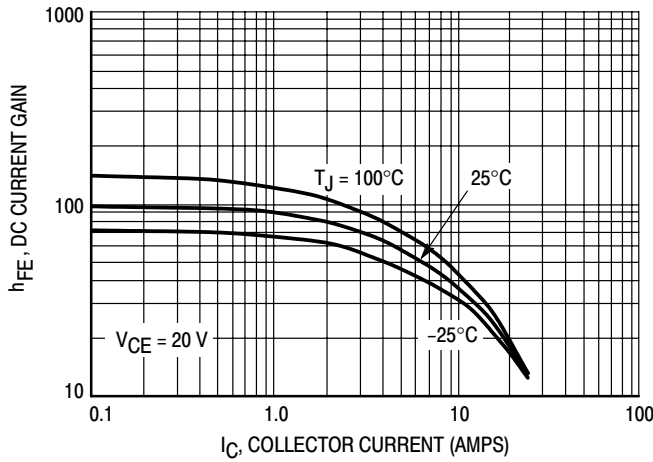


Figure 3. DC Current Gain, $V_{CE} = 20\text{ V}$

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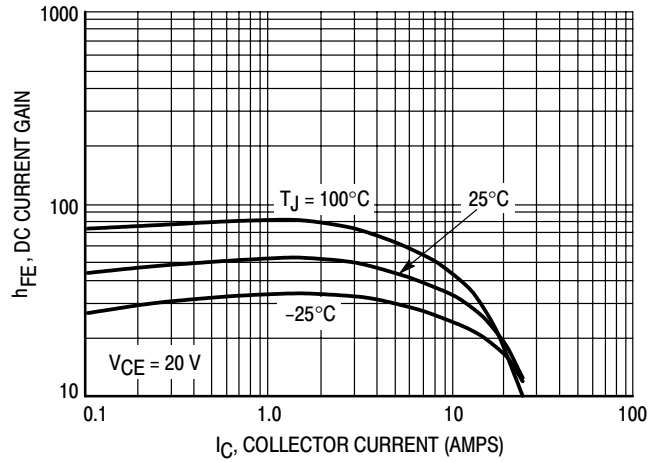


Figure 4. DC Current Gain, $V_{CE} = 20\text{ V}$

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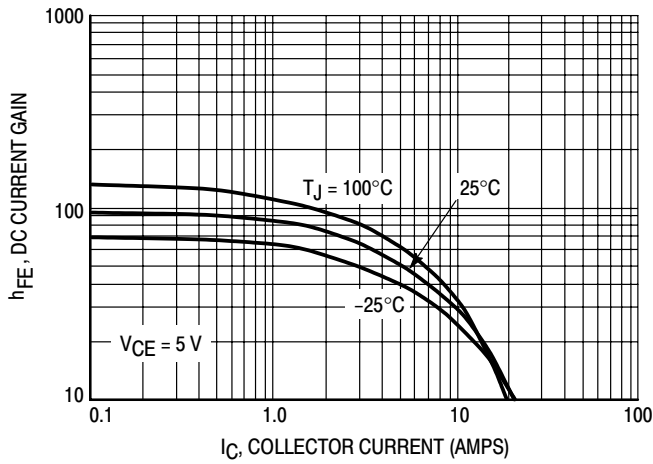


Figure 5. DC Current Gain, $V_{CE} = 5\text{ V}$

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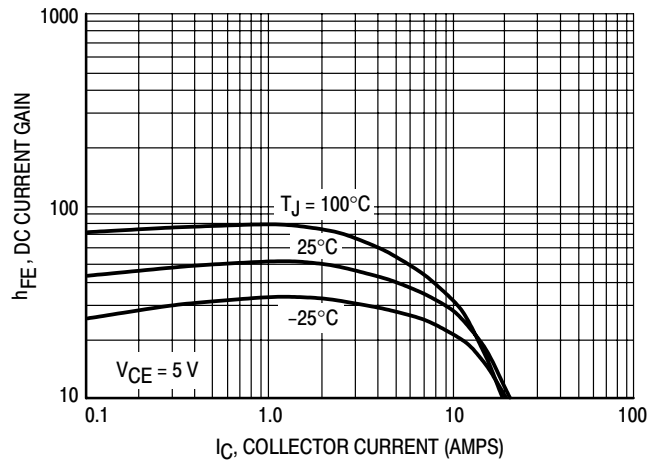


Figure 6. DC Current Gain, $V_{CE} = 5\text{ V}$

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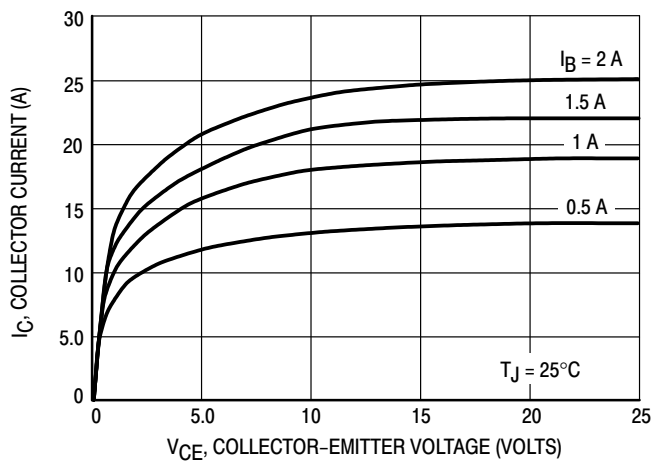


Figure 7. Typical Output Characteristics

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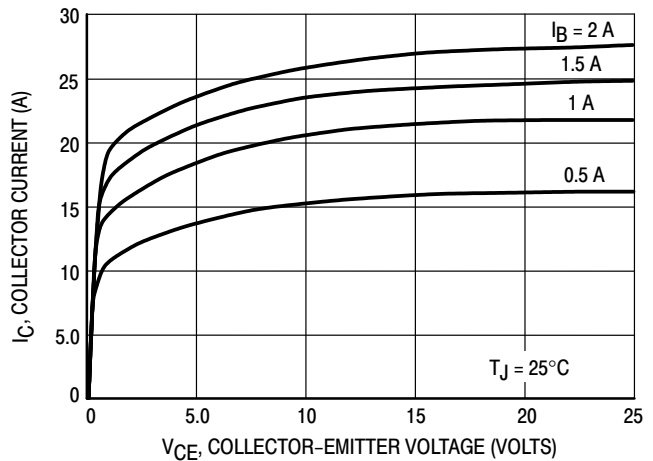


Figure 8. Typical Output Characteristics

TYPICAL CHARACTERISTICS

PNP MJ21195

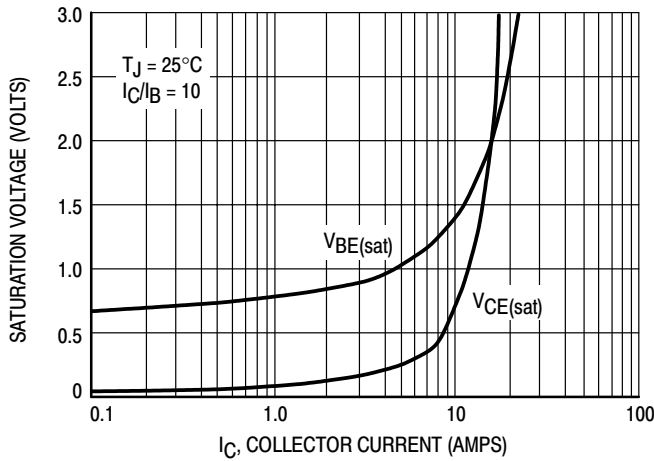


Figure 9. Typical Saturation Voltages

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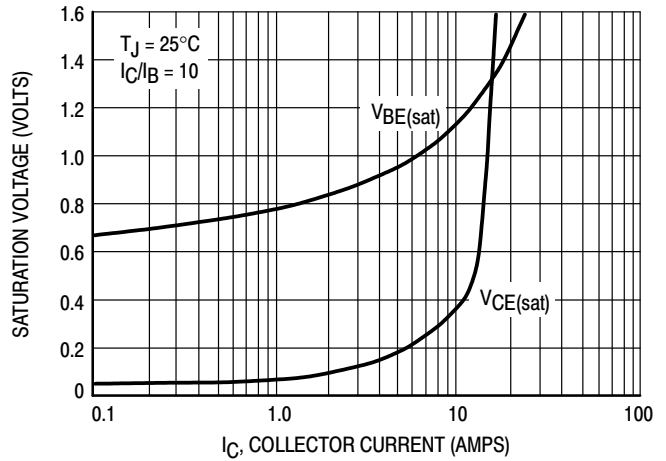


Figure 10. Typical Saturation Voltages

PNP MJ21195

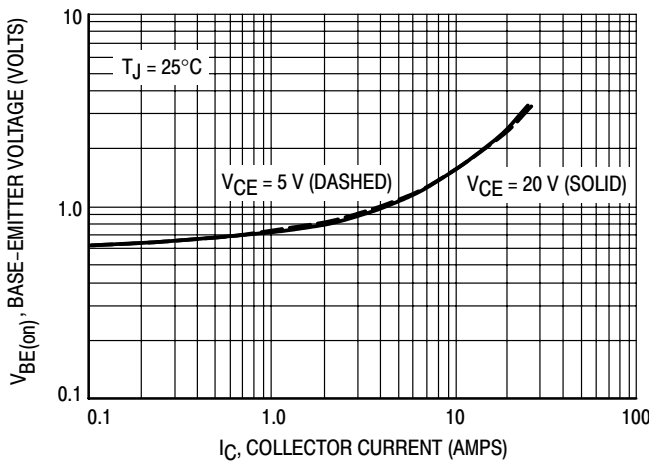


Figure 11. Typical Base-Emitter Voltage

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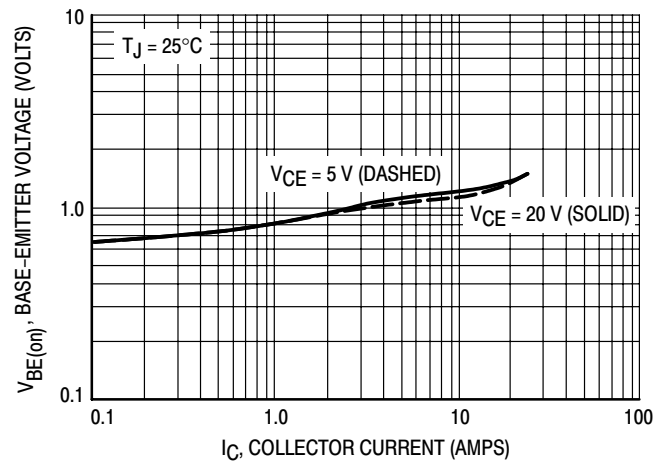


Figure 12. Typical Base-Emitter Voltage

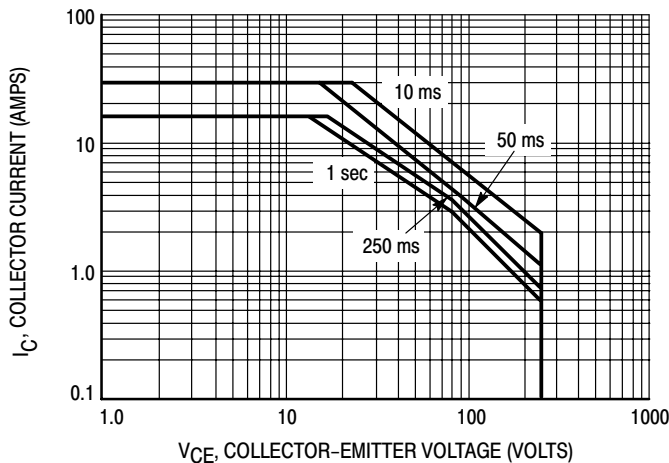


Figure 13. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on $T_{J(pk)} = 200^\circ\text{C}$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

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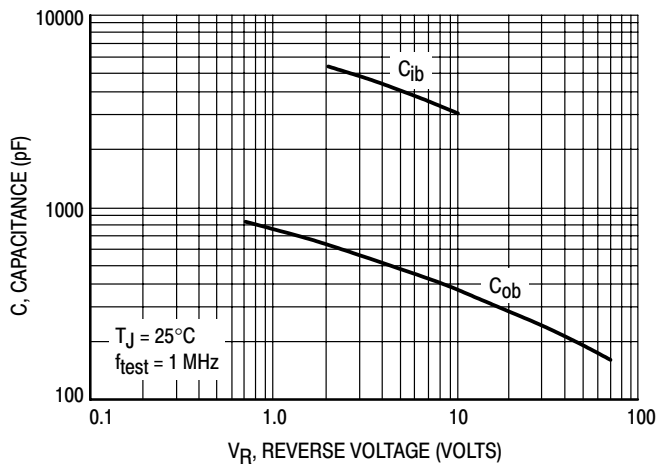


Figure 14. MJ21195 Typical Capacitance

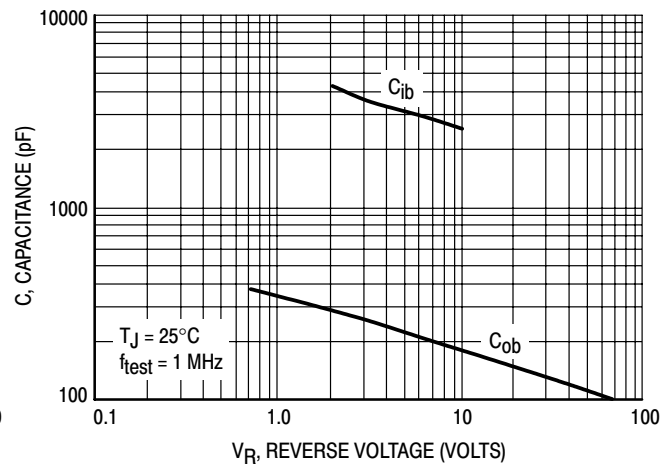


Figure 15. MJ21196 Typical Capacitance

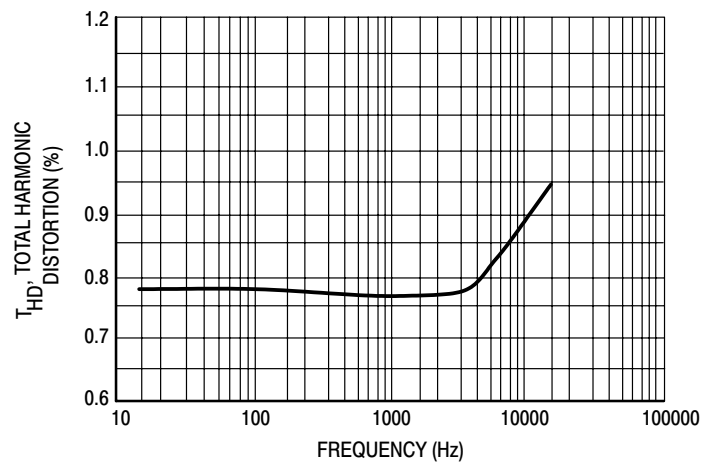


Figure 16. Typical Total Harmonic Distortion

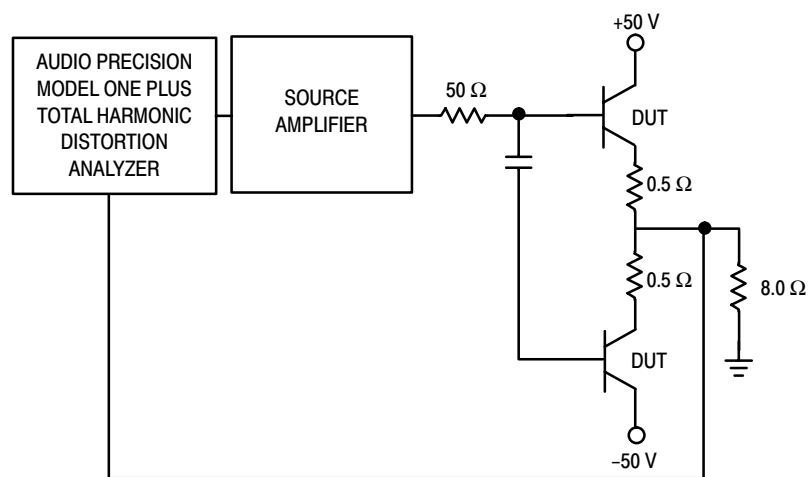
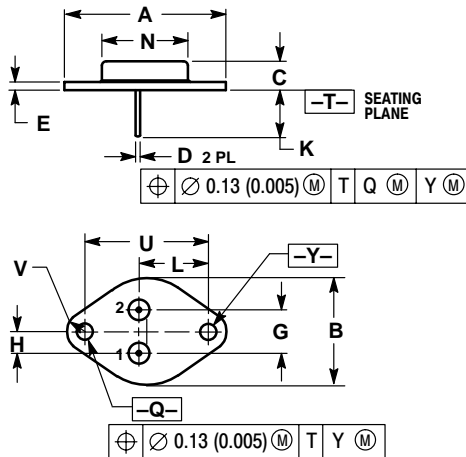


Figure 17. Total Harmonic Distortion Test Circuit

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PACKAGE DIMENSIONS

TO-204 (TO-3) CASE 1-07 ISSUE Z



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.550 REF		39.37 REF	
B	---	1.050	---	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	---	0.830	---	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

Notes

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