

SN74LS682, SN74LS684, SN74LS688

8-Bit Magnitude Comparators

The SN74LS682, 684, 688 are 8-bit magnitude comparators. These device types are designed to perform comparisons between two eight-bit binary or BCD words. All device types provide $\overline{P} = \overline{Q}$ outputs and the LS682 and LS684 have $\overline{P} > \overline{Q}$ outputs also.

The LS682, LS684 and LS688 are totem pole devices. The LS682 has a 20 k Ω pullup resistor on the Q inputs for analog or switch data.

TYPE	$\overline{P} = \overline{Q}$	$\overline{P} > \overline{Q}$	OUTPUT ENABLE	OUTPUT CONFIGURATION	PULLUP
LS682	yes	yes	no	totem-pole	yes
LS684	yes	yes	no	totem-pole	no
LS688	yes	no	yes	totem-pole	no

GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	4.75	5.0	5.25	V
T _A	Operating Ambient Temperature Range	0	25	70	°C
I _{OH}	Output Current – High			– 0.4	mA
I _{OL}	Output Current – Low			24	mA

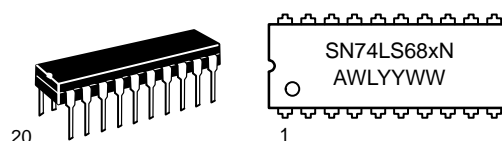


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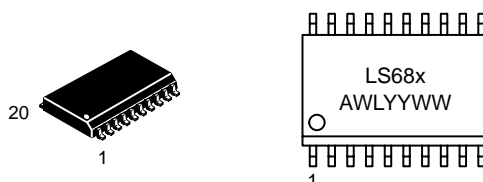
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LOW POWER SCHOTTKY

MARKING DIAGRAMS



PDIP–20
N SUFFIX
CASE 738



SOIC–20
DW SUFFIX
CASE 751D

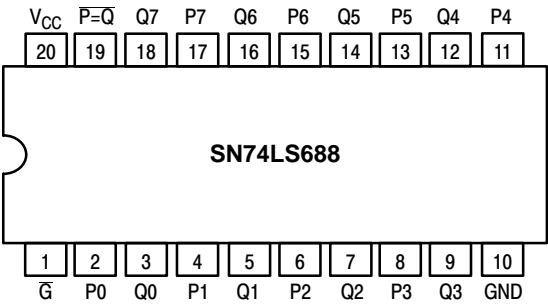
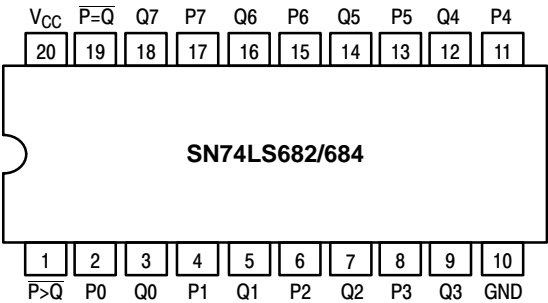
x = 2, 4, or 8
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
SN74LS682N	PDIP–20	1440 Units/Box
SN74LS682DW	SOIC–20	2500/Tape & Reel
SN74LS684N	PDIP–20	1440 Units/Box
SN74LS684DW	SOIC–20	2500/Tape & Reel
SN74LS688N	PDIP–20	1440 Units/Box
SN74LS688DW	SOIC–20	2500/Tape & Reel

SN74LS682, SN74LS684, SN74LS688

CONNECTION DIAGRAMS (TOP VIEW)



FUNCTION TABLE

INPUTS			OUTPUTS	
DATA	ENABLES		$\overline{P=Q}$	$\overline{P>Q}$
P, Q	$\overline{G}, \overline{GT}$	G2		
$\overline{P=Q}$ $\overline{P>Q}$ $\overline{P<Q}$ X	L L L H	L L L H	L H H H	H L H H

H = HIGH Level, L = LOW Level, X = Irrelevant

SN74LS682, SN74LS684, SN74LS688

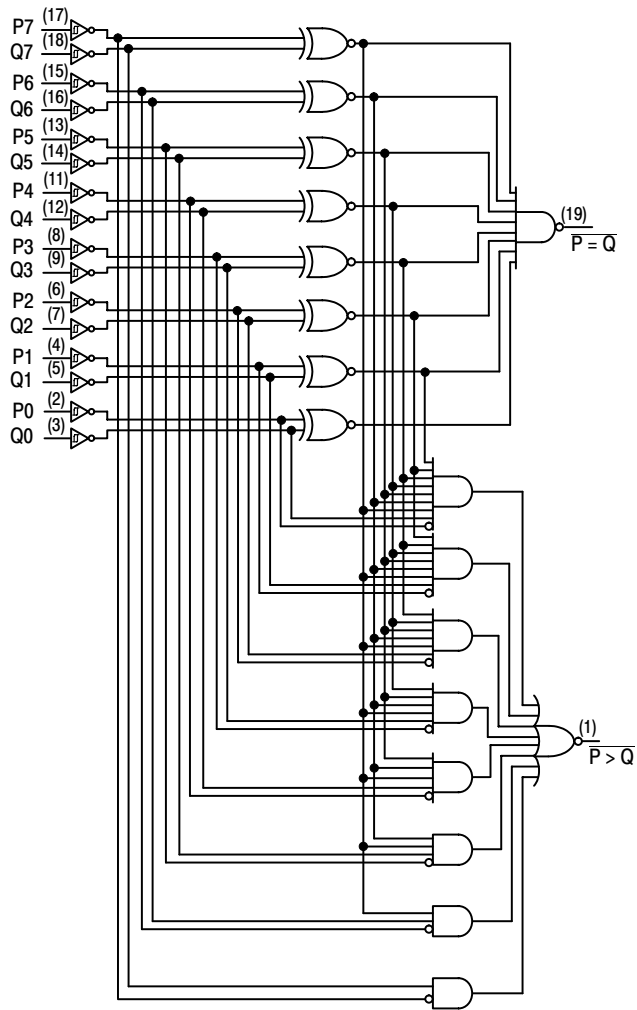
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V_{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$, $I_{IN} = -18 \text{ mA}$
V_{OH}	Output HIGH Voltage	2.7	3.5		V	$V_{CC} = \text{MIN}$, $I_{OH} = \text{MAX}$, $V_{IN} = V_{IH}$ or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.25	0.4	V	$I_{OL} = 12 \text{ mA}$
			0.35	0.5	V	$I_{OL} = 24 \text{ mA}$
I_{IH}	Input HIGH Current			20	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7 \text{ V}$
		LS682-Q Inputs		0.1	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 5.5 \text{ V}$
		Others		0.1	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 7.0 \text{ V}$
I_{IL}	Input LOW Current	LS682-Q Inputs		-0.4	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 0.4 \text{ V}$
		Others		-0.2	mA	
I_{OS}	Short Circuit Current (Note 1.)	-30		-130	mA	$V_{CC} = \text{MAX}$
I_{CC}	Power Supply Current	LS682		70	mA	$V_{CC} = \text{MAX}$
		LS684		65	mA	
		LS688		65	mA	

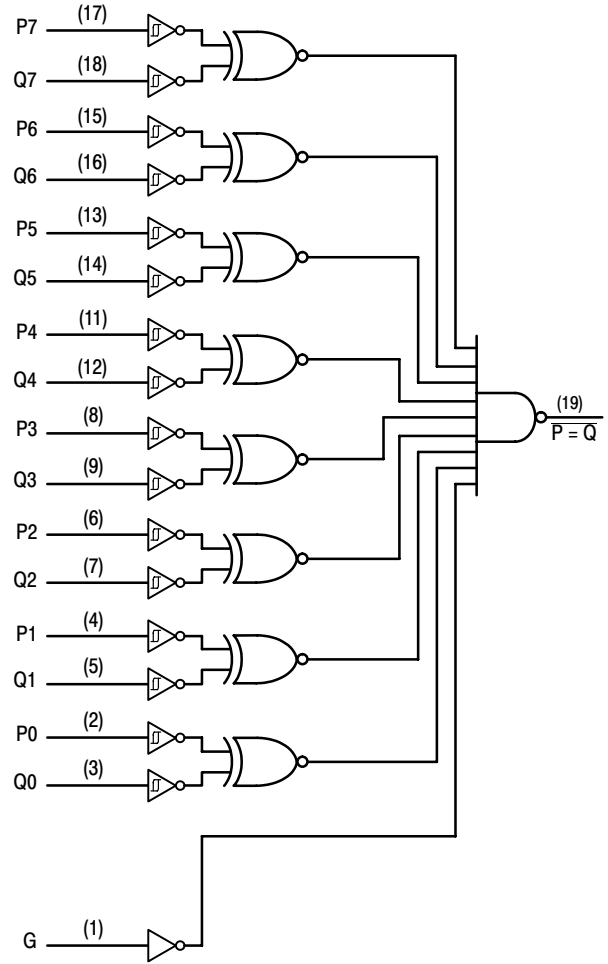
1. Not more than one output should be shorted at a time, nor for more than 1 second.

SN74LS682, SN74LS684, SN74LS688

LOGIC DIAGRAMS



SN74LS682 and LS684



SN74LS688

SN74LS682, SN74LS684, SN74LS688

AC CHARACTERISTICS (T_A = 25°C)

SN74LS682

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _{PLH} t _{PHL}	Propagation Delay, P to $\overline{P} = \overline{Q}$		13 15	25 25	ns	V _{CC} = 5.0 V C _L = 45 pF R _L = 667 Ω
t _{PLH} t _{PHL}	Propagation Delay, Q to $\overline{P} = \overline{Q}$		14 15	25 25	ns	
t _{PLH} t _{PHL}	Propagation Delay, P to $\overline{P} > \overline{Q}$		20 15	30 30	ns	
t _{PLH} t _{PHL}	Propagation Delay, Q to $\overline{P} > \overline{Q}$		21 19	30 30	ns	

SN74LS684

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _{PLH} t _{PHL}	Propagation Delay, P to $\overline{P} = \overline{Q}$		15 17	25 25	ns	V _{CC} = 5.0 V C _L = 45 pF R _L = 667 Ω
t _{PLH} t _{PHL}	Propagation Delay, Q to $\overline{P} = \overline{Q}$		16 15	25 25	ns	
t _{PLH} t _{PHL}	Propagation Delay, P to $\overline{P} > \overline{Q}$		22 17	30 30	ns	
t _{PLH} t _{PHL}	Propagation Delay, Q to $\overline{P} > \overline{Q}$		24 20	30 30	ns	

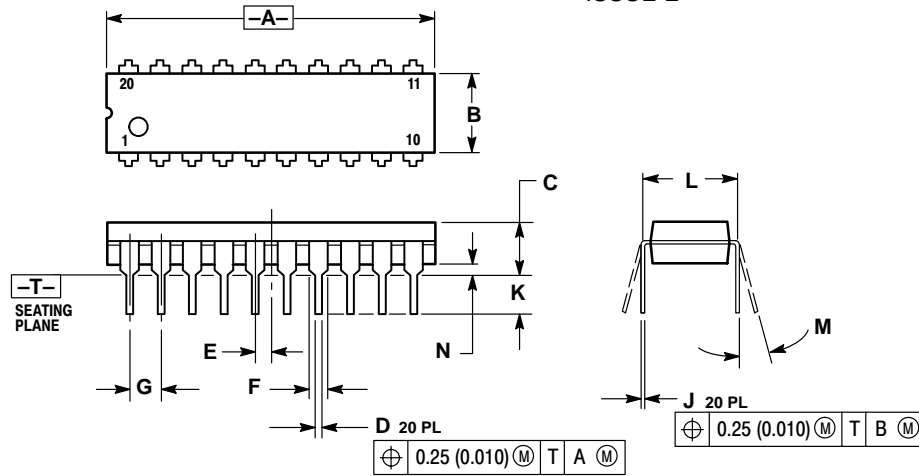
SN74LS688

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _{PLH} t _{PHL}	Propagation Delay, P to $\overline{P} = \overline{Q}$		12 17	18 23	ns	V _{CC} = 5.0 V C _L = 45 pF R _L = 667 Ω
t _{PLH} t _{PHL}	Propagation Delay, Q to $\overline{P} = \overline{Q}$		12 17	18 23	ns	
t _{PLH} t _{PHL}	Propagation Delay, \overline{G} , $\overline{G1}$ to $\overline{P} = \overline{Q}$		12 13	18 20	ns	

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PACKAGE DIMENSIONS

N SUFFIX
PLASTIC PACKAGE
CASE 738-03
ISSUE E



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
J	0.110	0.140	2.80	3.55
K	0.300 BSC		7.62 BSC	
L	0°	15°	0°	15°
M	0.020	0.040	0.51	1.01

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