TOSHIBA Insulated Gate Bipolar Transistor Silicon N Channel IGBT

GT10G131

Strobe Flash Applications

- Supplied in compact and thin package requires only a small mounting area
- 5th generation (trench gate structure) IGBT
- Enhancement-mode
- 4-V gate drive voltage: VGE = 4.0 V (min) (@IC = 200 A)
- Peak collector current: IC = 200 A (max)
- Built-in zener diode between gate and emitter
- SOP-8 package

Absolute Maximum Ratings (Ta = 25°C)

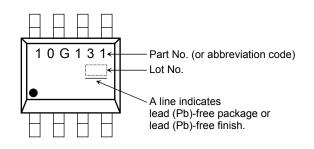
Characteristics		Symbol	Rating	Unit	
Collector-emitter voltage	V_{CES}	400	V		
Gate-emitter voltage	DC	$V_{\sf GES}$	± 6	٧	
	Pulse	V_{GES}	± 8		
Collector current	Pulse (Note 1)	I _{CP}	200	Α	
Collector power	(Note 2a)	P _C (1)	1.9	W	
dissipation(t=10 s)	(Note 2b)	P _C (2)	1.0	W	
Junction temperature		Tj	150	°C	
Storage temperature range		T _{stg}	−55 ~ 150	°C	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

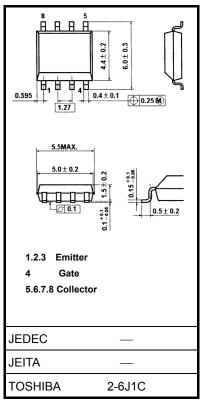
Thermal Characteristics

Characteristics	Symbol	Rating	Unit	
Thermal resistance , junction to ambient (t = 10 s) (Note2a)	R _{th (j-a)} (1)	65.8	°C/W	
Thermal resistance , junction to ambient (t = 10 s) (Note2b)	R _{th (j-a)} (2)	125	°C/W	

Marking (Note 3)

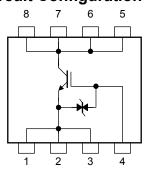


Unit: mm



Weight: 0.08 g (typ.)

Circuit Configuration



Note: For (Note 1), (Note 2a), (Note 2b) and (Note 3), Please refer to the next page.

Electrical Characteristics (Ta = 25°C)

Chara	cteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage current		I _{GES}	$V_{GE} = \pm 6 \text{ V}, V_{CE} = 0$	_	_	± 10	μΑ
Collector cut-off c	urrent	I _{CES}	V _{CE} = 400 V, V _{GE} = 0	_	_	10	μΑ
Gate-emitter cut-o	off voltage	V _{GE} (OFF)	I _C = 1 mA, V _{CE} = 5 V	0.6	0.9	1.2	V
Collector-emitter	saturation voltage	V _{CE (sat)}	I _C = 200 A, V _{GE} = 4 V		2.3	_	V
Input capacitance		C _{ies}	V _{CE} = 10 V, V _{GE} = 0, f = 1 MHz		2800	_	pF
Switching time	Rise time	t _r	$\begin{array}{c} 4 \ V \\ 0 \\ \hline \\ V_{\text{IN}} : \ t_r \leq 100 \ \text{ns} \\ t_f \leq 100 \ \text{ns} \\ \hline \\ \text{Duty cycle} \leq 1\% \\ \end{array} \begin{array}{c} 51 \ \Omega \\ \hline \\$		2.8	_	μ\$
	Turn-on time	t _{on}		_	3.1	_	
	Fall time	t _f			1.8	_	
	Turn-off time	t _{off}		_	2.0	_	

Note

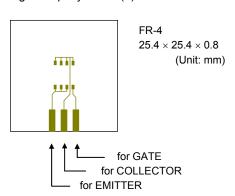
Note 1: Please use devices on condition that the junction temperature is below 150°C. Repetitive rating: pulse width limited by maximum junction temperature.

Note 2a : Device mounted on a glass-epoxy board (a)

FR-4
25.4 × 25.4 × 0.8
(Unit: mm)

for COLLECTOR
for EMITTER
for GATE

Note 2b : Device mounted on a glass-epoxy board (b)



Note 3: O on lower right of the marking indicates Pin 1.

Weekly code: (Three digits)
 Week of manufacture
 (01 for first week of year, continues up to 52 or 53)
 Year of manufacture
 (One low-order digits of calendar year)

Pb-Free Finish (Only a coating lead terminal):
 It is marking about an underline to a week of manufacture mark.



Caution on handling

This device is MOS gate type. Therefore, please care of a protection from ESD in your handling.

Caution in design

You should be design dV/dt value is below 400 V/ μs when IGBT turn off.

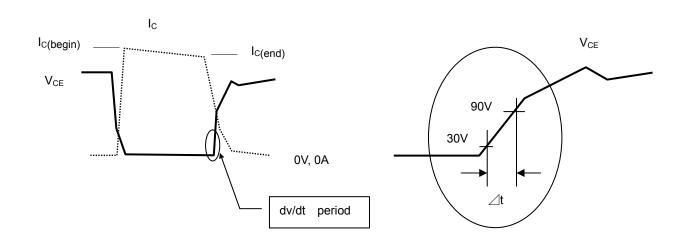
definition of dv/dt

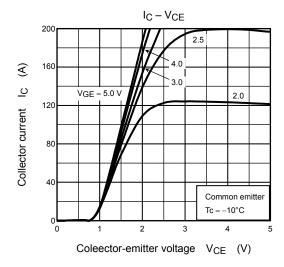
The slope of vce from 30v to 90v (attached figure.1)

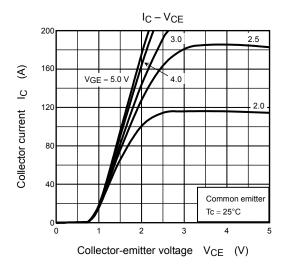
$$dv/dt = (90V-30V) / (\triangle t)$$
$$= 60V / \triangle t$$

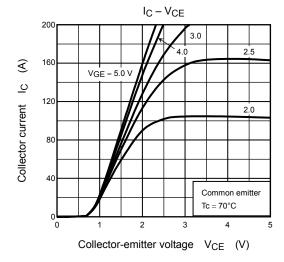
waveform

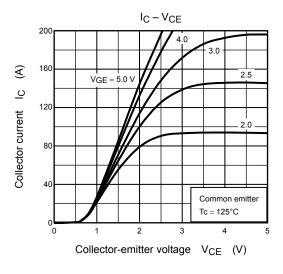
•waveform (expansion)

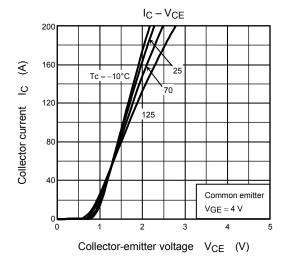


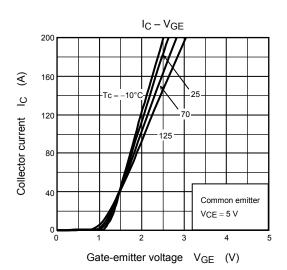


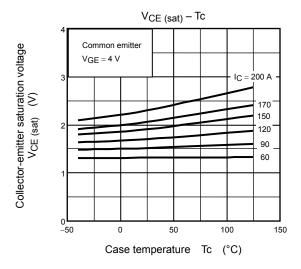


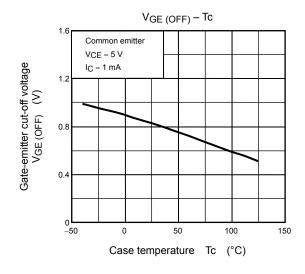


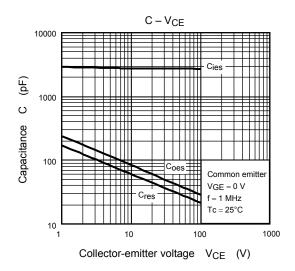


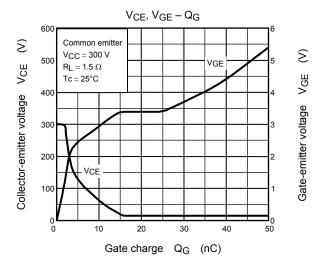


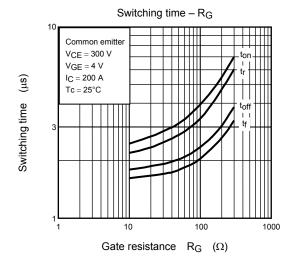


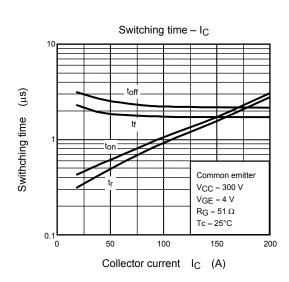




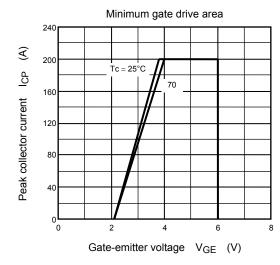


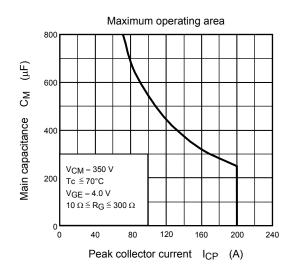






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