

TOSHIBA Bipolar Linear IC Silicon Monolithic

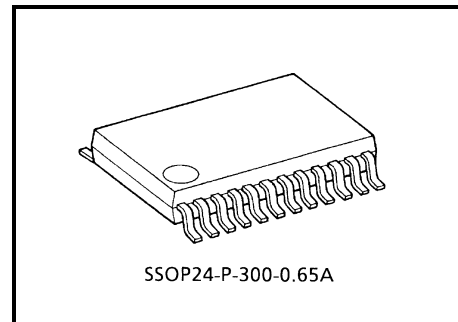
# TA2131FNG

Low Current Consumption Headphone Amplifier for Portable MD Player (With Bass Boost Function)

The TA2131FNG is a low current consumption headphone amplifier developed for portable digital audio. It is particularly well suited to portable MD players that are driven by a single dry cell. It also features a built-in bass boost function with AGC, and is capable of bass amplification of DAC output and analog signals such as tuner.

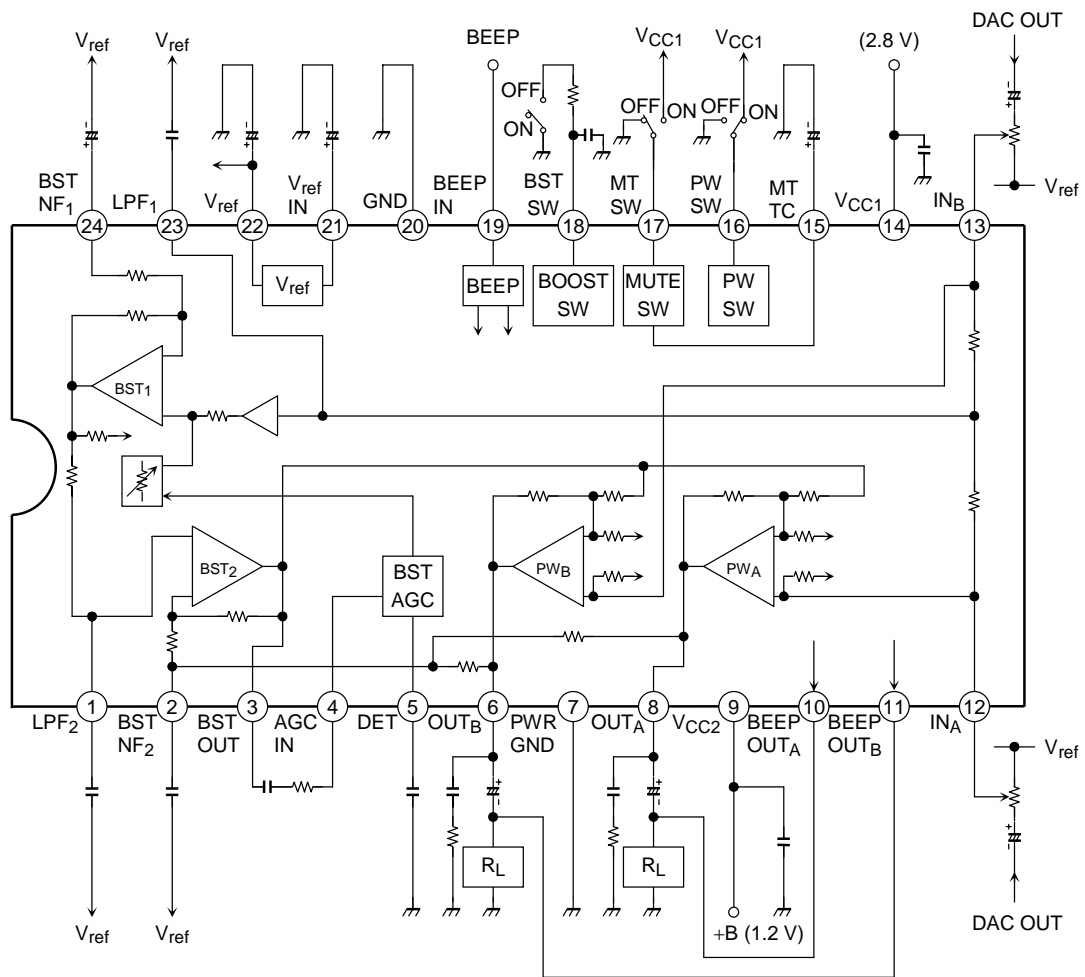
## Features

- Low current consumption:  $ICCQ(VCC1) = 0.55\text{ mA (typ.)}$   
 $ICCQ(VCC2) = 0.20\text{ mA (typ.)}$
- Output power:  $P_o = 8\text{ mW (typ.)}$   
( $VCC1 = 2.8\text{ V}$ ,  $VCC2 = 1.2\text{ V}$ ,  $f = 1\text{ kHz}$ ,  $THD = 10\%$ ,  $R_L = 16\ \Omega$ )
- Low noise:  $V_{no} = -102\text{ dBV (typ.)}$
- Built-in low-pass boost (with AGC)
- I/O pin for beep sound
- Outstanding ripple rejection ratio
- Built-in power mute
- Built-in power ON/OFF switch
- Operating supply voltage range ( $T_a = 25^\circ\text{C}$ ):  $VCC1 = 1.8\sim 4.5\text{ V}$   
 $VCC2 = 0.9\sim 4.5\text{ V}$



Weight: 0.14 g (typ.)

## Block Diagram



## Terminal Explanation (Terminal voltage: Typical terminal voltage at no signal with test circuit, $V_{CC1} = 2.8\text{ V}$ , $V_{CC2} = 1.2\text{ V}$ , $T_a = 25^\circ\text{C}$ )

Terminal No.		Terminal Explanation	Internal Circuit	Terminal Voltage (V)
1	LPF <sub>2</sub>	BST amplifier 1 output (filter terminal)	<p>Internal circuit diagram for the first section of the chip. It shows an ADD amplifier, an AGC (Automatic Gain Control) block, and two BST (Baseband Tuning) amplifiers, BST1 and BST2. BST1 is connected to terminal 12 (PWA) and terminal 23 (PWB). BST2 is connected to terminal 24 and terminal 1. Various resistors are shown: 20 kΩ, 10 kΩ, 30 kΩ, and 2 kΩ. Reference voltages V<sub>ref</sub> are indicated at terminals 24 and 1.</p>	0.61
23	LPF <sub>1</sub>	ADD amplifier output (filter terminal)		0.61
24	BST NF <sub>1</sub>	BST amplifier 1 NF		0.61
2	BST NF <sub>2</sub>	BST amplifier 2 NF terminal (low-pass compensation condenser connection terminal)	<p>Internal circuit diagram for the second section of the chip. It shows a PWA (Power Amplifier) and a PWB (Power Amplifier) block. The circuit includes an ADD amplifier, BST1, and BST2. Various resistors are shown: 20 kΩ, 10 kΩ, 15 kΩ, and 10 kΩ. The diagram shows connections to terminals 12, 13, 8, 3, 6, and 2.</p>	0.61
3	BST OUT	BST amplifier 2 output terminal		0.61
6	OUT <sub>B</sub>	Power amplifier output		0.61
8	OUT <sub>A</sub>			0.61
12	IN <sub>A</sub>	Power amplifier input		0.61
13	IN <sub>B</sub>		0.61	

Terminal No.		Terminal Explanation	Internal Circuit	Terminal Voltage (V)
4	AGC IN	Signal input level to BST amplifier is varied according to the input level to the boost AGC input terminal. Input impedance: 15 k $\Omega$ (typ.)		0.61
5	DET	Smoothing of boost AGC level detection		—
7	PWR GND	GND of power amplifier output stage	—	0
9	VCC2	VCC (+B) at power amplifier output stage	—	1.2
10	BEEP OUT <sub>A</sub>	Beep sound output terminal		—
11	BEEP OUT <sub>B</sub>			—
19	BEEP IN	Beep sound input terminal Receives beep sound signals from microcomputer.		0
14	VCC1	Main VCC	—	2.8
15	MT TC	Mute smoothing Power mute switch Reduces the shock noise during switching		1.2

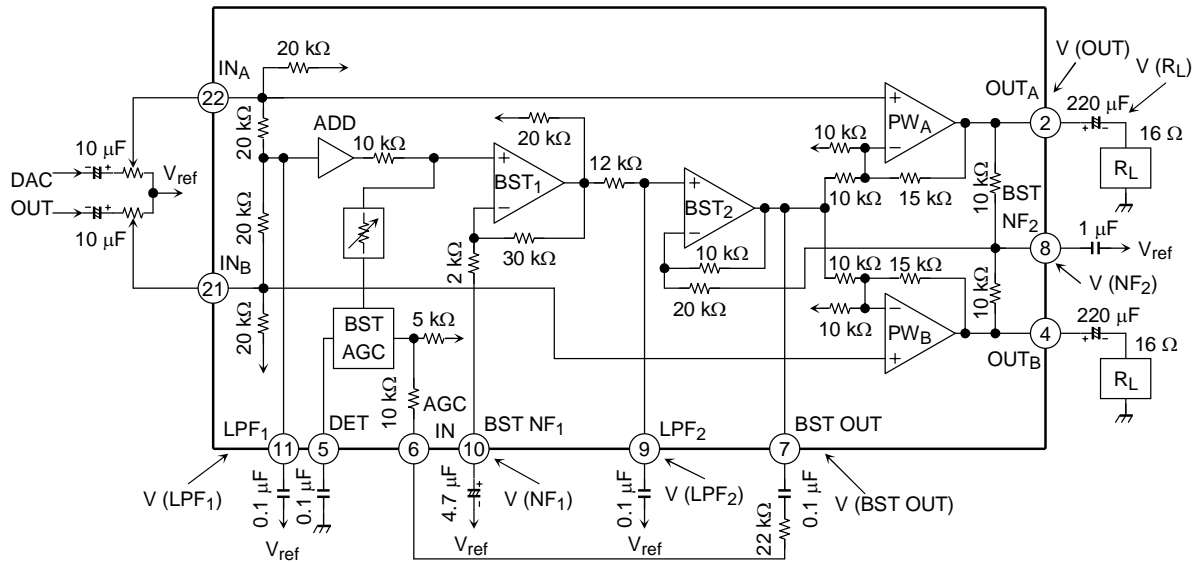
Terminal No.		Terminal Explanation	Internal Circuit	Terminal Voltage (V)
16	PW SW	Power ON/OFF switch "H" level: IC operation "L" level: IC OFF Refer to function explanation 5		—
17	MT SW	Mute switch "L" level: mute reset "H" level: mute ON Refer to function explanation 5		—
18	BST SW	Bass boost ON/OFF switch "H" level/OPEN: BST ON "L" level: BST OFF Refer to function explanation 5		—
20	GND	GND of input stage in power amplifier	—	0
21	V <sub>ref</sub> IN	Reference voltage circuit filter terminal		0.61
22	V <sub>ref</sub>	Reference voltage circuit		0.61

## Function Explanation

### 1. Bass Boost Function

#### 1-1 Description of Operation

TA2131FNG has a bass boost function for bass sound reproduction built-in to the power amplifier. With the bass boost function, at medium levels and lower, channel A and channel B are added for the low frequency component, and output to BST amplifier 2 (BST<sub>2</sub>) in negative phase. That signal is inverted and added before being subjected to bass boost. If the signal of the low-frequency component reaches a high level, the boost gain is controlled to main a low distortion (see Fig.1).



**Figure 1 System Diagram of Bass Boost**

#### 1-2 AGC Circuit

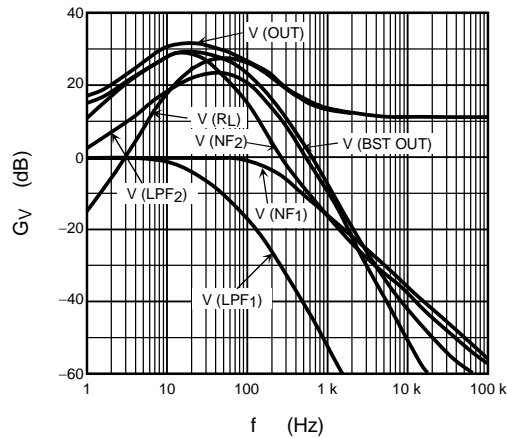
The AGC circuit of the bass boost function detects with “AGC DET” the voltage component created by “BST<sub>2</sub>,” and as the input level increases, the variable impedance circuit is changed, and the bass boost signal is controlled so that it is not assigned to BST amplifier 1. In this way, the bass signal to “BST<sub>2</sub>” input is shut-off, and that boost gain is controlled.

#### 1-3 Bass Boost System

As shown in Fig.1, the flow of the bass boost signal is that the signal received from power amplifier input goes through LPF<sub>1</sub>, ADD amplifier, ATT (variable impedance circuit), BPF<sub>1</sub> (BST amplifier 1) and LPF<sub>2</sub>, and the negative phase signal to the power amplifier input signal is output from BST amplifier 2. The reason why it becomes the negative phase of the BST amplifier 2 signal is that the phase is inverted by 180° in the audible bandwidth by the secondary characteristics of LPF<sub>1</sub> and LPF<sub>2</sub> in Fig.1.

Ultimately the main signal and the bass boost signal formed before BST<sub>2</sub> are added.

Fig.2 shows the frequency characteristics to each terminal.



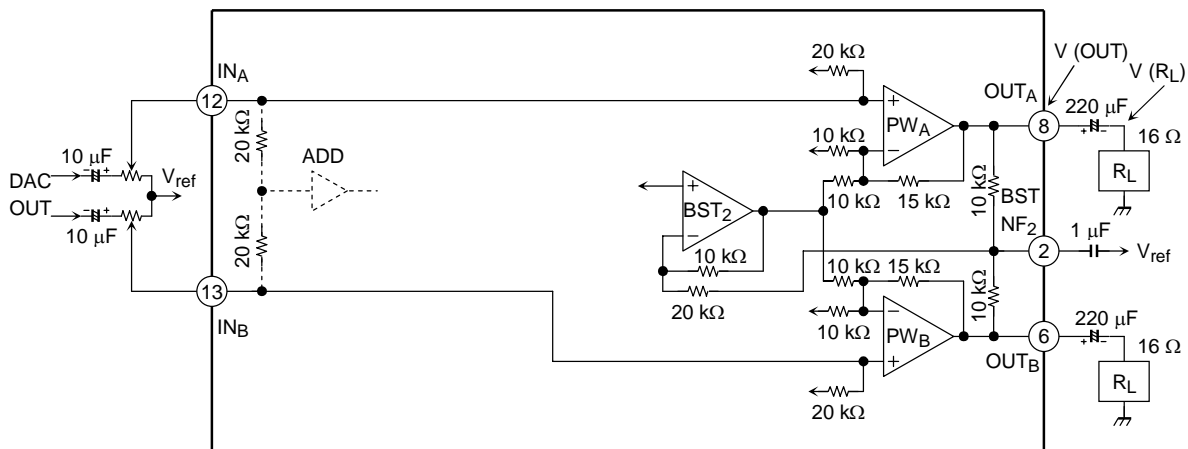
**Figure 2 During Bass Boost (Frequency Characteristics to Each Terminal)**

## 2. Low-Pass Compensation

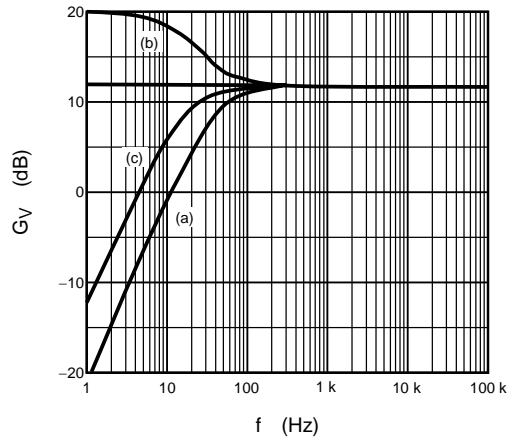
### 2-1. Function

In C-couple type power amplifiers, it is necessary to give the output condenser  $C$  a large capacity to flatten out the frequency characteristics to the low frequency band (this is because the loss in the low frequency bandwidth becomes larger due to the effect of the high-pass filter comprising  $C$  and  $R_L$ ). Particularly when the headphone load is approximately  $16\ \Omega$  and an attempt is being made to achieve frequency characteristics of  $\pm 3\ \text{dB}$  at  $20\ \text{Hz}$ , a large capacity condenser of  $C = 470\ \mu\text{F}$  is required. Bearing this situation in mind, a low-pass compensation function was built in to the TA2131FNG, and while reducing the capacity of the output coupling condenser, almost flat ( $\pm 3\ \text{dB}$ ) frequency characteristics in all audible bandwidths ( $20\ \text{Hz}$  to  $20\ \text{kHz}$ ) have been achieved.

Fig.3 shows the low-pass system diagram, and Fig.4 shows the frequency characteristics at each point. In Fig.4, (a) represents the status lost by the low-pass as a result of the high-pass filter comprising the headphone load ( $R_L = 16\ \Omega$ ) and the output coupling condenser ( $220\ \mu\text{F}$ ) in the C-coupling system.



**Figure 3 Low-Pass Compensation System Diagram**



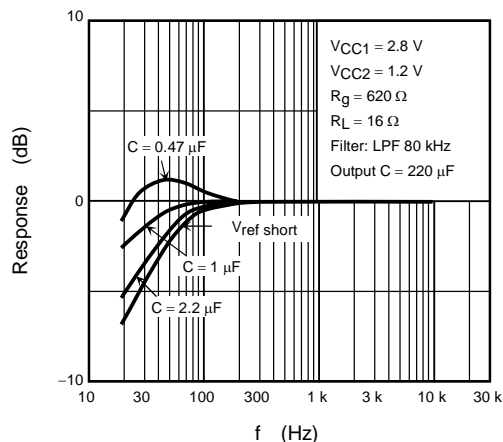
**Figure 4 Power Amplifier Frequency Characteristics**

<Principle of Low-Pass Compensation>

The low-pass component alone is extracted from the composite signal of PWA/PWB output, and that frequency signal is fed back to PWA/PWB once more via the inversion amplifier, thereby making it possible to increase the gain only of the low-pass component. The frequency characteristics of the power amplifier output V (OUT) in this state are shown in Fig.4 (b). In practice they are the frequency characteristics (c) viewed from load terminal V (RL), and the low-pass is compensated relative to the state in (a).

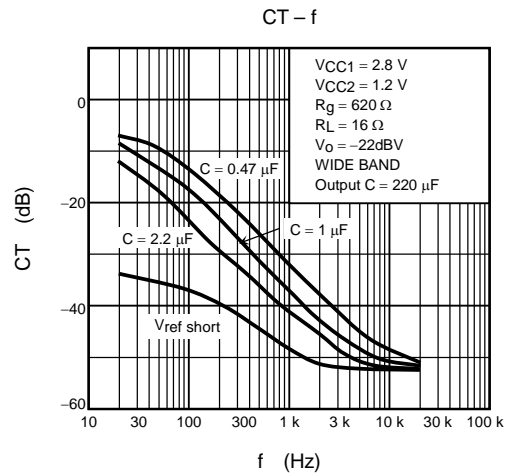
## 2-2. Low-Pass Compensation Condenser and Crosstalk

In this low-pass compensation condenser circuit, processing is carried out using the composite signal of power amplifier output, so this affects crosstalk, according to the amount of compensation. f characteristics and crosstalk generated by the capacity of the condenser for compensation (2-pin) are shown below.



**Figure 5 Condenser and f Characteristics for Low-Pass Compensation**



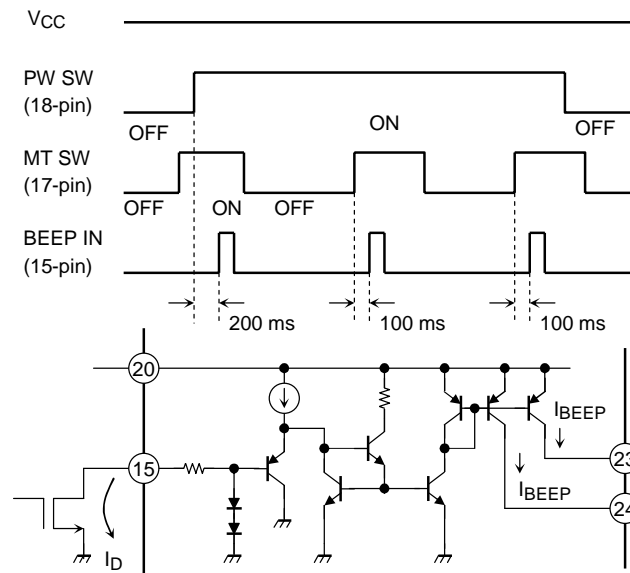


**Figure 6 Low-Pass Compensation Condenser and Crosstalk**

### 3. Beep

Beep sound signals from microcomputer can be received by the beep input terminal (19-pin). The  $PW_A$  and  $PW_B$  of the power amplifier during power mute are turned OFF, and the beep signal input from BEEP-IN (19-pin) is output from the BEEP-OUT terminal (10/11-pin) as fixed current, after passing through the converter and current amplification stage. Connecting this terminal to the headphone load outputs the beep sound.

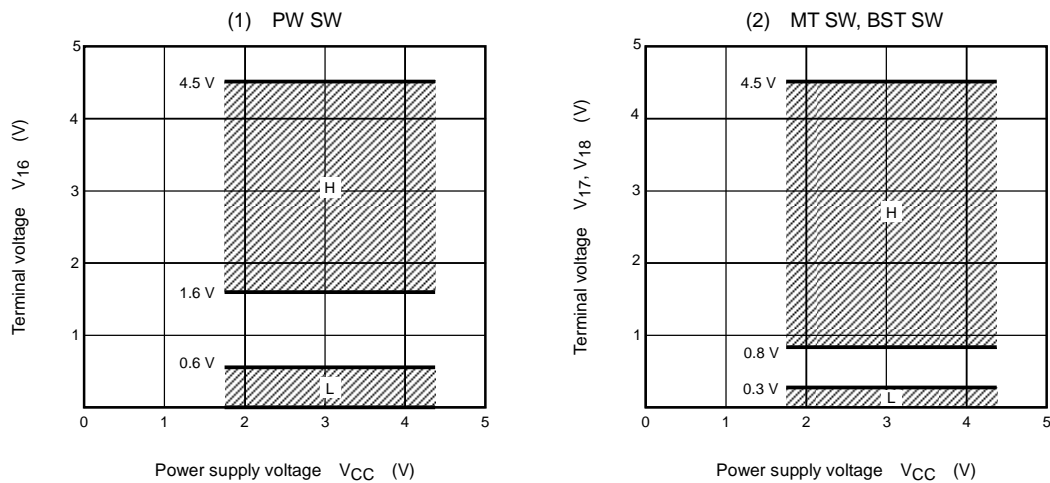
If the beep sound is not input, fix the BEEP-IN (19-pin) terminal to GND level.



#### 4. Power Switch

As long as the power switch is not connected to “H” level, the IC does not operate. If it malfunctions due to external noise, however, it is recommended to connect a pull-down resistor externally (the power switch is set to be highly sensitive).

#### 5. Threshold Voltages of Switches



	PW SW ( $V_{16}$ )
“H” level	IC operation
“L” level	IC OFF

	MT SW ( $V_{17}$ )
“H” level	Mute ON
“L” level	Mute reset

	BST SW ( $V_{18}$ )
“H” level/OPEN	BST ON
“L” level	BST OFF

- These capacitors which prevent oscillation of the power amplifier, and are between the  $V_{ref}$  and  $V_{CC}$ -GND must have a small temperature coefficient and outstanding frequency characteristics.

## Absolute Maximum Ratings

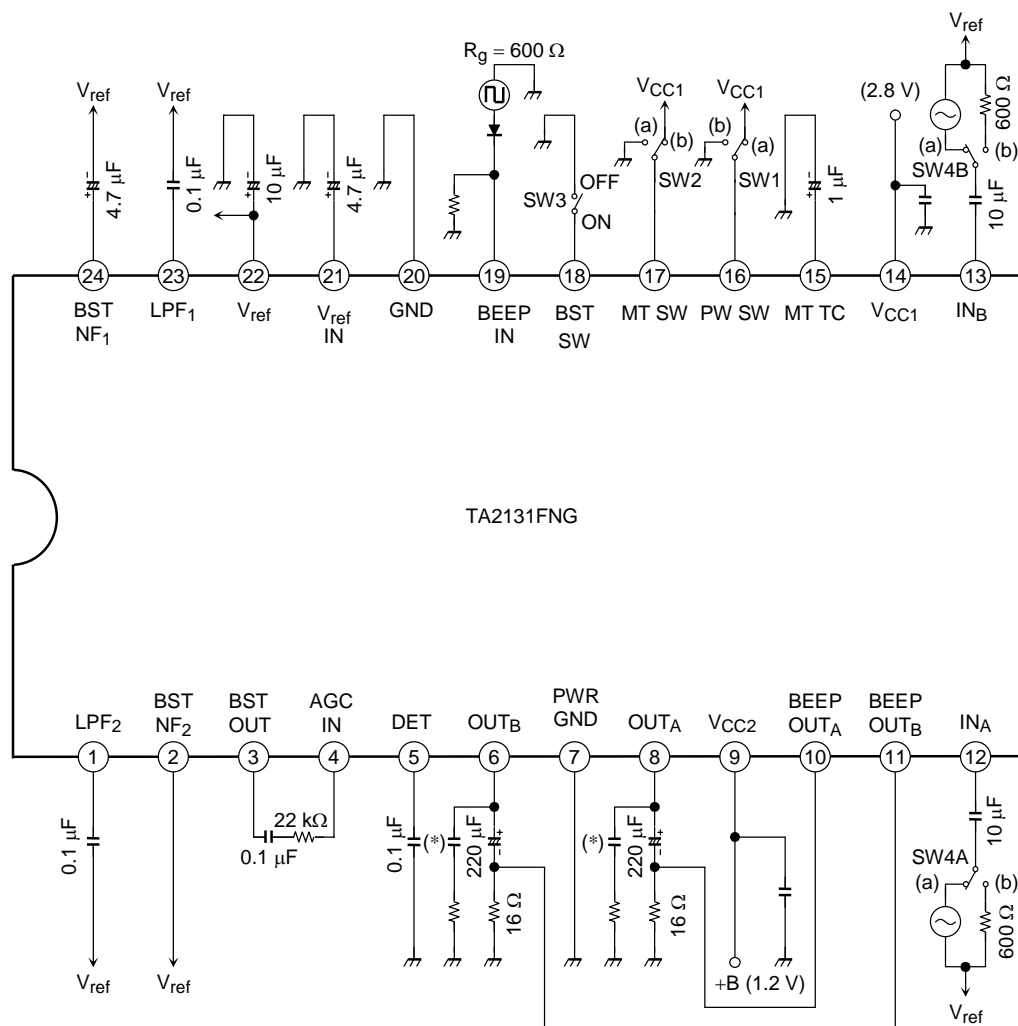
Characteristic	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	4.5	V
Output current	$I_o$ (peak)	100	mA
Power dissipation	$P_D$ (Note)	500	mW
Operating temperature	$T_{opr}$	-25~75	°C
Storage temperature	$T_{stg}$	-55~150	°C

Note: Derated above  $T_a = 25^\circ\text{C}$  in the proportion of 4 mW/°C.

**Electrical Characteristics (Unless specified otherwise,  $V_{CC1} = 2.8\text{ V}$ ,  $V_{CC2} = 1.2\text{ V}$ ,  $R_g = 600\ \Omega$ ,  $R_L = 16\ \Omega$ ,  $f = 1\text{ kHz}$ ,  $T_a = 25^\circ\text{C}$ )**

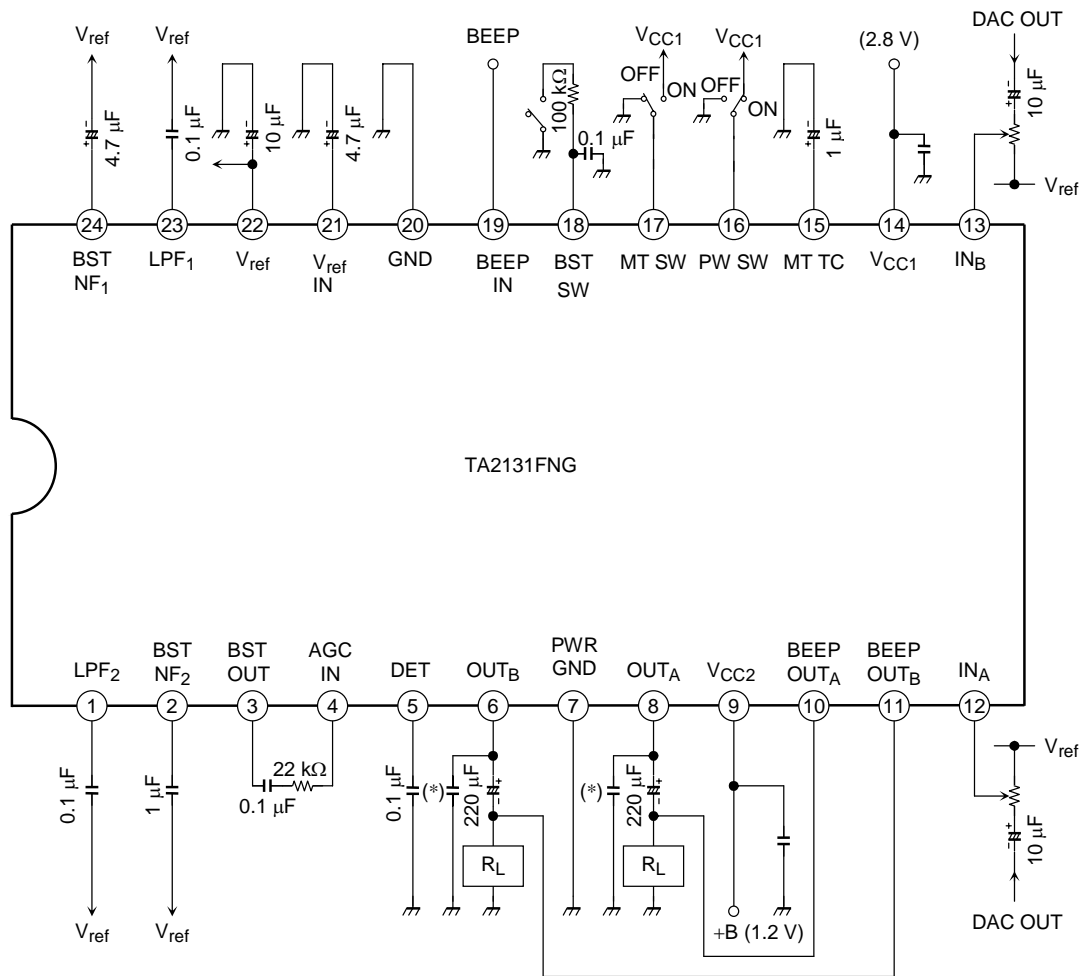
Characteristic		Symbol	Test condition	Min	Typ.	Max	Unit
Quiescent supply current		$I_{CC1}$	IC OFF ( $V_{CC1}$ ), SW1: b, SW2: b	—	0.1	5	$\mu\text{A}$
		$I_{CC2}$	IC OFF ( $V_{CC2}$ ), SW1: b, SW2: b	—	0.1	5	
		$I_{CC3}$	MUTE ON ( $V_{CC1}$ ), SW1: a, SW2: b	—	0.35	0.50	mA
		$I_{CC4}$	MUTE ON ( $V_{CC2}$ ), SW1: a, SW2: b	—	5	10	$\mu\text{A}$
		$I_{CC5}$	No signal ( $V_{CC1}$ ), SW1: a, SW2: a	—	0.55	0.75	mA
		$I_{CC6}$	No signal ( $V_{CC2}$ ), SW1: a, SW2: a	—	0.20	0.40	
Power supply current during drive		$I_{CC7}$	$P_o = 0.5\text{ mW} + 0.5\text{ mW output}$ ( $V_{CC1}$ )	—	0.6	—	mA
		$I_{CC8}$	$P_o = 0.5\text{ mW} + 0.5\text{ mW output}$ ( $V_{CC2}$ )	—	5.3	—	
Power Section	Gain	$G_V$	$V_o = -22\text{dBV}$	10	12	14	dB
	Channel balance	CB	$V_o = -22\text{dBV}$	-1.5	0	1.5	
	Output power	$P_{omax}$	THD = 10%	5	8	—	mW
	Total harmonic distortion	THD	$P_o = 1\text{ mW}$	—	0.1	0.3	%
	Output noise voltage	$V_{no}$	$R_g = 600\ \Omega$ , Filter: IHF-A, SW4: b	—	-102	-96	dBV
	Crosstalk	CT	$V_o = -22\text{dBV}$	-42	-48	—	dB
	Ripple rejection ratio	RR1	$f_r = 100\text{ Hz}$ , $V_r = -20\text{dBV}$ inflow to $V_{CC2}$	-71	-77	—	
		RR2	$f_r = 100\text{ Hz}$ , $V_r = -20\text{dBV}$ inflow to $V_{CC1}$	-54	-64	—	
	Mute attenuation	ATT	$V_o = -12\text{dBV}$ , SW2: a $\rightarrow$ b	-90	-100	—	
	Beep sound output voltage	VBEEP	V Beep IN = 2 $V_{p-o}$ , SW2: b	-53	-48	-43	dBV
Boost gain		BST1	$V_o = -20\text{dBV}$ , $f = 100\text{ Hz}$ , SW3: ON $\rightarrow$ OPEN	1	4	7	dB
		BST2	$V_o = -30\text{dBV}$ , $f = 100\text{ Hz}$ , SW3: ON $\rightarrow$ OPEN	10	13	16	
		BST3	$V_o = -50\text{dBV}$ , $f = 100\text{ Hz}$ , SW3: ON $\rightarrow$ OPEN	13.5	16.5	19.5	

## Test Circuit



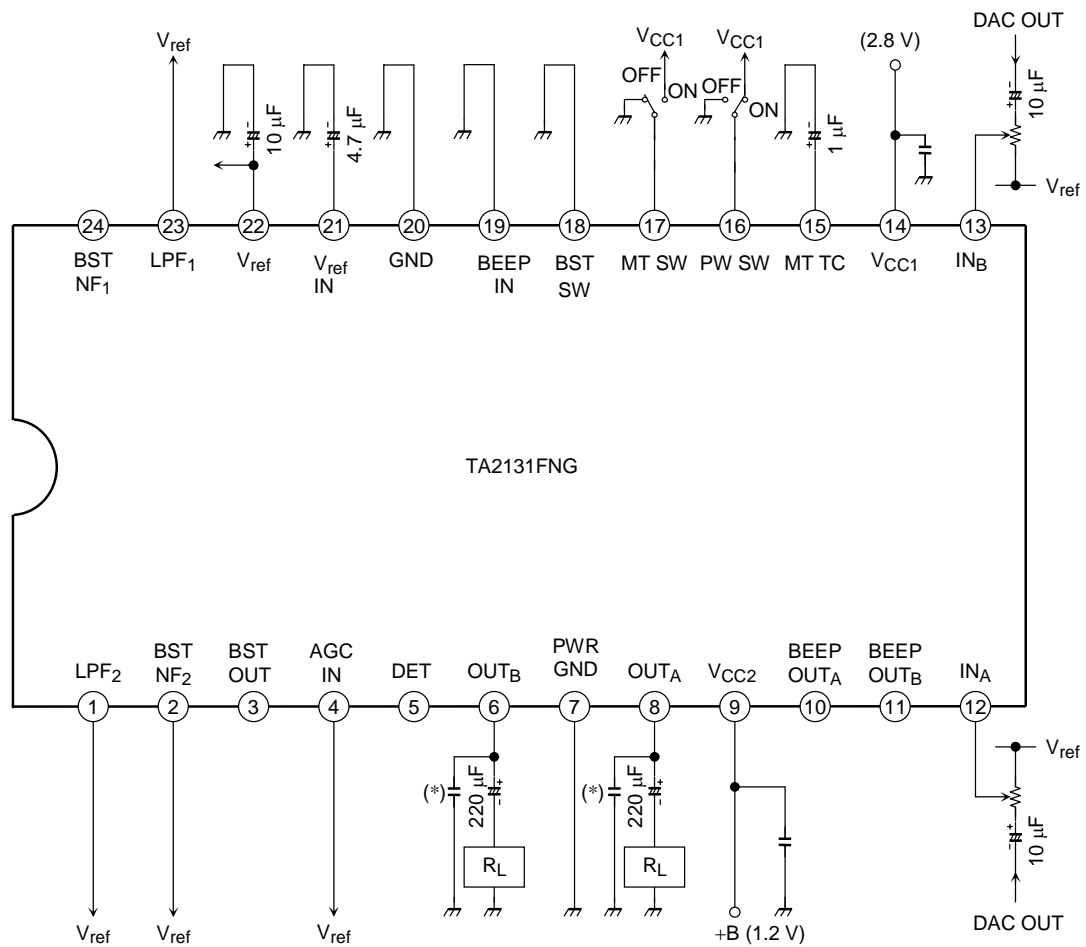
(\*) 0.22 μF + 10 Ω  
Monolithic ceramic capacitor

## Application Circuit 1



(\*) 0.22  $\mu\text{F}$  + 10  $\Omega$   
Monolithic ceramic capacitor

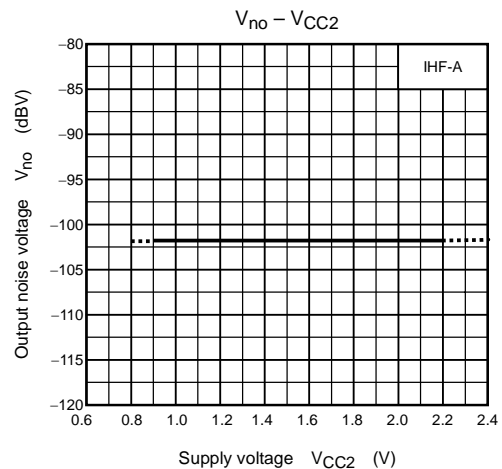
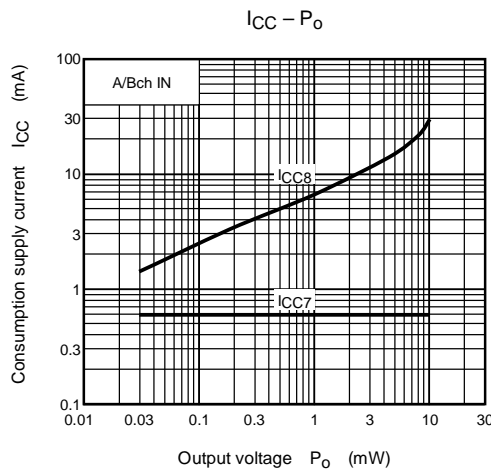
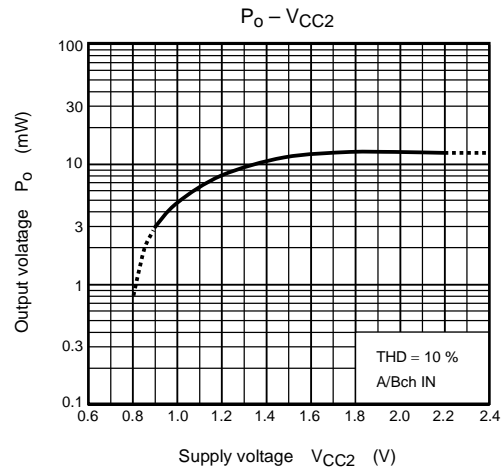
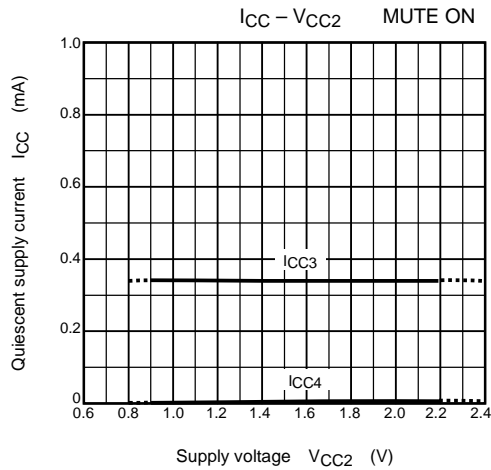
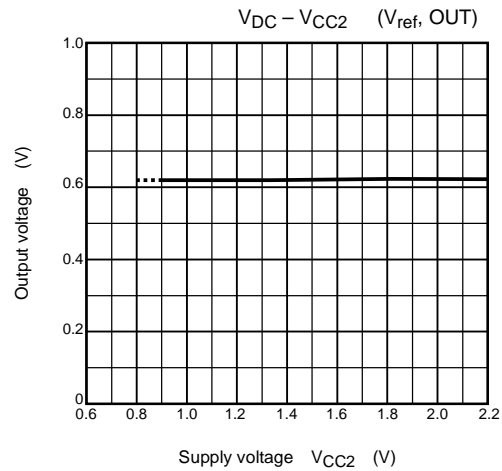
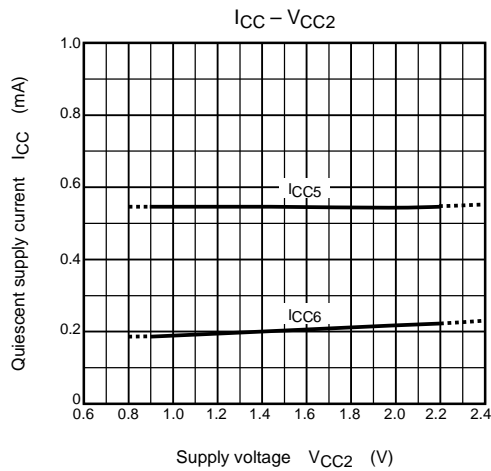
## Application Circuit 2 (Low-Pass Compensation/Bass Boost Function/Beep Not Used)

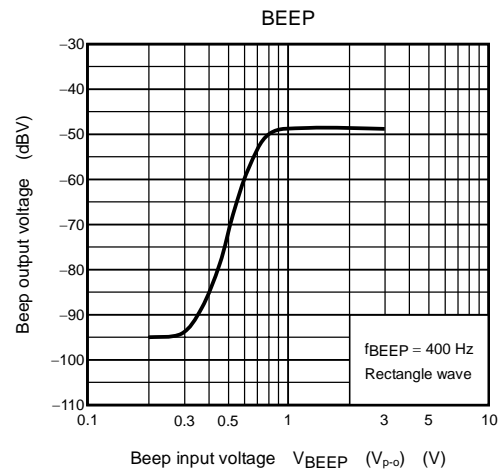
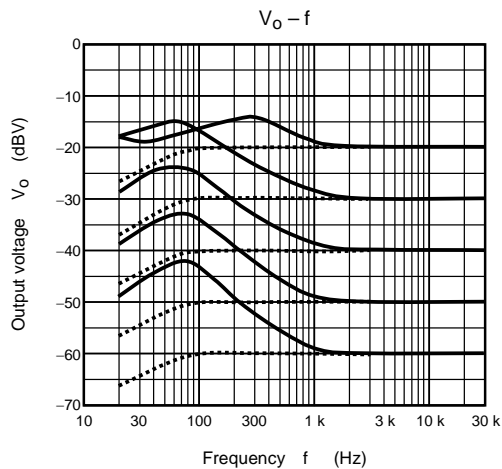
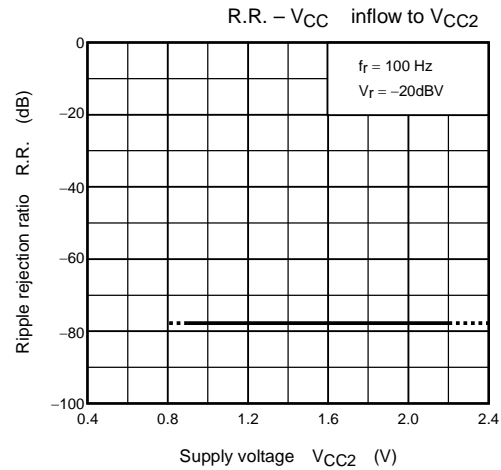
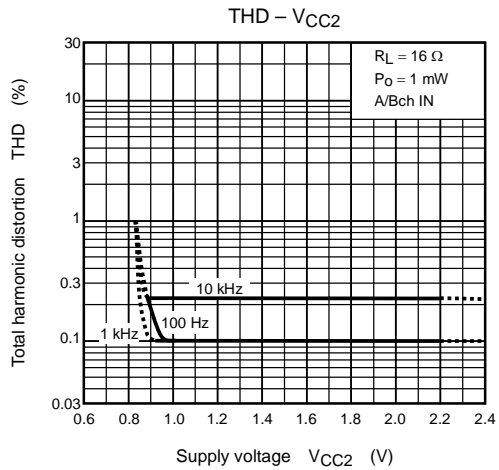
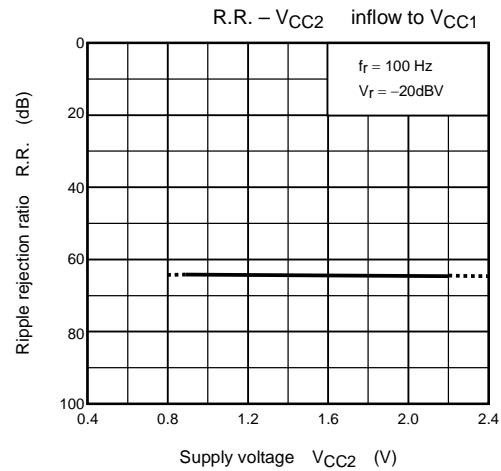
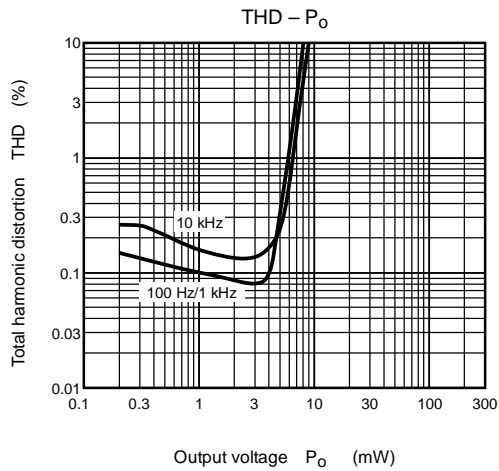


(\*) 0.22 μF + 10 Ω  
Monolithic ceramic capacitor

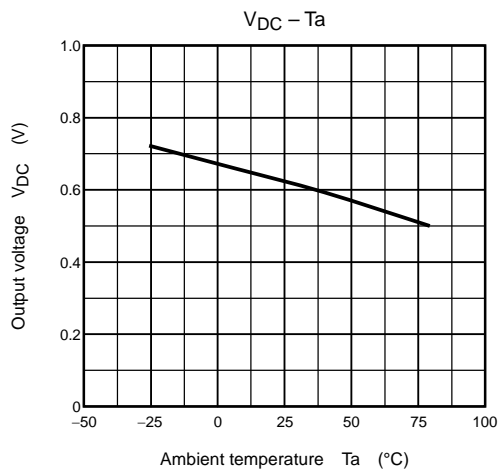
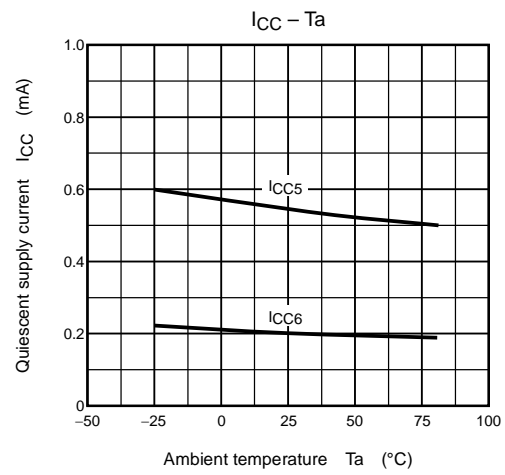
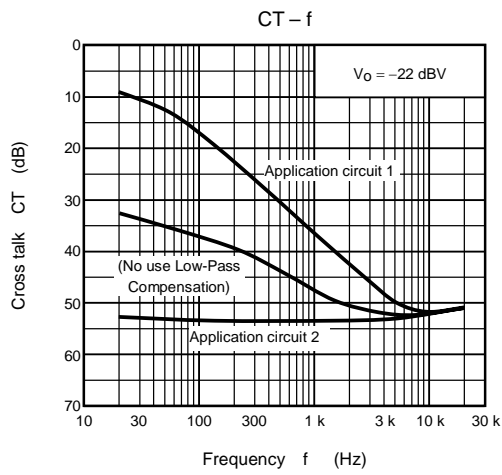
**Characteristics**

(Unless otherwise specified  $V_{CC1} = 2.8 \text{ V}$ ,  $V_{CC2} = 1.2 \text{ V}$ ,  $R_g = 600 \Omega$ ,  $f = 1 \text{ kHz}$ ,  $T_a = 25^\circ\text{C}$ )





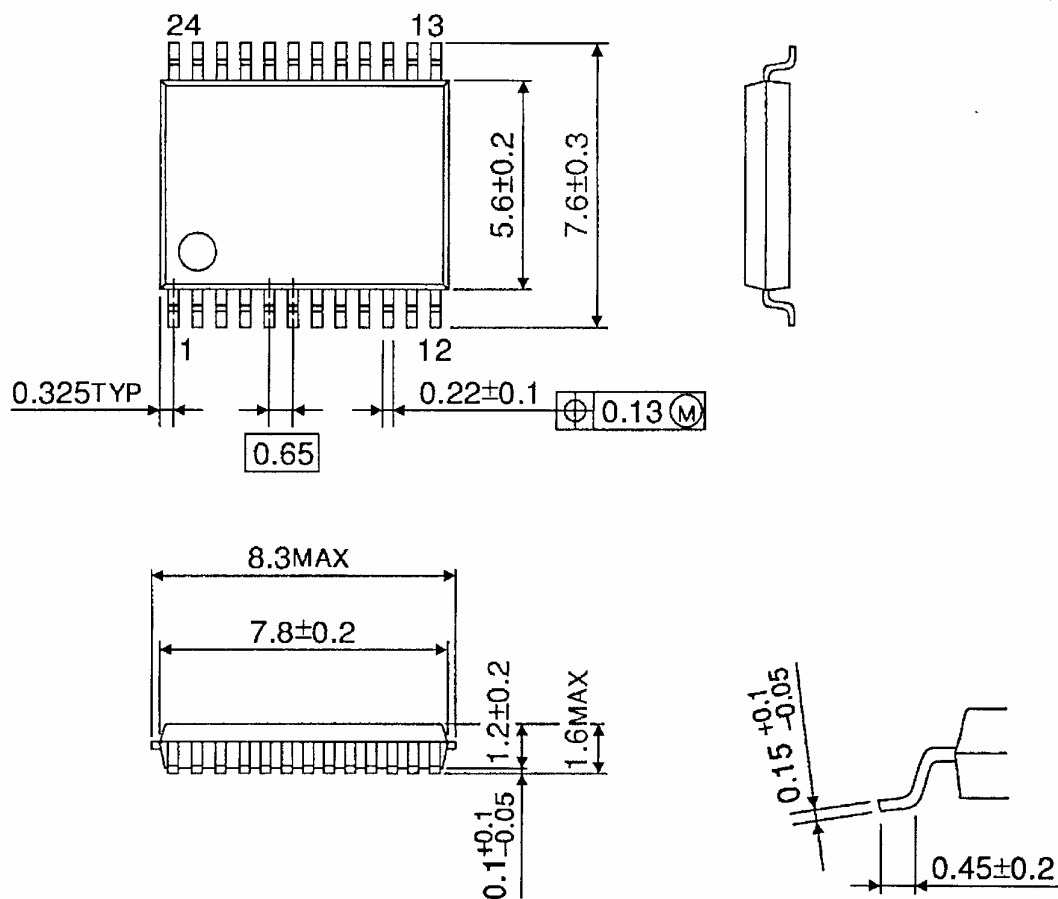




**Package Dimensions**

SSOP24-P-300-0.65A

Unit : mm



Weight: 0.14 g (typ.)

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About solderability, following conditions were confirmed

- Solderability
  - (1) Use of Sn-37Pb solder Bath
    - solder bath temperature = 230°C
    - dipping time = 5 seconds
    - the number of times = once
    - use of R-type flux
  - (2) Use of Sn-3.0Ag-0.5Cu solder Bath
    - solder bath temperature = 245°C
    - dipping time = 5 seconds
    - the number of times = once
    - use of R-type flux