

TB62707FG

8BIT PIPO (Parallel In , Parallel Out) CONSTANT CURRENT DRIVERS

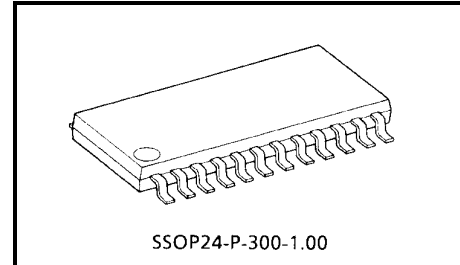
The TB62707FG is specifically designed for LED and LED DISPLAY constant current drivers.

This constant current output is able to set up external resistor ($I_{OUT} = 90 \text{ mA MAX.}$).

This IC is monolithic integrated circuit designed to be used together with Bi-CMOS process.

The devices consist of 8bit latches, AND-GATE and Constant Current Drivers.

The suffix (G) appended to the part number represents a Lead(Pb)-Free product.



Weight: 0.32 g (typ.)

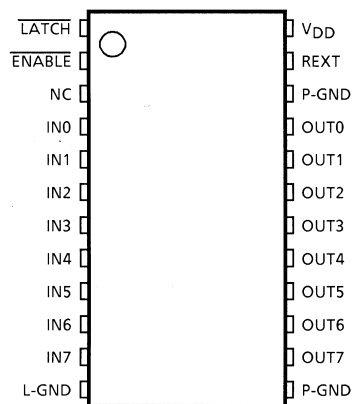
FEATURES

- Constant Current Output:
Can set up all output current with one resistor for 5 to 90mA.
- Constant Output Current Matching:

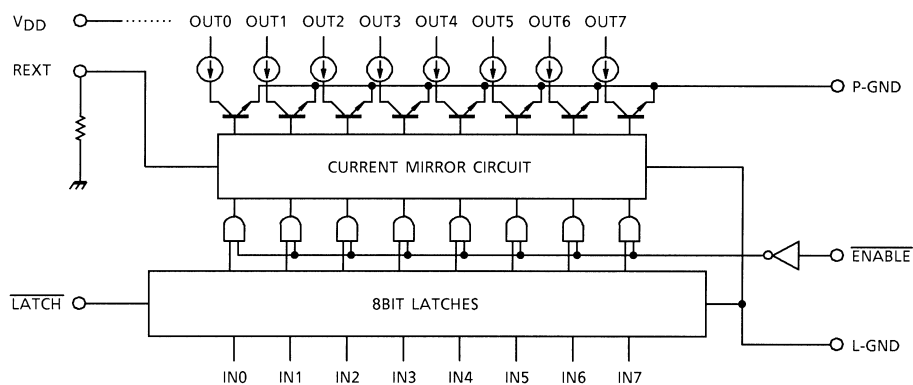
OUTPUT-GND VOLTAGE	CURRENT MATCHING	OUTPUT CURRENT
$\geq 0.4 \text{ [V]}$	$\pm 6.0 \text{ [%]}$	5~40 mA
$\geq 0.7 \text{ [V]}$	$\pm 6.0 \text{ [%]}$	40~90 mA

- 5 V CMOS Compatible Input
- Package: SSOP24-P-300

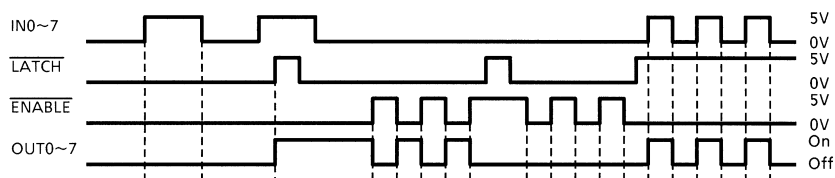
PIN CONNECTION (Top view)



BLOCK DIAGRAM



TIMING DIAGRAM






Note: Latches are level sensitive, not rising edge sensitive and not synchronous CLOCK.
 Input of $\overline{\text{LATCH}}$ -terminal to "H" level, data passes latches, and input to "L" level, data hold latches.
 Input of $\overline{\text{ENABLE}}$ -terminal to "H" level, all output (OUT0~7) do off.

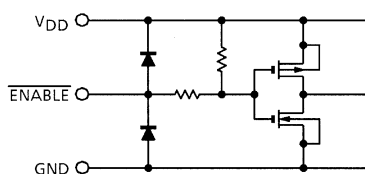
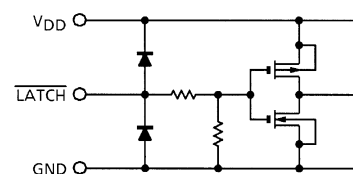
TERMINAL DESCRIPTION

PIN No.	PIN NAME	FUNCTION
1	$\overline{\text{LATCH}}$	Input terminal of a data strobe. Latches passes data with "H" level input of $\overline{\text{LATCH}}$ -terminal, and hold data with "L" level input.
2	$\overline{\text{ENABLE}}$	Input terminal of output enable. All outputs (OUT0~7) do off with "H" level input of $\overline{\text{ENABLE}}$ -terminal, and do on with "L" level input.
4~11	IN0~7	Input terminal of a parallel-data for latches.
3	NC	No connection.
12	L-GND	GND terminal for controll logic.
13	P-GND	GND terminal for output constant current drivers.
14~21	OUT0~7	Output terminals.
22	P-GND	GND terminal for output constant current drivers.
23	REXT	Input terminal of connects with a resister for to set up all output current.
24	V _{DD}	5V Supply voltage terminal

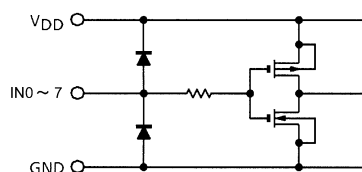
TRUTH TABLE

IN0~7	$\overline{\text{LATCH}}$	$\overline{\text{ENABLE}}$	OUT0~7
L	L	L	OFF
H	L	L	OFF
L	H	L	OFF
H	H	L	ON
L		L	OFF
H		L	ON
H		H	OFF

EQUIVALENT CIRCUIT OF INPUTS

1. $\overline{\text{ENABLE}}$ terminal2. $\overline{\text{LATCH}}$ terminal

3. IN0~7 terminal



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V _{CC}	7.0	V
Input Voltage	V _{IN}	-0.3~V _{DD} + 0.3	V
Output Current	I _O	90.0	mA
Output Voltage	V _O	-0.3~17.0	V
GND Terminal Current	I _{GND}	720	mA
Power Dissipation	P _D	780 (Note)	mW
Operating Temperature	T _{opr}	-40~85	°C
Storage Temperature	T _{stg}	-55~150	°C

Note: On PCB (50 × 50 × 1.6 mm Cu 30% Glass Epoxy PCB)
 Ambient temperature delated above 25°C in the proportion of 6.66 mW / °C

RECOMMENDED OPERATING CONDITION (Ta = -40~85°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Supply Voltage	V _{DD}	—	4.5	5.0	5.5	V
Output Voltage	V _O	—	—	—	15.0	V
Output Current	I _{OUT}	DC 1 circuit	5.0	—	88	mA
	I _{OH}	SERIAL-OUT	—	—	1.0	mA
	I _{OL}	SERIAL-OUT	—	—	-1.0	mA
Input Voltage	V _{IH}	—	0.7 V _{DD}	—	V _{DD} + 0.3	V
	V _{IL}	—	-0.3	—	0.3 V _{DD}	
$\overline{\text{LATCH}}$ Pulse Width	t _w $\overline{\text{LAT}}$	V _{DD} = 4.5 V	100	—	—	ns
	t _w $\overline{\text{LAT}}$		100	—	—	
INPUT Pulse Width	t _w $\overline{\text{IN}}$		4500	—	—	ns
	t _w $\overline{\text{IN}}$		4500	—	—	
$\overline{\text{ENABLE}}$ Pulse Width	t _w $\overline{\text{EN}}$		4500	—	—	ns
	t _w $\overline{\text{EN}}$		4500	—	—	
Set-Up Time for $\overline{\text{LATCH}}$	t _{setup} (L)		100	—	—	ns
Hold Time for $\overline{\text{LATCH}}$	t _{hold} (L)		100	—	—	ns
Power Dissipation	P _D	ON PCB, Ta = 85°C	—	—	0.60	W

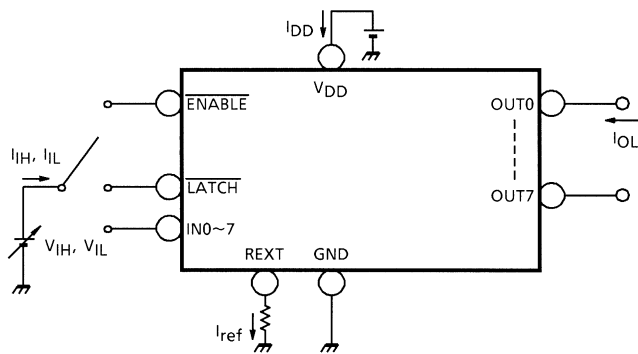
ELECTRICAL CHARACTERISTICS ($V_{DD} = 5.0 \text{ V}$, $T_a = 25^\circ\text{C}$ unless otherwise noted)

CHARACTERISTIC		SYMBOL	TEST CIR- CUIT	TEST CONDITION		MIN	TYP.	MAX	UNIT
Input Voltage	"H" Level	V _{IH}	—	—		0.7 V _{DD}	—	V _{DD}	V
	"L" Level	V _{IL}	—	—		GND	—	0.3 V _{DD}	
Output Leakage Current		I _{OH}	—	V _{OH} = 15.0 V		—	—	10	μA
Output Voltage	SERIAL-OUT	V _{OL}	—	I _{OL} = 1.0 mA		—	—	0.4	V
		V _{OH}	—	I _{OL} = -1.0 mA		4.6	—	—	
Output Current 1		I _{OL1}	—	V _{CE} = 0.7 V	R _{EXT} = 620 Ω (Include skew)	35.7	42.0	48.3	mA
		I _{OL2}	—	V _{CE} = 0.4 V		68.0	80.0	92.0	mA
Current Skew		Δ I _{OL1}	—	I _O = 40 mA, V _{CE} = 0.4 V	R _{EXT} = 620 Ω	—	±1.5	±6.0	%
Output Current 2		I _{OL3}	—	V _{CE} = 1.0 V	R _{EXT} = 330 Ω (Include skew)	64.2	75.5	86.8	mA
		I _{OL4}	—	V _{CE} = 0.7 V		63.8	75.0	86.2	mA
Current Skew		Δ I _{OL2}	—	I _O = 75 mA V _{CE} = 0.7 V	R _{EXT} = 330 Ω	—	±1.5	±6.0	%
Supply Voltage Regulation		% / V _{DD}	—	R _{EXT} = 470 Ω, Ta = -40~85°C		—	+5.0	—	% / V
Reference Voltage		V _{ref}	—	—		—	1.26	—	V
Supply Current "OFF"		I _{DD} (off) 1	—	R _{EXT} = OPEN, OUT0~7 = off V _{DD} = 4.5 V, ENABLE = "H"		—	0.6	1.2	mA
		I _{DD} (off) 2	—	R _{EXT} = 500 Ω, OUT0~7 = off V _{DD} = 4.5V, ENABLE = "H"		6.0	8.0	10.0	
		I _{DD} (off) 3	—	R _{EXT} = 280 Ω, OUT0~7 = off V _{DD} = 4.5V, ENABLE = "H"		12.0	15.0	18.0	
Supply Current "ON"		I _{DD} (on) 1	—	R _{EXT} = 500 Ω, OUT0~7 = on V _{DD} = 4.5 V, ENABLE = "L"		8.0	13.0	20.0	mA
		I _{DD} (on) 2	—	R _{EXT} = 280 Ω, OUT0~7 = on V _{DD} = 4.5 V, ENABLE = "L"		18.0	25.0	35.0	

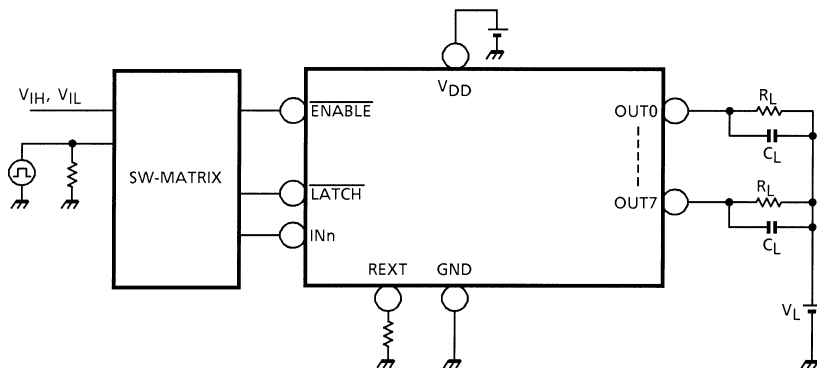
SWITCHING CHARACTERISTICS (Ta = 25°C, unless otherwise noted)

CHARACTERISTIC		SYMBOL	TEST CIR- CUIT	CONDITION	MIN	TYP.	MAX	UNIT
Propagation Delay Time ("L" to "H")	IN-OUTn	t _{pLH}	—	V _{DD} = 5.0 V V _{CE} = 0.4 V V _{IH} = V _{DD} V _{IL} = GND R _{EXT} = 500 Ω I _{OUT} = 40 mA V _L = 3.0 V R _L = 65 Ω C _L = 10.5 pF	—	600	1200	ns
	LATCH -OUTn				—	600	1200	
	ENABLE -OUTn				—	600	1200	
Propagation Delay Time ("H" to "L")	IN-OUTn	t _{pHL}	—		—	300	1200	ns
	LATCH -OUTn				—	300	1200	
	ENABLE -OUTn				—	300	1200	
Pulse Width	IN	t _w IN, $\overline{\text{IN}}$	—		—	2000	3500	ns
	LATCH	t _w LAT, $\overline{\text{LAT}}$	—		—	25	50	
	ENABLE	t _w ENA, $\overline{\text{EN}}$	—		—	2000	3500	
Set-up Time for LATCH & CLOCK	L-H	t _{setup} $\overline{\text{LAT}}$	—		—	25	50	ns
	H-L		—		—	25	50	
Hold Time for LATCH & CLOCK	L-H	t _{hold} $\overline{\text{LAT}}$	—		—	0	30	ns
	H-L		—		—	0	30	
Output Rise Time		t _{or}	—		200	1000	1200	ns
Output Fall Time		t _{of}	—		200	1000	1200	ns

DC CHARACTERISTICS TEST CIRCUIT



AC CHARACTERISTICS TEST CIRCUIT

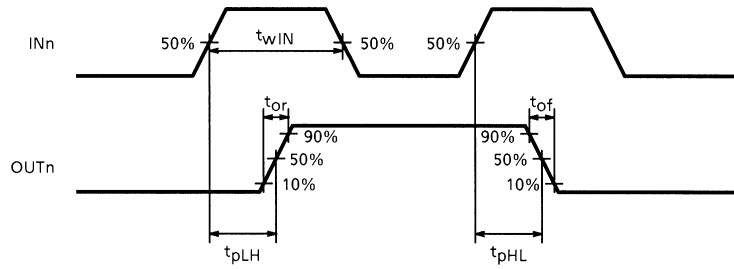


PRECAUTIONS for USING

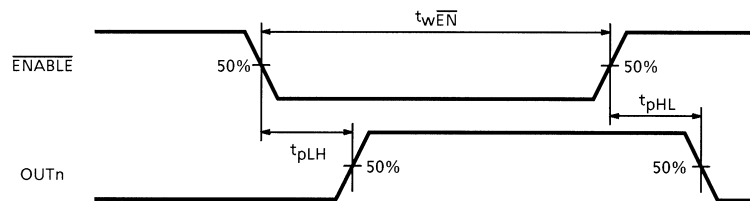
Utmost care is necessary in the design of the output line, VCC (V_{DD}) and GND (L-GND, P-GND) line since IC may be destroyed due to short-circuit between outputs, air contamination fault, or fault by improper grounding.

TIMING WAVEFORM

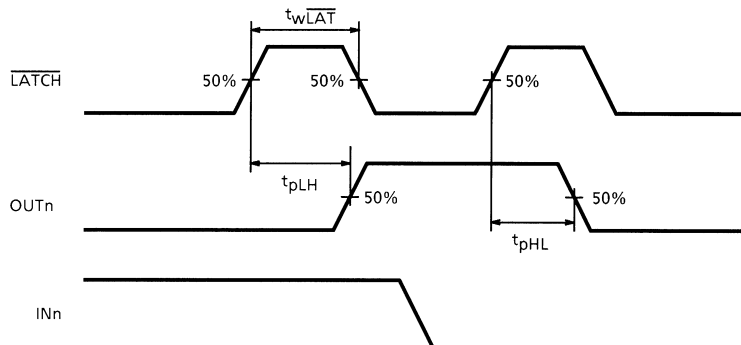
1. IN_n-OUT_n

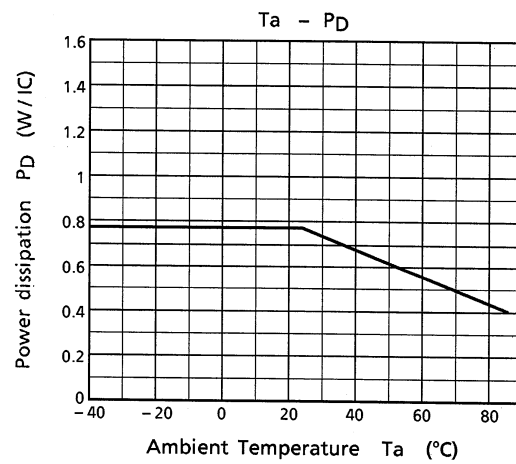
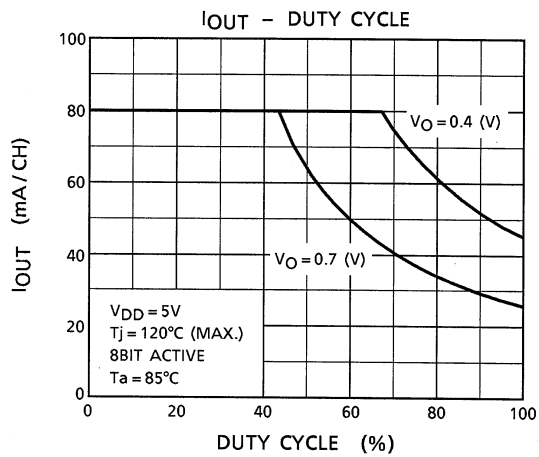
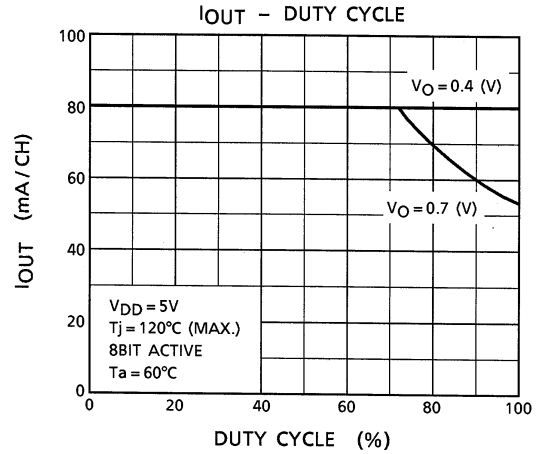
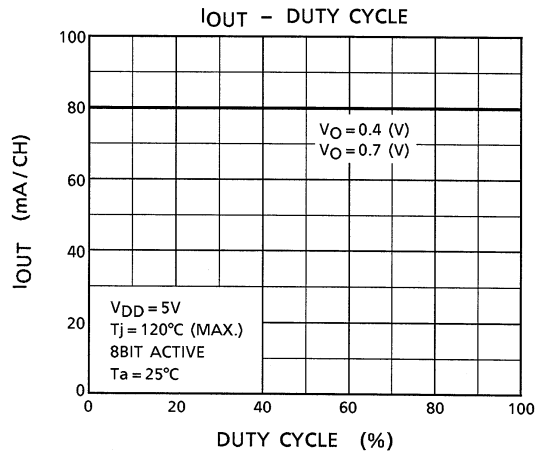


2. $\overline{ENABLE}-OUT_n$

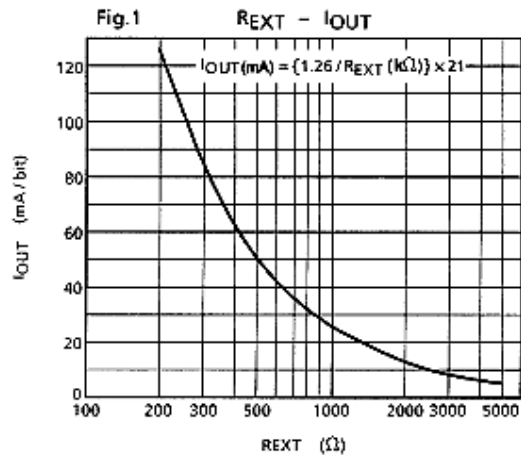


3. $\overline{LATCH}-OUT_n$





LED DRIVER TB6270X SERIES APPLICATION NOTE



[1] Output current (I_{OUT})

I_{OUT} is set by the external resistor (R_{EXT}) as shown in Fig.1.

[2] Total supply voltage (V_{LED})

This device can operate 0.4~0.7V (V_O).

When a higher voltage is input to the divide, the excess voltage is consumed inside the device, that leads to power dissipation.

In order to minimize power dissipation and loss, we would like to recommended to set the total supply voltage as shown below.

V_{LED} (Total supply voltage)

$$= V_{CE} (Tr V_{sat}) + V_f (\text{LED Forward voltage}) + V_O$$

When the total supply is too high considering the power dissipation of this divide, an additional R can decrease the

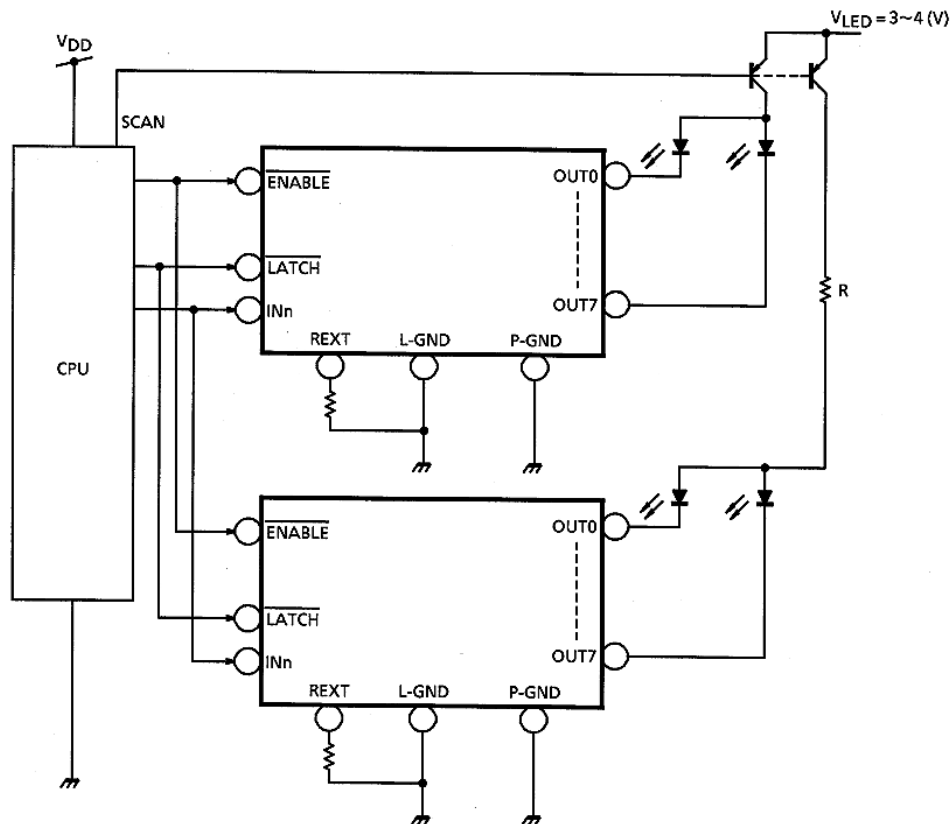
supply voltage (V_O). Moreover, Resistor R is calculable by the lower formula.

$$V_{LED} - V_f \text{ of LED} - V_O(\text{min.})$$

$$I_O(\text{max.}) \times \text{Number of CHs}(\text{max.})$$

Moreover, IC operation may become unstable by long wiring. It recommends arranging IC and LED to near.

APPLICATION



[3] Pattern layout

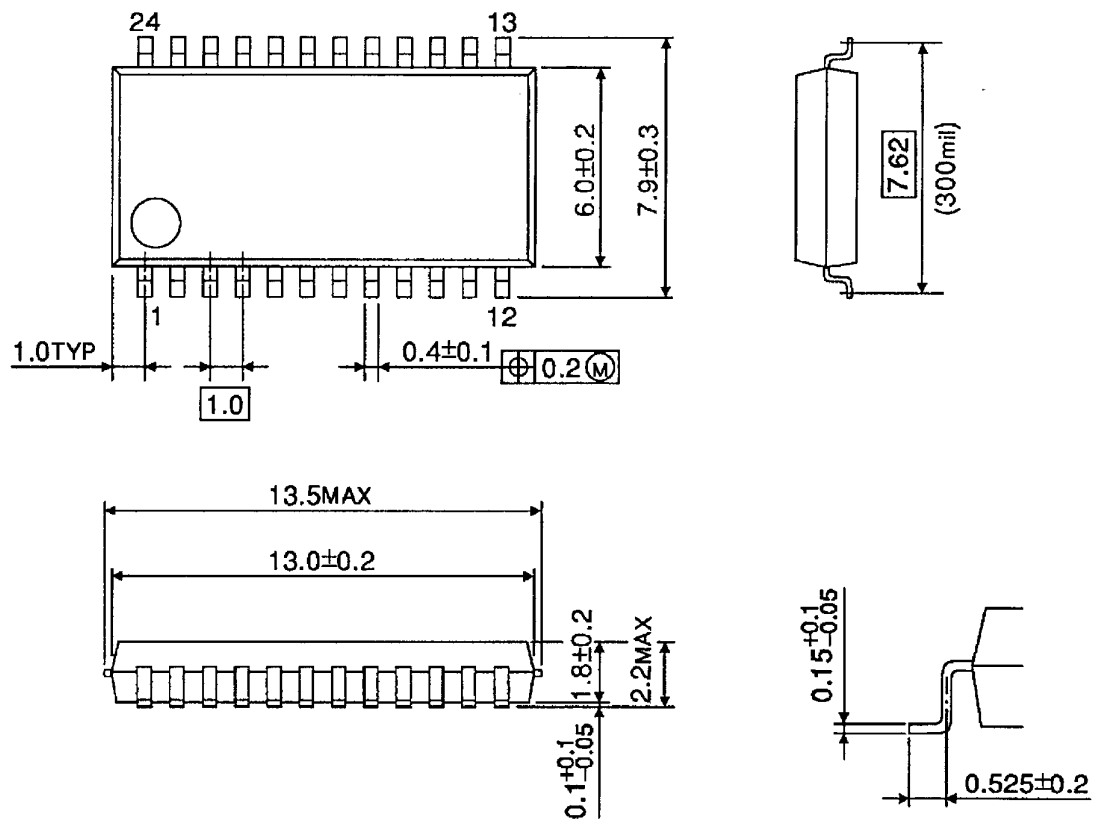
This device owns only one ground pin that means signal ground pin and power ground pin are common.

If ground pattern layout contains large inductance and impedance and the voltage between ground and LATCH, CLOCK terminals exceeds 2.5V by switching noise in operation, this device may miss-operate. So we would life you to pay attention to pattern layout to minimize inductance.

Package Dimensions

SSOP24-P-300-1.00

Unit : mm



Weight: 0.32 g (typ.)

Notes on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Application Circuits

The application circuits shown in this document are provided for reference purposes only.

Thorough evaluation is required, especially at the mass production design stage.

Toshiba does not grant any license to any industrial property rights by providing these examples of application circuits.

5. Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations

Notes on Handling of ICs

- (1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
- (2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.
- (3) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.
- (4) Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly. Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

- (5) Carefully select external components (such as inputs and negative feedback capacitors) and load components (such as speakers), for example, power amp and regulator.

If there is a large amount of leakage current such as input or negative feedback condenser, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, overcurrent or IC failure can cause smoke or ignition. (The over current can cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection type IC that inputs output DC voltage to a speaker directly.

Points to Remember on Handling of ICs**(1) Heat Radiation Design**

In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (T_j) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into consideration the effect of IC heat radiation with peripheral components.

(2) Back-EMF

When a motor rotates in the reverse direction, stops or slows down abruptly, a current flows back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

About solderability, following conditions were confirmed

- Solderability
 - (1) Use of Sn-37Pb solder Bath
 - solder bath temperature = 230°C
 - dipping time = 5 seconds
 - the number of times = once
 - use of R-type flux
 - (2) Use of Sn-3.0Ag-0.5Cu solder Bath
 - solder bath temperature = 245°C
 - dipping time = 5 seconds
 - the number of times = once
 - use of R-type flux

RESTRICTIONS ON PRODUCT USE

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