

350MHz Fixed Gain Amplifiers with Enable

The 5962-0625501QXC is a fully DSCC SMD compliant part and the SMD data sheet is available on the DSCC website (<http://www.dscclia.mil/programs/specfind/default.asp>).

The 5962-0625501QXC is electrically equivalent to the EL5106. Reference equivalent "EL" data sheet for additional information. The 5962-0625501QXC is a fixed gain amplifier with a bandwidth of 350MHz. This amplifier is ideal for today's high speed video and monitor applications. It features internal gain setting resistors and can be configured in a gain of +1, -1 or +2.

With a supply current of just 1.5mA and the ability to run from a single supply voltage from 5V to 12V, these amplifiers are also ideal for handheld, portable or battery powered equipment.

The 5962-0625501QXC has an enable and disable function to reduce the supply current to 25µA typical. Allowing the \overline{CE} pin to float or applying a low logic level will enable the amplifier.

Ordering Information

PART NUMBER (Note)	PART MARKING	PACKAGE	PKG. DWG. #
5962-0625501QXC	06255 01QXC	10 Ld Flat Pack	K10.A

NOTE: These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.

Features

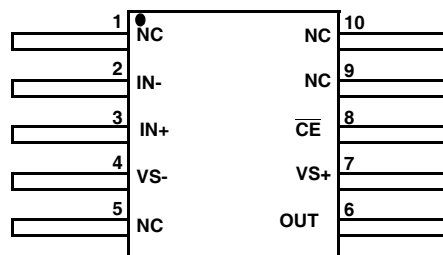
- Gain selectable (+1, -1, +2)
- 350MHz -3dB BW ($A_V = 2$)
- 1.5mA supply current per amplifier
- Fast enable/disable
- Single and dual supply operation, from 5V to 12V

Applications

- Battery powered equipment
- Handheld, portable devices
- Video amplifiers
- Cable drivers
- RGB amplifiers

Pinout

5962-0625501QXC
(10 LD FLAT PACK)
TOP VIEW



Absolute Maximum Ratings ($T_A = +25^{\circ}\text{C}$)

Supply Voltage between V_{S+} and V_{S-} 13.2V
 Pin Voltages $V_{S-} -0.5\text{V}$ to $V_{S+} +0.5\text{V}$
 Maximum Continuous Output Current 20mA

Thermal Information

Thermal Resistance (Typical) θ_{JA} ($^{\circ}\text{C}/\text{W}$) θ_{JC} ($^{\circ}\text{C}/\text{W}$)
 Flat Pack Package (Notes 1, 2) 165 60
 Storage Temperature -65°C to $+150^{\circ}\text{C}$
 Ambient Operating Temperature -55°C to $+125^{\circ}\text{C}$
 Operating Junction Temperature $+150^{\circ}\text{C}$
 Power Dissipation 21.8mW

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. For θ_{JC} , the "case temp" location is the center of the exposed metal pad on the package underside.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

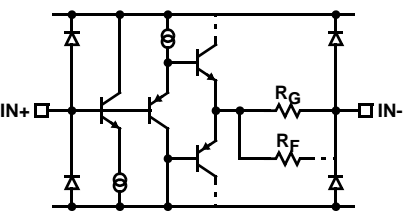
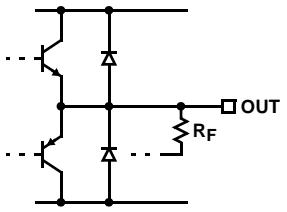
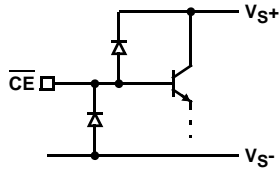
Electrical Specifications $V_{S+} = +5\text{V}$, $V_{S-} = -5\text{V}$, $R_L = 150\Omega$, $T_A = +25^{\circ}\text{C}$ unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
BW	-3dB Bandwidth	$A_V = +1$		250		MHz
		$A_V = -1$		380		MHz
		$A_V = +2$		350		MHz
BW1	0.1dB Bandwidth			20		MHz
SR	Slew Rate	$V_O = -2.5\text{V}$ to $+2.5\text{V}$, $A_V = +2$		4500		V/ μs
t_S	0.1% Settling Time	$V_{OUT} = -2.5\text{V}$ to $+2.5\text{V}$, $A_V = 2$		16		ns
e_N	Input Voltage Noise			2.8		nV/ $\sqrt{\text{Hz}}$
i_{N+}	IN+ Input Current Noise			6		pA/ $\sqrt{\text{Hz}}$
dG	Differential Gain Error (Note 3)	$A_V = +2$		0.02		%
dP	Differential Phase Error (Note 3)	$A_V = +2$		0.04		$^{\circ}$
DC PERFORMANCE						
R_F , R_G	Internal R_F and R_G			325		Ω
INPUT CHARACTERISTICS						
R_{IN}	Input Resistance	at I_{N+}		2		M Ω
C_{IN}	Input Capacitance			1		pF
ENABLE						
t_{EN}	Enable Time			280		ns
t_{DIS}	Disable Time			400		ns

NOTE:

3. Standard NTSC test, AC signal amplitude = 286mV_{P-P}, $f = 3.58\text{MHz}$

Pin Descriptions

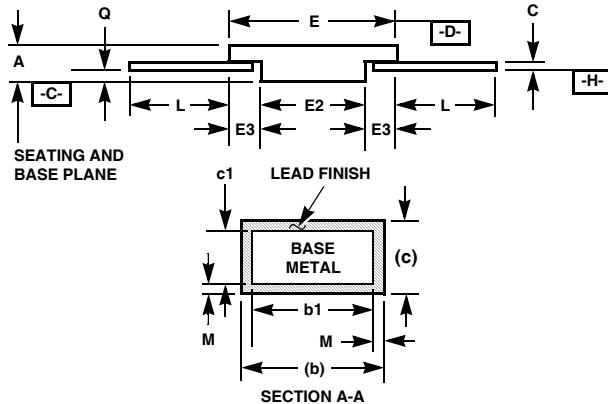
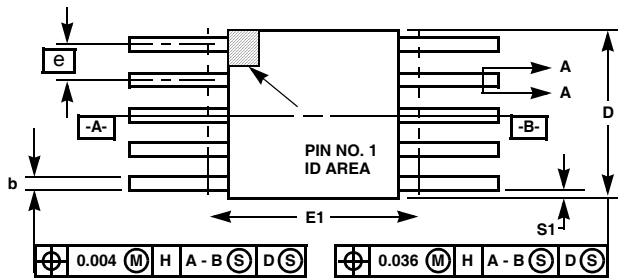
5962-0625501QXCIS (10 LD FLAT PACK)	PIN NAME	FUNCTION	EQUIVALENT CIRCUIT
1, 5, 9, 10	NC	Not connected	
2	IN-	Inverting input	 <p>CIRCUIT 1</p>
3	IN+	Non-inverting input	(Reference Circuit 1)
4	VS-	Negative supply	
6	OUT	Output	 <p>CIRCUIT 2</p>
7	VS+	Positive supply	
8	$\overline{\text{CE}}$	Chip enable	 <p>CIRCUIT 3</p>

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Ceramic Metal Seal Flatpack Packages (Flatpack)**K10.A MIL-STD-1835 CDFP3-F10 (F-4A, CONFIGURATION B)
10 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.290	-	7.37	3
E	0.240	0.260	6.10	6.60	-
E1	-	0.280	-	7.11	3
E2	0.125	-	3.18	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.250	0.370	6.35	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.005	-	0.13	-	6
M	-	0.0015	-	0.04	-
N	10		10		-

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NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.