5962-0721301QXC, 5962-0721302QXC, 5962-0721303QYC

Data Sheet | October 17, 2007 | FN6478.1

500MHz Rail-to-Rail Amplifiers

The 5962-0721301QXC, 5962-0721302QXC and 5962-0721303QYC are fully DSCC SMD compliant parts and the SMD data sheets are available on the DSCC website (http://www.dscc.dla.mil/ programs/specfind/default.asp). The 5962-0721301QXC is electrically equivalent to the EL8202, the 5962-0721302QXC is electrically equivalent to the EL8203, and the 5962-0721303QYC is electrically equivalent to the EL8403. Reference equivalent “EL” data sheet for additional information. These parts are dual and quad rail-to-rail amplifiers with a -3dB bandwidth of 500MHz and slew rate of 600V/µs.

Running off a low supply current of 13.5mA per channel, the 5962-0721301QXC, 5962-0721302QXC, and 5962-0721303QYC also feature inputs that go to 0.15V below the V_S- rail. The 5962-0721301QXC and 5962-0721302QXC are dual channel amplifiers. The 5962-0721303QYC is a quad channel amplifier.

The 5962-0721301QXC includes a fast-acting disable/power-down circuit with a 25ns disable and a 200ns enable, the 5962-0721301QXC is ideal for multiplexing applications.

Features

- 500MHz -3dB bandwidth
- 600V/µs slew rate
- Supplies from 3V to 5.5V
- Rail-to-rail output
- Input to 0.15V below V_S-
- Fast 25ns disable (5962-0721301QXC only)

Applications

- Video amplifiers
- Portable/hand-held products
- Communications devices

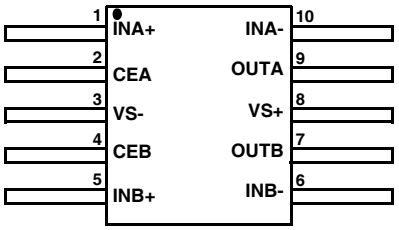
Ordering Information

PART NUMBER	PART MARKING	PACKAGE	PKG. DWG. #
5962-0721301QXC	07213 01QXC	10 Ld Flat Pack	K10.A
5962-0721302QXC	07213 02QXC	10 Ld Flat Pack	K10.A
5962-0721303QYC	07213 03QYC	14 Ld Flat Pack	K14.A

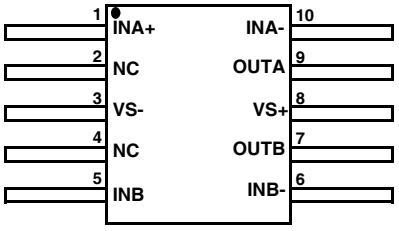
NOTE: These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.

Pinouts

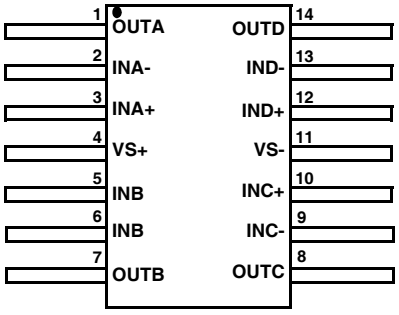
5962-0721301QXC
(10 LD FLATPACK)
TOP VIEW



5962-0721302QXC
(10 LD FLATPACK)
TOP VIEW



5962-0721303QYC
(14 LD FLATPACK)
TOP VIEW



Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage from V_S+ to V_S- 5.5V
Input Voltage . . . . . V_S+ +0.3V to V_S- -0.3V
Differential Input Voltage 2V
Continuous Output Current . . . . . 20mA/Op Amp

Thermal Information

Power Dissipation . . . . . 74.3mW/Op Amp
Storage Temperature . . . . . .-65°C to +150°C
Ambient Operating Temperature . . . . . .-55°C to +125°C
Operating Junction Temperature . . . . . .+150°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

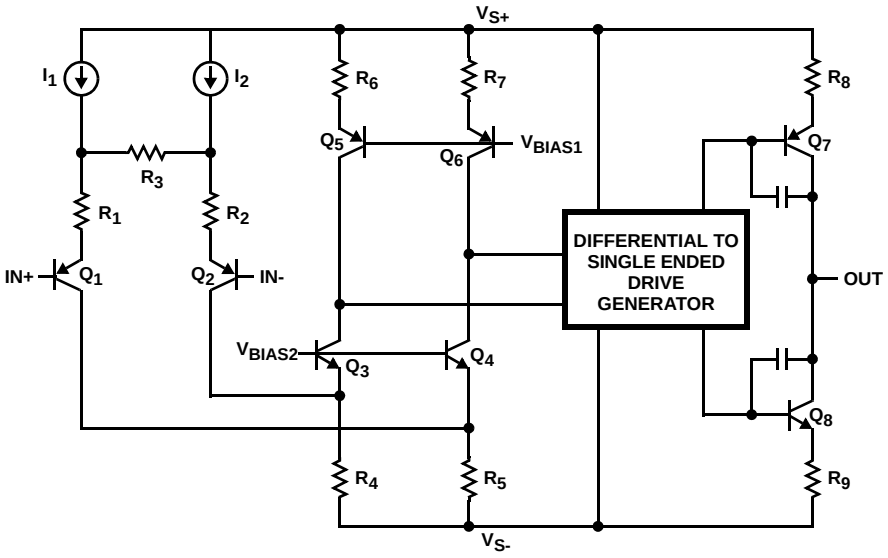
V_S+ = 5V, V_S- = GND, T_A = +25°C, V_{CM} = 2.5V, R_L to 2.5V, A_V = 1, Unless Otherwise Specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
R_{IN}	Input Resistance	Common Mode		3.5		MΩ
C_{IN}	Input Capacitance			0.5		pF
OUTPUT CHARACTERISTICS						
R_{OUT}	Output Resistance	A_V = +1		30		mΩ
I_{OUT}	Linear Output Current			65		mA
ENABLE (5962-0721301QXC ONLY)						
t_{EN}	Enable Time			200		ns
t_{DS}	Disable Time			25		ns
V_{IH-ENB}	$\overline{\text{ENABLE}}$ Pin Voltage for Power-up			0.8		V
V_{IL-ENB}	$\overline{\text{ENABLE}}$ Pin Voltage for Shut-down			2		V
AC PERFORMANCE						
BW	-3dB Bandwidth	A_V = +1, R_F = 0Ω, C_L = 2.5pF		500		MHz
		A_V = -1, R_F = 1kΩ, C_L = 2.5pF		140		MHz
		A_V = +2, R_F = 1kΩ, C_L = 2.5pF		165		MHz
		A_V = +10, R_F = 1kΩ, C_L = 2.5pF		18		MHz
BW	±0.1dB Bandwidth	A_V = +1, R_F = 0Ω, C_L = 2.5pF		35		MHz
Peak	Peaking	A_V = +1, R_L = 1kΩ, C_L = 2.5pF		2		dB
GBWP	Gain Bandwidth Product			200		MHz
PM	Phase Margin	R_L = 1kΩ, C_L = 2.5pF		55		°
SR	Slew Rate	A_V = 2, R_L = 100Ω, V_{OUT} = 0.5V to 4.5V		600		V/µs
t_R	Rise Time	$2.5V_{STEP}$, 20% to 80%		4		ns
t_F	Fall Time	$2.5V_{STEP}$, 20% to 80%		2		ns
OS	Overshoot	200mV step		10		%
t_{PD}	Propagation Delay	200mV step		1		ns
t_S	0.1% Settling Time	200mV step		15		ns
dG	Differential Gain	A_V = +2, R_F = 1kΩ, R_L = 150Ω		0.01		%
dP	Differential Phase	A_V = +2, R_F = 1kΩ, R_L = 150Ω		0.01		°
e_N	Input Noise Voltage	f = 10kHz		12		nV/√Hz
i_N+	Positive Input Noise Current	f = 10kHz		1.7		pA/√Hz
i_N-	Negative Input Noise Current	f = 10kHz		1.3		pA/√Hz
e_S	Channel Separation	f = 100kHz		95		dB

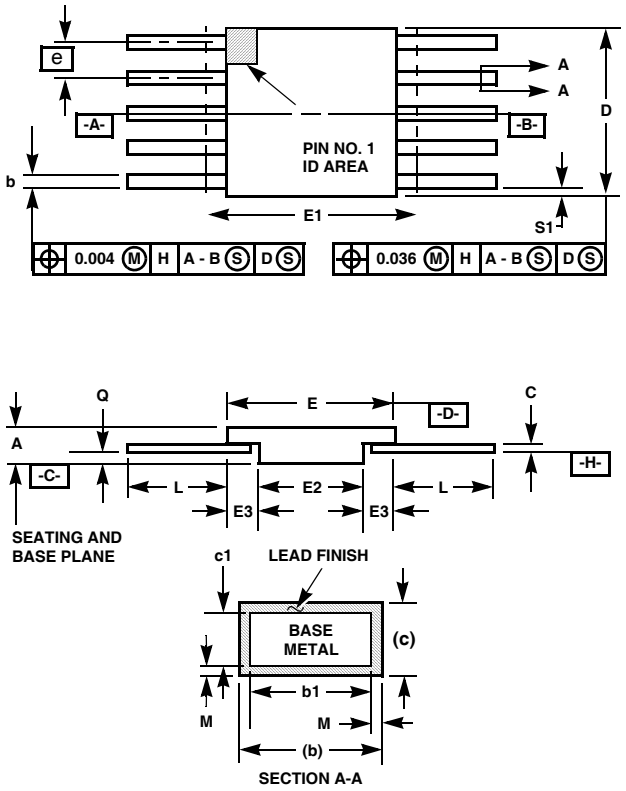
Pin Descriptions

5962-0721301QXC (10 LD FLATPACK)	5962-0721302QXC (10 LD FLATPACK)	5962-0721303QYC (14 LD FLATPACK)	NAME	FUNCTION
1, 5	1, 5	3, 5, 10, 12	IN+	Non-inverting input for each channel
2, 4			$\overline{CE}$	Enable and disable input for each channel
3	3	11	VS-	Negative power supply
6, 10	6, 10	2, 6, 9, 13	IN-	Inverting input for each channel
7, 9	7, 9	1, 7, 8, 14	OUT	Amplifier output for each channel
8	8	4	VS+	Positive power supply
	2, 4		NC	Not Connected

Simplified Schematic Diagram



Ceramic Metal Seal Flatpack Packages (Flatpack)



K10.A MIL-STD-1835 CDFP3-F10 (F-4A, CONFIGURATION B)
10 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

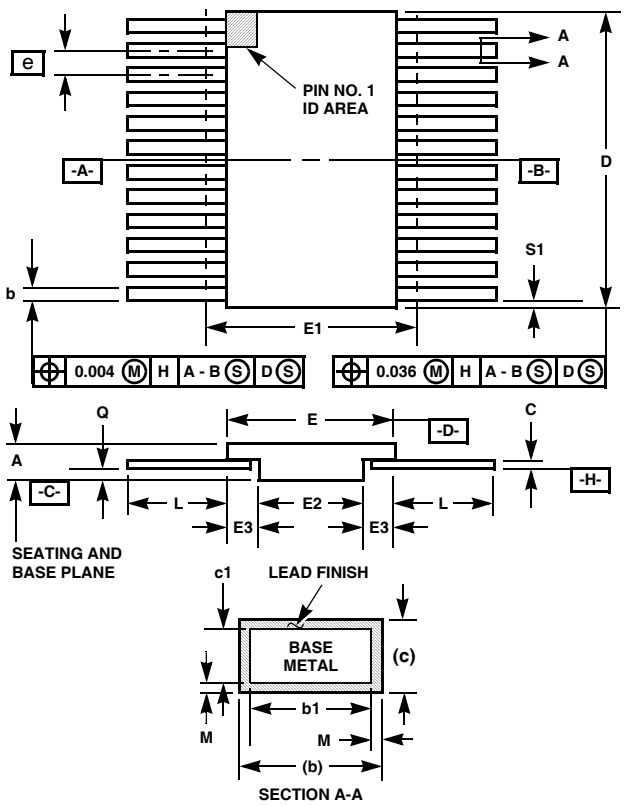
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.290	-	7.37	3
E	0.240	0.260	6.10	6.60	-
E1	-	0.280	-	7.11	3
E2	0.125	-	3.18	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.250	0.370	6.35	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.005	-	0.13	-	6
M	-	0.0015	-	0.04	-
N	10		10		-

Rev. 0 3/07

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

14 ld FLATPACK Package Outline Drawing



K14.A MIL-STD-1835 CDFP3-F14 (F-2A, CONFIGURATION B)
14 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.390	-	9.91	3
E	0.235	0.260	5.97	6.60	-
E1	-	0.290	-	7.11	3
E2	0.125	-	3.18	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.270	0.370	6.86	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.005	-	0.13	-	6
M	-	0.0015	-	0.04	-
N	14		14		-

Rev. 0 5/18/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
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