MC10EP89

3.3V / 5V ECL Coaxial Cable Driver

The MC10EP89 is a differential fanout gate specifically designed to drive coaxial cables. The device is especially useful in digital video broadcasting applications; for this application, since the system is polarity free, each output can be used as an independent driver. The driver produces swings 70% larger than a standard ECL output. When driving a coaxial cable, proper termination is required at both ends of the line to minimize signal loss. The 1.6 V (5 V) and 1.4 V (3.3 V) swing allow for termination at both ends of the cable, while maintaining a 800 mV (5 V) and 700 mV (3.3 V) swing at the receiving end of the cable. Because of the larger output swings, the device cannot be terminated into the standard V_{CC}–2.0 V. All of the DC parameters are tested with a 50 Ω to V_{CC}–3.0 V load. The driver accepts a standard differential ECL input and can run off of the digital video broadcast standard –5.0 V supply.

- 310 ps Typical Propagation Delay
- Maximum Frequency > 3 Ghz Typical
- 1.6 V (5 V) and 1.4 V (3.3 V) Swing
- PECL Mode Operating Range: V_{CC}= 3.0 V to 5.5 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –3.0 V to –5.5 V
- Internal Input Resistors: Pulldown on D, Pulldown and Pullup on $\overline{D}$
- Q Output will default LOW with inputs open or at V_{EE}
- ESD Protection: >4 KV HBM, >200 V MM, >2 KV CDM
- New Differential Input Common Mode Range
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1, Indefinite Time Out of Drypack
- Flammability Rating: UL–94 code V–0 @ 1/8”, Oxygen Index 28 to 34
- Transistor Count = 152 devices

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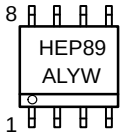
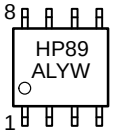
MARKING DIAGRAMS*

SO–8
D SUFFIX
CASE 751



TSSOP–8
DT SUFFIX
CASE 948R

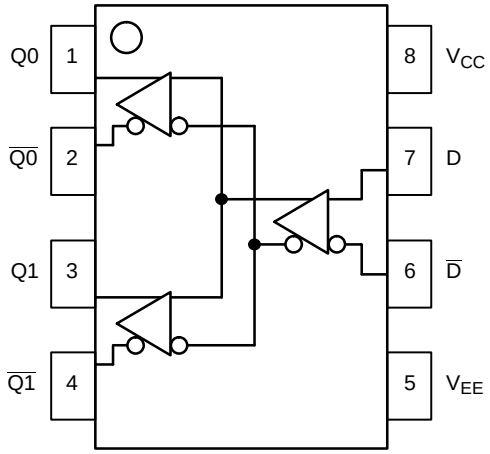


A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC10EP89D	SO–8	98 Units/Rail
MC10EP89DR2	SO–8	2500 Tape & Reel
MC10EP89DT	TSSOP–8	98 Units/Rail
MC10EP89DTR2	TSSOP–8	2500 Tape & Reel



PIN DESCRIPTION

PIN	FUNCTION
D, $\overline{D}$	ECL Data Inputs
Q0, Q1, $\overline{Q0}$, $\overline{Q1}$	ECL Data Outputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply

Figure 1. 8–Lead Pinout (Top View) **and Logic Diagram**

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		6	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–6	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

DC CHARACTERISTICS, PECL V_{CC} = 3.3 V, V_{EE} = 0 V (Note 2.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current	22	28	34	24	32	38	28	34	40	mA
V_{OH}	Output HIGH Voltage (Note 3.)	2080	2180	2280	2150	2250	2350	2225	2325	2425	mV
V_{OL}	Output LOW Voltage (Note 3.)	620	720	820	630	730	830	670	770	870	mV
V_{IH}	Input HIGH Voltage (Single Ended)	2070		2410	2170		2490	2240		2580	mV
V_{IL}	Input LOW Voltage (Single Ended)	1350		1800	1350		1820	1350		1855	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 4.)	2.0		3.3	2.0		3.3	2.0		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

2. Input and output parameters vary 1:1 with V_{CC}.
3. All loading with 50 ohms to V_{CC}–3.0 volts.
4. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

DC CHARACTERISTICS, PECL V_{CC} = 5.0 V, V_{EE} = 0 V (Note 5.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current	27	34	41	30	37	44	32	39	46	mA
V_{OH}	Output HIGH Voltage (Note 6.)	3780	3880	3980	3850	3950	4050	3925	4025	4125	mV
V_{OL}	Output LOW Voltage (Note 6.)	2075	2225	2375	2060	2210	2360	2090	2240	2390	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3770		4110	3870		4190	3940		4280	mV
V_{IL}	Input LOW Voltage (Single Ended)	3050		3500	3050		3520	3050		3555	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 7.)	2.0		5.0	2.0		5.0	2.0		5.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

5. Input and output parameters vary 1:1 with V_{CC}.
6. All loading with 50 ohms to V_{CC}–3.0 volts.
7. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

DC CHARACTERISTICS, NECL V_{CC} = 0 V; V_{EE} = –3.3 V (Note 8.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current	22	28	34	24	32	38	28	34	40	mA
V_{OH}	Output HIGH Voltage (Note 9.)	–1220	–1120	–1020	–1150	–1050	–950	–1075	–975	–875	mV
V_{OL}	Output LOW Voltage (Note 9.)	–2680	–2580	–2480	–2670	–2570	–2470	–2630	–2530	–2430	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1230		–890	–1130		–810	–1060		–720	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1950		–1500	–1950		–1480	–1950		–1445	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 10.)	–1.3		0.0	–1.3		0.0	–1.3		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

8. Input and output parameters vary 1:1 with V_{CC}.
9. All loading with 50 ohms to V_{CC}–3.0 volts.
10. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

DC CHARACTERISTICS, NECL V_{CC} = 0V; V_{EE} = –5.2 (Note 11.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current	25	32	39	28	35	42	31	38	45	mA
V_{OH}	Output HIGH Voltage (Note 12.)	–1220	–1120	–1020	–1150	–1050	–950	–1075	–975	–875	mV
V_{OL}	Output LOW Voltage (Note 12.)	–2950	–2800	–2650	–2950	–2850	–2650	–2950	–2800	–2650	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1230		–890	–1130		–810	–1060		–720	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1950		–1500	–1950		–1480	–1950		–1445	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 13.)	–3.2		0.0	–3.2		0.0	–3.2		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

11. Input and output parameters vary 1:1 with V_{CC}.
12. All loading with 50 ohms to V_{CC}–3.0 volts.
13. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

AC CHARACTERISTICS V_{CC} = 0V; V_{EE} = –3.0 V to –5.5 V or V_{CC} = 3.0 V to 5.5 V; $V_{EE = 0\ V}$ (Note 14.)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Toggle (See Figure 2. F_{max}/JITTER)			> 3			> 3			> 3	GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential	220	280	340	250	310	370	270	330	390	ps
t_{SKEW}	Within Device Skew Q, $\overline{Q}$ Device to Device Skew (Note 15.)		5.0	20 120		5.0	20 120		5.0	20 120	ps
t_{JITTER}	Cycle–to–Cycle Jitter (See Figure 2. F_{max}/JITTER)		.5	< 1		.5	< 1		.5	< 1	ps
V_{PP}	Input Voltage Swing (Differential)	150	800	1200	150	800	1200	150	800	1200	mV
t_r t_f	Output Rise/Fall Times Q, $\overline{Q}$ (20% – 80%)	175	250	325	200	275	350	225	295	375	ps

14. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 ohms to V_{CC}–2.0 V.
15. Skew is measured between outputs under identical transitions.

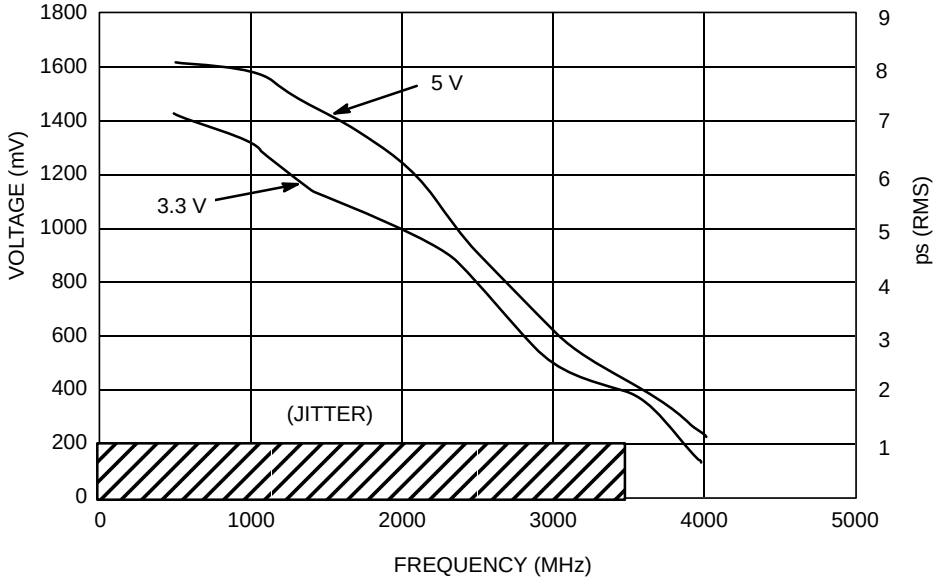


Figure 2. F_{max}/Jitter

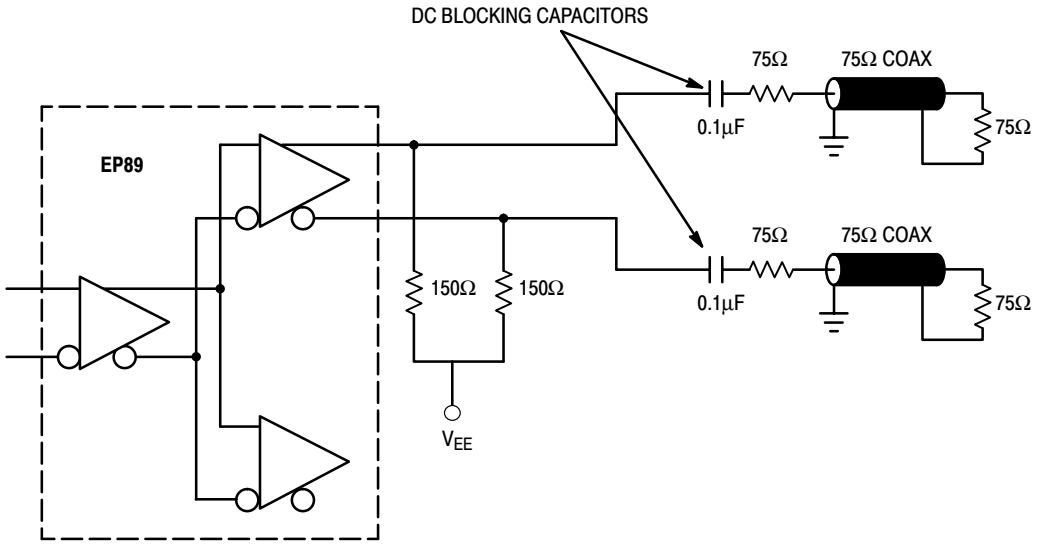


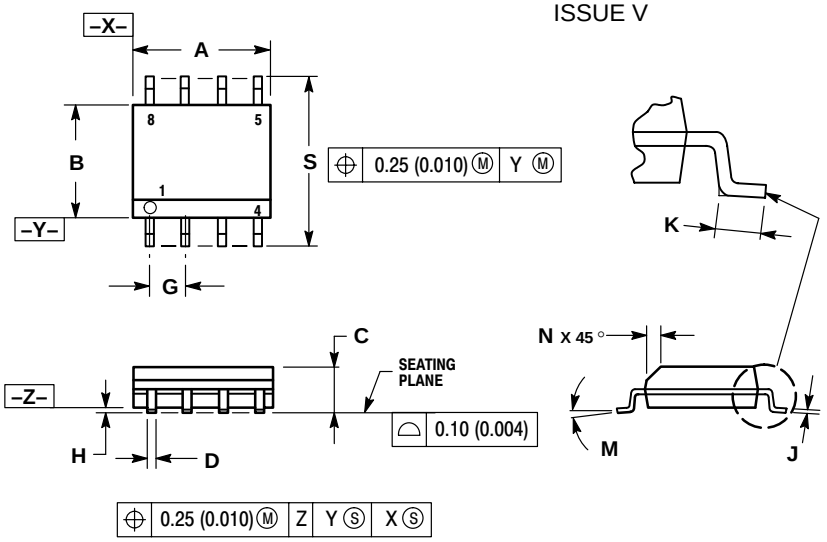
Figure 3. Termination Configuration

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8009	–	ECLinPS Plus Spice I/O Model Kit
AND8020	–	Termination of ECL Logic Devices

PACKAGE DIMENSIONS

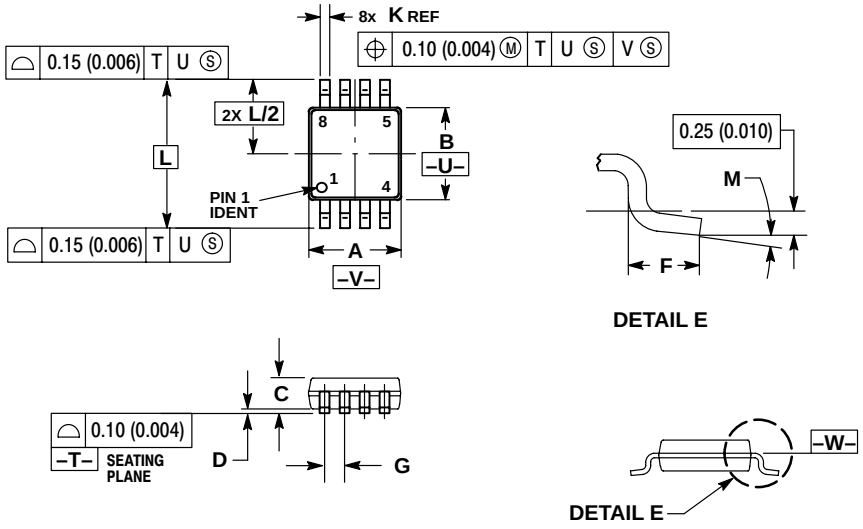
SO–8
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751–07
ISSUE V



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

TSSOP–8
DT SUFFIX
CASE 948R–02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0 °	6 °	0 °	6 °

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