MC100EPT25

-3.3V / -5V Differential ECL to LVTTL Translator

The MC100EPT25 is a Differential ECL to LVTTL translator. This device requires +3.3 V, –3.3 V to –5.2 V, and ground. The small outline 8–lead package and the single gate of the EPT25 make it ideal for applications which require the translation of a clock or data signal.

The V_{BB} output allows the EPT25 to also be used in a single–ended input mode. In this mode the V_{BB} output is tied to the D input for a non–inverting buffer or the $\overline{D}$ input for an inverting buffer. If used, the V_{BB} pin should be bypassed to ground via a 0.01 mF capacitator.

- 1.1 ns Typical Propagation Delay
- 275 MHz Fmax (Clock bit stream, not pseudo–random)
- Differential LVECL/ECL inputs
- The 100 Series Contains Temperature Compensation
- Operating Range: $V_{CC=}$ 3.0 V to 3.6 V; V_{EE}= –5.5 V to –3.0 V; GND = 0 V
- 24 mA TTL outputs
- Flow Through Pinouts
- Internal Input Resistors: Pulldown on D, Pulldown and Pullup on $\overline{D}$
- Q Output will default LOW with inputs open or at V_{EE}
- ESD Protection: 4 KV HBM, 200 V MM, 2 KV CDM
- V_{BB} Output
- New Differential Input Common Mode Range
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1, Indefinite Time Out of Drypack. For Additional Information, See Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”, Oxygen Index 28 to 34
- Transistor Count = 111 devices

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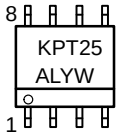
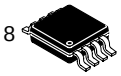
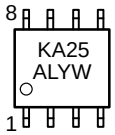
MARKING DIAGRAMS*

SO–8
D SUFFIX
CASE 751





TSSOP–8
DT SUFFIX
CASE 948R

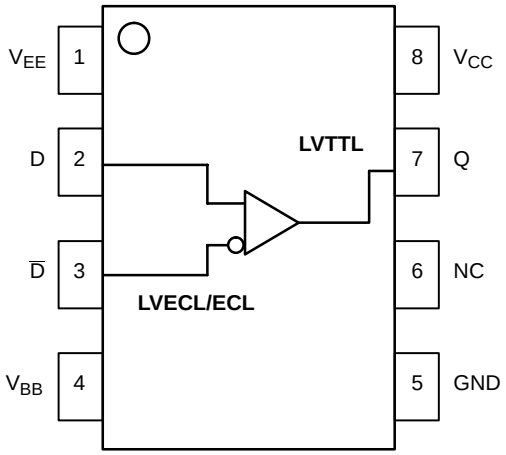


A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100EPT25D	SO–8	98 Units / Rail
MC100EPT25DR2	SO–8	2500 Tape & Reel
MC100EPT25DT	TSSOP–8	98 Units / Rail
MC100EPT25DTR2	TSSOP–8	2500 Tape & Reel



PIN DESCRIPTION

PIN	FUNCTION
Q	LVTTL Output
D, $\overline{D}$	Differential ECL Input Pair
V_{CC}	Positive Supply
V_{BB}	Output Reference Voltage
GND	Ground
V_{EE}	Negative Supply
NC	No Connect

Figure 1. 8–Lead Pinout (Top View) **and Logic Diagram**

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	Positive Power Supply	GND = 0 V	V_{EE} = –5.0 V	3.8	V
V_{EE}	Negative Power Supply	GND = 0 V	V_{CC} = +3.3 V	–6	V
V_{IN}	Input Voltage	GND = 0 V		0 to V_{EE}	V
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

NECL DC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= –5.5 V to –3.0 V; GND= 0.0 V (Note 2.)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
IEE	Power Supply Current	8.0	16	25	8.0	16	25	8.0	16	25	mA
V_{IH}	Input HIGH Voltage Single Ended	–1225		–880	–1225		–880	–1225		–880	mV
V_{IL}	Input LOW Voltage Single Ended	–1945		–1625	–1945		–1625	–1945		–1625	mV
V_{BB}	Output Voltage Reference	–1525	–1425	–1325	–1525	–1425	–1325	–1525	–1425	–1325	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 3.)	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: 100EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

2. Input parameters vary 1:1 with GND.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

TTL OUTPUT DC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= –5.5 V to –3.0 V; GND= 0.0 V; T_A= –40°C to 85°C

Symbol	**Characteristic**	**Condition**	**Min**	**Typ**	**Max**	**Unit**
V_{OH}	Output HIGH Voltage (Note 4.)	I_{OH} = –3.0 mA	2.2			V
V_{OL}	Output LOW Voltage (Note 4.)	I_{OL} = 24 mA			0.5	V
I_{CCH}	Power Supply Current		6	10	14	mA
I_{CCL}	Power Supply Current		7	12	17	mA

NOTE: 100EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

4. All loading with 500 ohms to GND; CL = 20pF.

AC CHARACTERISTICS V_{CC}= 3.0 V to 3.6 V; V_{EE}= –5.5 V to –3.0 V; GND= 0.0 V (Note 5.)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Frequency (See Figure 2. F_{max}/JITTER)	275			275			275			MHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential	800	1200	1800	800	1100	1600	800	1100	1600	ns
t_{SKPP}	Device–to–Device Skew (Note 6.)			500			500			500	ps
t_{JITTER}	Cycle–to–Cycle Jitter (See Figure 2. F_{max}/JITTER)		0.2	< 1		0.2	< 1		0.2	< 1	ps
V_{PP}	Input Voltage Swing (Differential)	150	800	1200	150	800	1200	150	800	1200	mV
t_r t_f	Output Rise/Fall Times Q, $\overline{Q}$ (0.8V – 2.0V)	450 900	600 1160	750 1400	450 900	600 1100	750 1400	450 900	600 1100	750 1400	ps

5. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 500 ohms to GND.
6. Skews are measured between outputs under identical conditions.

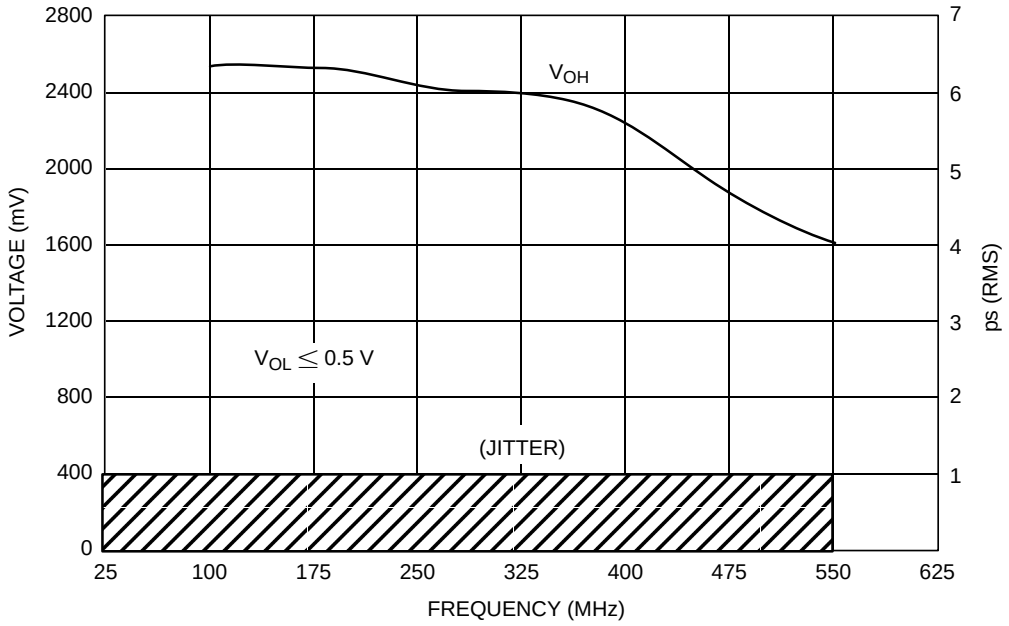


Figure 2. F_{max}/Jitter

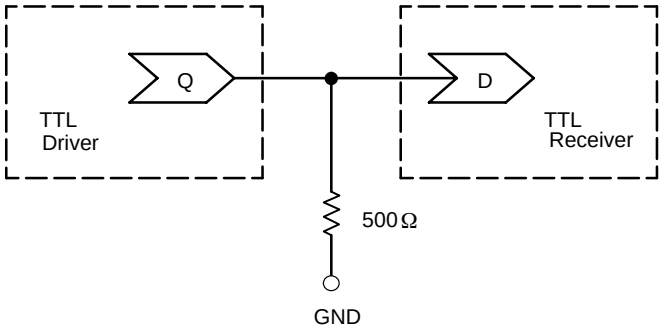


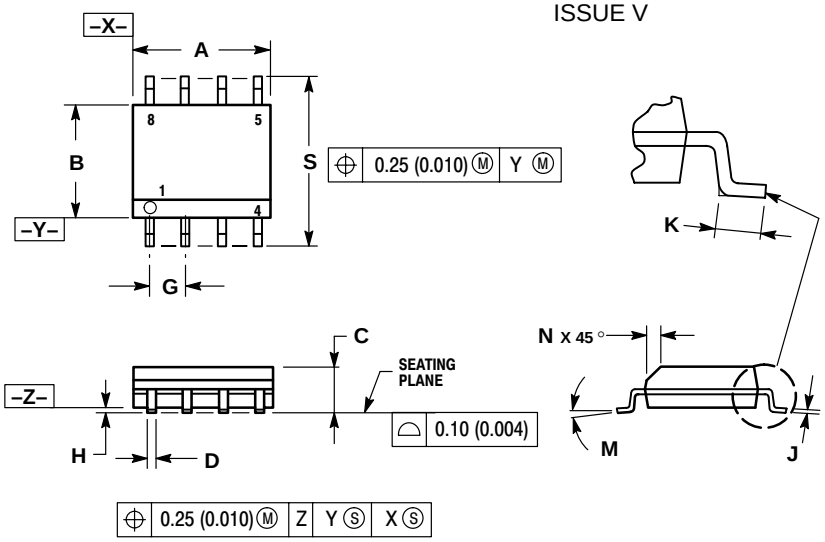
Figure 3. TTL Output Termination

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

PACKAGE DIMENSIONS

SO–8
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751–07
ISSUE V

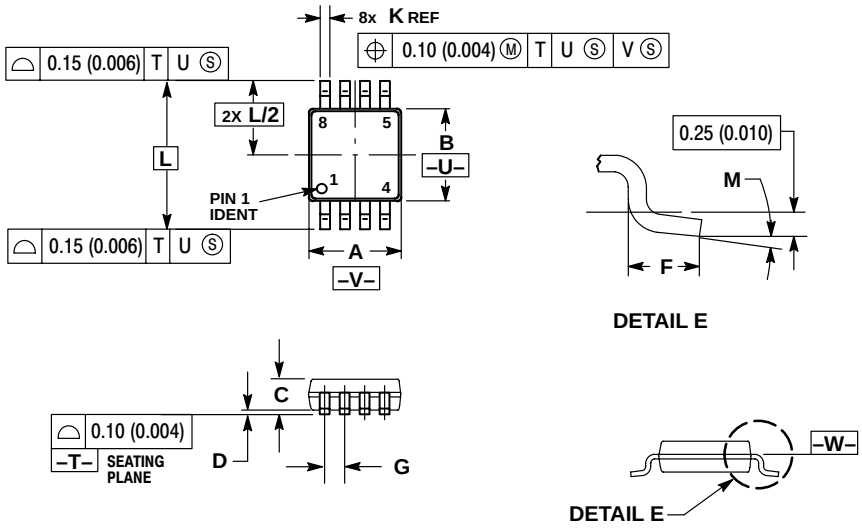


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

PACKAGE DIMENSIONS

TSSOP–8
DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948R–02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

Notes

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