# MC100LVE222

# 3.3V ECL 1:15 Differential ÷1/÷2 Clock Driver

The MC100LVE222 is a low skew 1:15 differential ÷1/÷2 ECL fanout buffer designed with clock distribution in mind. The LVECL/LVPECL input signal pairs can be differential or used single–ended (with VBB output reference bypassed and connected to the unused input of a pair). Either of two fully differential clock inputs may be selected. Each of the four output banks of 2, 3, 4, and 6 differential pairs may be independently configured to fanout 1X or 1/2X of the input frequency. The LVE222 specifically guarantees low output to output skew. Optimal design, layout, and processing minimize skew within a device and from lot to lot.

The fsel pins and CLK_Sel pin are asynchronous control inputs. Any changes may cause indeterminate output states requiring a MR pulse to resynchronize any 1/2X outputs.

To ensure that the tight skew specification is realized, both sides of any differential output pair need to be terminated identically even if only one side is being used. When fewer than all fifteen pairs are used, identically terminate all the output pairs on the same package side whether used or unused. If no outputs on a side are used, then leave all these outputs open (unterminated). This will maintain minimum output skew. Failure to do this will result in a 10–20 ps loss of skew margin (propagation delay) in the output(s) in use.

The MC100LVE222, as with most ECL devices, can be operated from a positive $V_{CC}$ supply in PECL mode. This allows the LVE222 to be used for high performance clock distribution in +3.3 V systems. Designers can take advantage of the LVE222's performance to distribute low skew clocks across the backplane or the board. In a PECL environment series or Thevenin line, terminations are typically used as they require no additional power supplies. All power supply pins must be connected. For more information on using PECL, designers should refer to Application Note AN1406/D. For a SPICE model, see Application Note AN1560/D.

- 200 ps Part–to–Part Skew
- 50 ps Output–to–Output Skew
- Selectable 1x or 1/2x Frequency Outputs
- ESD Protection: >2 KV HBM, >200 V MM
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: $V_{CC}$= 3.0 V to 3.8 V with $V_{EE}$= 0 V
- NECL Mode Operating Range: $V_{CC}$= 0 V with $V_{EE}$= –3.0 V to –3.8 V
- Internal Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 2
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8",
  Oxygen Index 28 to 34
- Transistor Count = 684 devices

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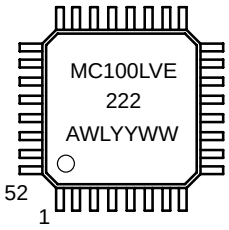
**MARKING DIAGRAM***

**TQFP**
**FA SUFFIX**
**CASE 848D**



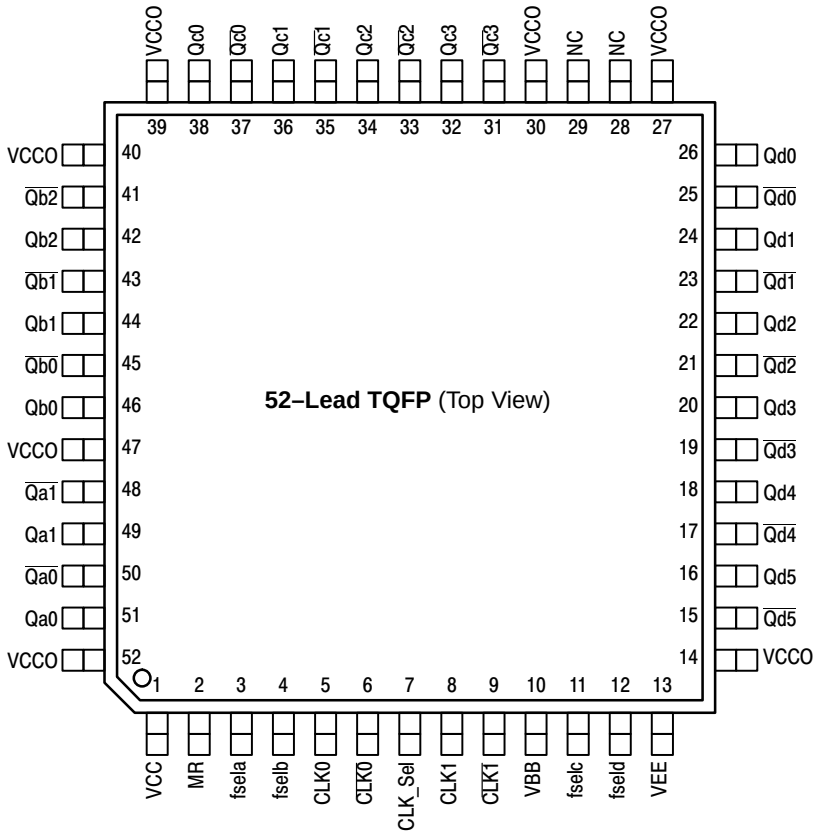

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*For additional information, see Application Note AND8002/D

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MC100LVE222FA | TQFP | 160 Units/Tray |
| MC100LVE222FAR2 | TQFP | 1500 Tape & Reel |

## LOGIC DIAGRAM AND PINOUT ASSIGNMENT




**52–Lead TQFP** (Top View)

## FUNCTION TABLE

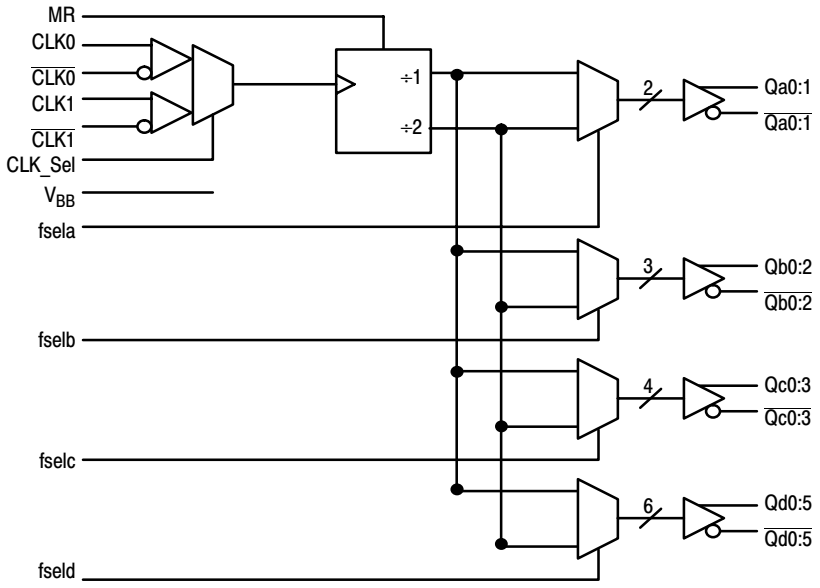
| Input | Function | |
|---|---|---|
| | L | H |
| MR | Active | Reset |
| CLK_Sel | CLK0 | CLK1 |
| fseln | ÷1 | ÷2 |

## PIN DESCRIPTION

| PIN | FUNCTION |
|---|---|
| CLK0, $\overline{\text{CLK0}}$ | ECL Differential Input Clock |
| CLK1, $\overline{\text{CLK1}}$ | ECL Differential Input Clock |
| CLK_Sel | ECL Clock Select |
| MR | ECL Master Reset |
| Qa0:1, $\overline{\text{Qa0:1}}$ | ECL Differential Outputs |
| Qb0:2, $\overline{\text{Qb0:2}}$ | ECL Differential Outputs |
| Qc0:3, $\overline{\text{Qc0:3}}$ | ECL Differential Outputs |
| Qd0:5, $\overline{\text{Qd0:5}}$ | ECL Differential Outputs |
| fseln | ECL ÷1 or ÷2 Select |
| $V_{BB}$ | Reference Voltage Output |
| $V_{CC}$, $V_{CCO}$ | Positive Supply |
| $V_{EE}$ | Negative Supply |
| NC | No Connect |

Warning: All $V_{CC}$, $V_{CCO}$, and $V_{EE}$ pins must be externally connected to Power Supply to guarantee proper operation.

## LOGIC SYMBOL



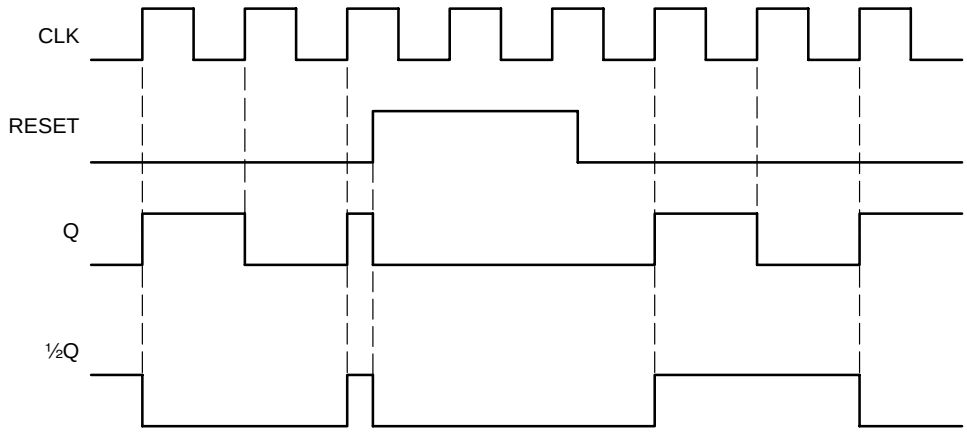



**Figure 1. Timing Diagram**

**MAXIMUM RATINGS** (Note 1.)

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Units |
|---|---|---|---|---|---|
| $V_{CC}$ | PECL Mode Power Supply | $V_{EE}$ = 0 V | | 8 to 0 | V |
| $V_{EE}$ | NECL Mode Power Supply | $V_{CC}$ = 0 V | | –8 to 0 | V |
| $V_I$ | PECL Mode Input Voltage<br>NECL Mode Input Voltage | $V_{EE}$ = 0 V<br>$V_{CC}$ = 0 V | $V_I \leq V_{CC}$<br>$V_I \geq V_{EE}$ | 6 to 0<br>–6 to 0 | V<br>V |
| $I_{out}$ | Output Current | Continuous<br>Surge | | 50<br>100 | mA<br>mA |
| $I_{BB}$ | $V_{BB}$ Sink/Source | | | ± 0.5 | mA |
| TA | Operating Temperature Range | | | –40 to +85 | °C |
| $T_{stg}$ | Storage Temperature Range | | | –65 to +150 | °C |
| $\theta_{JA}$ | Thermal Resistance (Junction to Ambient) | 0 LFPM<br>500 LFPM | 52 TQFP<br>52 TQFP | 70<br>48 | °C/W<br>°C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction to Case) | std bd | 52 TQFP | TBD | °C/W |
| $T_{sol}$ | Wave Solder | <2 to 3 sec @ 248°C | | 265 | °C |

1. Maximum Ratings are those values beyond which device damage may occur.

**LVPECL DC CHARACTERISTICS** $V_{CC}$= 3.3 V; $V_{EE}$= 0.0 V (Note 1.)

| | | –40°C | | | 25°C | | | 85°C | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Characteristic** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| $I_{EE}$ | Power Supply Current | | 122 | 136 | | 122 | 136 | | 125 | 139 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 2.) | 2215 | 2295 | 2420 | 2275 | 2345 | 2420 | 2275 | 2345 | 2420 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 2.) | 1470 | 1605 | 1745 | 1490 | 1595 | 1680 | 1490 | 1595 | 1680 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single Ended) | 2135 | | 2420 | 2135 | | 2420 | 2135 | | 2420 | mV |
| $V_{IL}$ | Input LOW Voltage (Single Ended) | 1490 | | 1825 | 1490 | | 1825 | 1490 | | 1825 | mV |
| $V_{BB}$ | Output Voltage Reference | 1.92 | | 2.04 | 1.92 | | 2.04 | 1.92 | | 2.04 | V |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential) (Note 3.)<br>Vpp < 500 mV<br>Vpp ≧ 500 mV | <br>1.3<br>1.6 | | <br>2.9<br>2.9 | <br>1.2<br>1.5 | | <br>2.9<br>2.9 | <br>1.2<br>1.5 | | <br>2.9<br>2.9 | <br>V<br>V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current Others<br>$\overline{CLK0}$, $\overline{CLK1}$ | 0.5<br>–300 | | | 0.5<br>–300 | | | 0.5<br>–300 | | | μA<br>μA |

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to $V_{CC}$–2 volts.
3. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, max varies 1:1 with $V_{CC}$. $V_{IHCMR}$ is defined as the range within which the $V_{IH}$ level may vary, with the device still meeting the propagation delay specification. The $V_{IL}$ level must be such that the peak to peak voltage is less than 1.0 V and greater than or equal to $V_{PP}$(min).

**LVNECL DC CHARACTERISTICS** $V_{CC}$= 0.0 V; $V_{EE}$= –3.3 V (Note 1.)

| | | –40°C | | | 25°C | | | 85°C | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Characteristic** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| $I_{EE}$ | Power Supply Current | | 122 | 136 | | 122 | 136 | | 125 | 139 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 2.) | –1085 | –1005 | –880 | –1025 | –955 | –880 | –1025 | –955 | –880 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 2.) | –1830 | –1695 | –1555 | –1810 | –1705 | –1620 | –1810 | –1705 | –1620 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single Ended) | –1165 | | –880 | –1165 | | –880 | –1165 | | –880 | mV |
| $V_{IL}$ | Input LOW Voltage (Single Ended) | –1810 | | –1475 | –1810 | | –1475 | –1810 | | –1475 | mV |
| $V_{BB}$ | Output Voltage Reference | –1.38 | | –1.26 | –1.38 | | –1.26 | –1.38 | | –1.26 | V |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential) (Note 3.)<br>Vpp < 500 mV<br>Vpp ≧ 500 mV | <br>–2.0<br>–1.7 | | <br>–0.4<br>–0.4 | <br>–2.1<br>–1.8 | | <br>–0.4<br>–0.4 | <br>–2.1<br>–1.8 | | <br>–0.4<br>–0.4 | <br>V<br>V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current Others<br>$\overline{CLK0}$, $\overline{CLK1}$ | 0.5<br>–300 | | | 0.5<br>–300 | | | 0.5<br>–300 | | | μA<br>μA |

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to $V_{CC}$–2 volts.
3. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, max varies 1:1 with $V_{CC}$. $V_{IHCMR}$ is defined as the range within which the $V_{IH}$ level may vary, with the device still meeting the propagation delay specification. The $V_{IL}$ level must be such that the peak to peak voltage is less than 1.0 V and greater than or equal to $V_{PP}$(min).

**AC CHARACTERISTICS** $V_{CC}$= 3.3 V; $V_{EE}$= 0.0 V or $V_{CC}$= 0.0 V; $V_{EE}$= –3.3 V (Note 1.)

| Symbol | Characteristic | –40°C | | | 25°C | | | 70°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{max}$ | Maximum Toggle Frequency | | TBD | | | TBD | | | TBD | | GHz |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay to Output<br>IN (differential) (Note 2.)<br>IN (single–ended) (Note 3.)<br>MR | <br>1040<br>990<br>1100 | <br>1140<br>1140<br>1250 | <br>1240<br>1290<br>1400 | <br>1080<br>1030<br>1170 | <br>1180<br>1180<br>1320 | <br>1280<br>1330<br>1470 | <br>1120<br>1070<br>1220 | <br>1220<br>1220<br>1370 | <br>1320<br>1370<br>1520 | ps |
| $t_{skew}$ | Within–Device Skew (Note 4.)<br>Part–to–Part Skew (Diff) | | | 50<br>200 | | | 50<br>200 | | | 50<br>200 | ps |
| $t_{JITTER}$ | Cycle–to–Cycle Jitter | | TBD | | | TBD | | | TBD | | ps |
| $V_{PP}$ | Input Swing (Note 5.) | 400 | | 1000 | 400 | | 1000 | 400 | | 1000 | mV |
| $t_r/t_f$ | Output Rise/Fall Time 20%–80% | 200 | | 600 | 200 | | 600 | 200 | | 600 | ps |

1. $V_{EE}$ can vary ±0.3 V.
2. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals.
3. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal.
4. The within–device skew is defined as the worst case difference between any two similar delay paths within a single device.
5. $V_{PP}$(min) is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The $V_{PP}$(min) is AC limited for the LVE222. A differential input as low as 50 mV will still produce full ECL levels at the output.

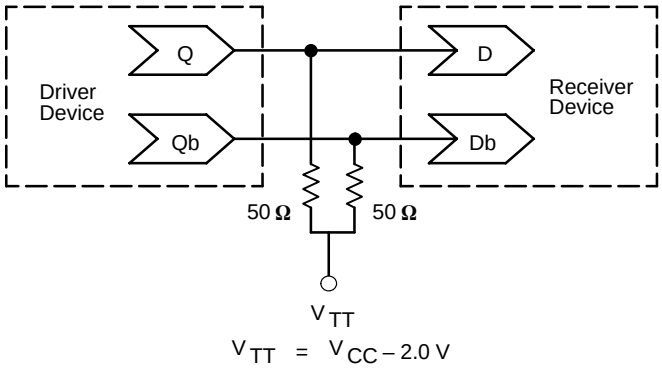



**Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)**

## Resource Reference of Application Notes

**AN1404** – ECLinPS Circuit Performance at Non–Standard $V_{IH}$ Levels

**AN1405** – ECL Clock Distribution Techniques

**AN1406** – Designing with PECL (ECL at +5.0 V)

**AN1503** – ECLinPS I/O SPICE Modeling Kit

**AN1504** – Metastability and the ECLinPS Family

**AN1560** – Low Voltage ECLinPS SPICE Modeling Kit

**AN1568** – Interfacing Between LVDS and ECL

**AN1596** – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit

**AN1650** – Using Wire–OR Ties in ECLinPS Designs

**AN1672** – The ECL Translator Guide

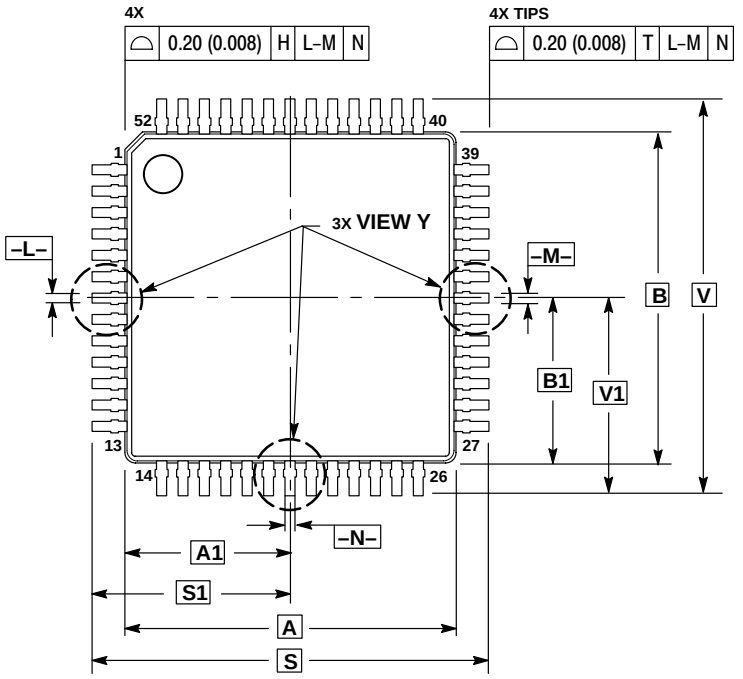
**AND8001** – Odd Number Counters Design

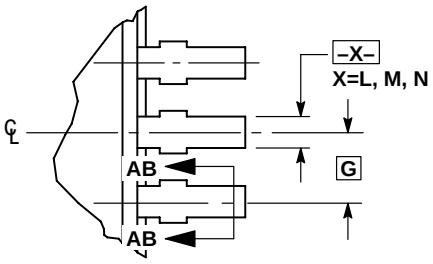
**AND8002** – Marking and Date Codes

**AND8020** – Termination of ECL Logic Devices

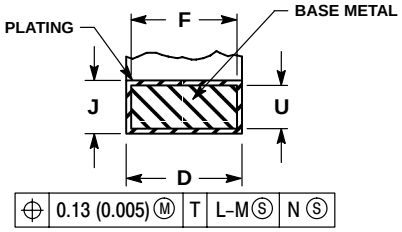
## PACKAGE DIMENSIONS

**FA SUFFIX**
TQFP PACKAGE
CASE 848D–03
ISSUE C

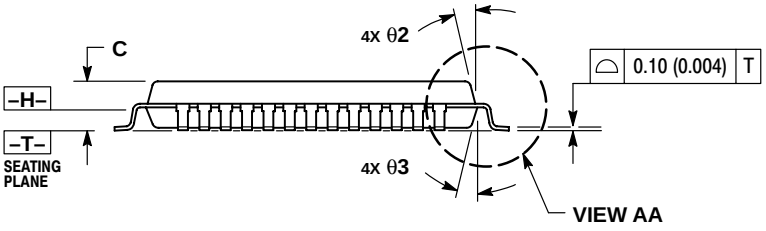


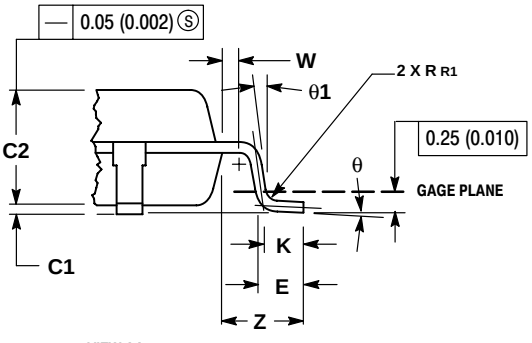




VIEW Y




SECTION AB–AB
ROTATED 90° CLOCKWISE




VIEW AA

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –L–, –M– AND –N– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –T–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 (0.018). MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 (0.003).

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 10.00 BSC | | 0.394 BSC | |
| A1 | 5.00 BSC | | 0.197 BSC | |
| B | 10.00 BSC | | 0.394 BSC | |
| B1 | 5.00 BSC | | 0.197 BSC | |
| C | --- | 1.70 | --- | 0.067 |
| C1 | 0.05 | 0.20 | 0.002 | 0.008 |
| C2 | 1.30 | 1.50 | 0.051 | 0.059 |
| D | 0.20 | 0.40 | 0.008 | 0.016 |
| E | 0.45 | 0.75 | 0.018 | 0.030 |
| F | 0.22 | 0.35 | 0.009 | 0.014 |
| G | 0.65 BSC | | 0.026 BSC | |
| J | 0.07 | 0.20 | 0.003 | 0.008 |
| K | 0.50 REF | | 0.020 REF | |
| R1 | 0.08 | 0.20 | 0.003 | 0.008 |
| S | 12.00 BSC | | 0.472 BSC | |
| S1 | 6.00 BSC | | 0.236 BSC | |
| U | 0.09 | 0.16 | 0.004 | 0.006 |
| V | 12.00 BSC | | 0.472 BSC | |
| V1 | 6.00 BSC | | 0.236 BSC | |
| W | 0.20 REF | | 0.008 REF | |
| Z | 1.00 REF | | 0.039 REF | |
| θ | 0° | 7° | 0° | 7° |
| θ1 | 0° | --- | 0° | --- |
| θ2 | 12° REF | | 12° REF | |
| θ3 | 5° | 13° | 5° | 13° |

# Notes

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