

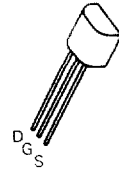
N-CHANNEL ENHANCEMENT MODE VERTICAL DMOS FET

2N7000P

ISSUE 2 – MARCH 94

FEATURES

- * 60 Volt V_{CEO}
- * $R_{DS(on)} = 5 \Omega$



E-Line
TO92 Compatible

ABSOLUTE MAXIMUM RATINGS.

| PARAMETER | SYMBOL | VALUE | UNIT |
|---|----------------|-------------|-------------|
| Drain-Source Voltage | V_{DS} | 60 | V |
| Continuous Drain Current at $T_{amb}=25^{\circ}C$ | I_D | 200 | mA |
| Pulsed Drain Current | I_{DM} | 500 | mA |
| Gate-Source Voltage | V_{GS} | ± 40 | V |
| Power Dissipation at $T_{amb}=25^{\circ}C$ | P_{tot} | 400 | mW |
| Operating and Storage Temperature Range | $T_j; T_{stg}$ | -55 to +150 | $^{\circ}C$ |

ELECTRICAL CHARACTERISTICS (at $T_{amb} = 25^{\circ}C$ unless otherwise stated).

| PARAMETER | SYMBOL | MIN. | MAX. | UNIT | CONDITIONS. |
|---|--------------|------|------------|---------------|--|
| Drain-Source Breakdown Voltage | BV_{DSS} | 60 | | V | $I_D=10\mu A, V_{GS}=0V$ |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | 0.8 | 3 | V | $I_D=1mA, V_{DS}=V_{GS}$ |
| Gate-Body Leakage | I_{GSS} | | 10 | nA | $V_{GS}=\pm 15V, V_{DS}=0V$ |
| Zero Gate Voltage Drain Current | I_{DSS} | | 1 1 | μA mA | $V_{DS}=48V, V_{GS}=0$ $V_{DS}=48V, V_{GS}=0V, T=125^{\circ}C(2)$ |
| On-State Drain Current(1) | $I_{D(on)}$ | 75 | | mA | $V_{DS}=10V, V_{GS}=4.5V$ |
| Static Drain-Source On-State Voltage (1) | $V_{DS(on)}$ | | 2.5 0.4 | V V | $V_{GS}=10V, I_D=500mA$ $V_{GS}=4.5V, I_D=75mA$ |
| Static Drain-Source On-State Resistance (1) | $R_{DS(on)}$ | | 5 | Ω | $V_{GS}=10V, I_D=500mA$ |
| Forward Transconductance(1)(2) | g_{fs} | 100 | | mS | $V_{DS}=10V, I_D=200mA$ |
| Input Capacitance (2) | C_{iss} | | 60 | pF | $V_{DS}=25V, V_{GS}=0V, f=1MHz$ |
| Common Source Output Capacitance (2) | C_{oss} | | 25 | pF | |
| Reverse Transfer Capacitance (2) | C_{rss} | | 5 | pF | |
| Turn-On Time (2)(3) | $t_{(on)}$ | | 10 | ns | $V_{DD}=15V, I_D=500mA$ $R_g=25\Omega, R_L=25\Omega$ |
| Turn-Off Time (2)(3) | $t_{(off)}$ | | 10 | ns | |

- (1) Measured under pulsed conditions. Width=300 μs . Duty cycle $\leq 2\%$ (2) Sample test.
 (3) Switching times measured with 50 Ω source impedance and <5ns rise time on a pulse generator