# **Quint Differential Line Receiver**

The MC10E416/100E416 is a 5-bit differential line receiving device. The 2.0GHz of bandwidth provided by the high frequency outputs makes the device ideal for buffering of very high speed oscillators.

A  $V_{BB}$  pin is available to AC couple an input signal to the device. More information on AC coupling can be found in the design handbook section of this data book.

The design incorporates two stages of gain, internal to the device, making it an excellent choice for use in high bandwidth amplifier applications.

The differential inputs have internal clamp structures which will force the Q output of a gate in an open input condition to go to a LOW state. Thus, inputs of unused gates can be left open and will not affect the operation of the rest of the device. Note that the input clamp will take affect only if both inputs fall 2.5V below  $V_{CC}$ .

- Differential D and Q; VBB available
- 600ps Max. Propagation Delay
- High Frequency Outputs
- · 2 Stages of Gain
- Extended 100E V<sub>EE</sub> Range of 4.2V to 5.46V
- Internal 75kΩ Input Pulldown Resistors

#### Pinout: 28-Lead PLCC (Top View) VCCO Vcco $Q_4$ 20 18 $Q_3$ $D_2$ $Q_3$ $D_2$ 28 16 VCC 1 15 $Q_2$ VEE 14 $V_{BB}$ 2 Q2 $D_0$ 3 13 | V<sub>CCO</sub> $D_0$ 12 ∏ Q<sub>1</sub> 10 $D_1$ $Q_0$ $Q_0$ Vcco **VCCO**

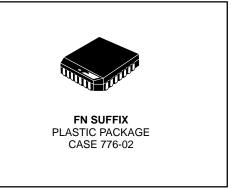
 $^{\star}$  All VCC and VCCO pins are tied together on the die.

#### **PIN NAMES**

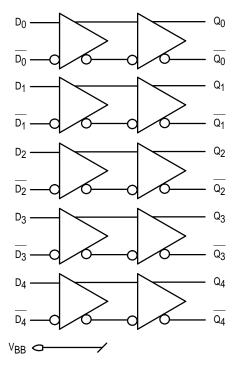
Pin	Function
D[0:4], D[0:4]	Differential Data Inputs
Q[0:4], Q[0:4]	Differential Data Outputs

### MC10E416 MC100E416

## QUINT DIFFERENTIAL LINE RECEIVER



#### **LOGIC DIAGRAM**



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#### **DC CHARACTERISTICS** (VEE = VEE(min) to VEE(max); VCC = VCCO = GND)

		0°C			25°C			85°C				
Symbol	Characteristic	min	typ	max	min	typ	max	min	typ	max	Unit	Condition
V <sub>BB</sub>	Output Reference Voltage										V	
	10E	-1.38		-1.27	-1.35		-1.25	-1.31		-1.19		
	100E	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26		
lн	Input HIGH Current			150			150			150	μΑ	
IEE	Power Supply Current										mA	
	10E		135	162		135	162	1	135	162		
	100E		135	162		135	162		155	186		
V <sub>PP</sub> (DC)	Input Sensitivity	50			50			50			mV	1
VCMR	Common Mode Range	-1.5		0	-1.5		0	-1.5		0	V	2

#### **AC CHARACTERISTICS** ( $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$ ; $V_{CC} = V_{CCO} = GND$ )

		0°C			25°C			85°C				
Symbol	Characteristic	min	typ	max	min	typ	max	min	typ	max	Unit	Condition
<sup>t</sup> PLH <sup>t</sup> PHL	Propagation Delay to Output d(Diff) D(SE)	250 200	350 350	500 550	250 200	350 350	500 550	250 200	350 350	500 550	ps	
tSKEW	Within-Device Skew		50			50			50		ps	1
tSKEW	Duty Cycle Skew  tPLH-tPHL		±10			±10			±10		ps	2
V <sub>PP</sub> (AC)	Minimum Input Swing	150			150			150			mV	3
t <sub>r</sub> t <sub>f</sub>	Rise/Fall Time 20 - 80%	100	200	350	100	200	350	100	200	350	ps	

<sup>1.</sup> Within-device skew is defined as identical transitions on similar paths through a device.

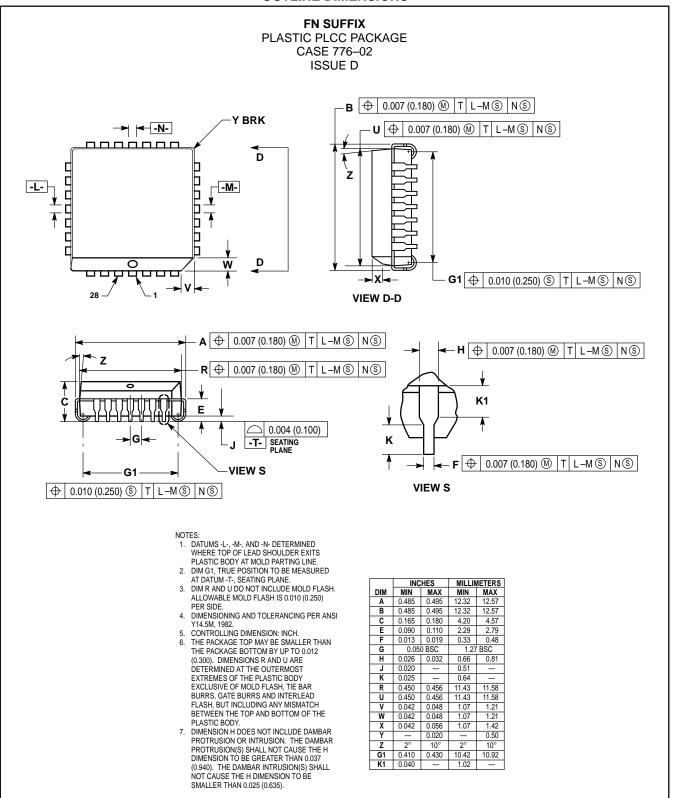
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Differential input voltage required to obtain a full ECL swing on the outputs.
 V<sub>CMR</sub> is referenced to the most positive side of the differential input signal. Normal operation is obtained when the input signal are within the VCMR range and the input swing is greater than VPP MIN and < 1.0V

<sup>2.</sup> Duty cycle skew defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

<sup>3.</sup> Minimum input swing for which AC parameters are guaranteed.

#### **OUTLINE DIMENSIONS**



#### MC10E416 MC100E416

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