National Semiconductor

December 1994

54F/74F646 • 74F646B • 54F/74F648
Octal Transceiver/Register with TRI-STATE® Outputs

General Description

These devices consist of bus transceiver circuits with TRI-STATE, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a high logic level. Control $\overline{G}$ and direction pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or the B register or in both. The select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the enable control $\overline{G}$ is Active LOW. In the isolation mode (control $\overline{G}$ HIGH), A data may be stored in the B register and/or B data may be stored in the A register.

Features

- Independent registers for A and B buses
- Multiplexed real-time and stored data
- 'F648 has inverting data paths
- 'F646/'F646B have non-inverting data paths
- 'F646B is a faster version of the 'F646
- TRI-STATE outputs
- 300 mil slim DIP
- Guaranteed 4000V minimum ESD protection

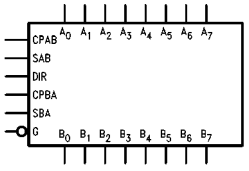
Commercial	Military	Package Number	Package Description
74F646SPC		N24C	24-Lead (0.300″ Wide) Molded Dual-In-Line
	54F646DM (Note 2)	J24F	24-Lead (0.300″ Wide) Ceramic Dual-In-Line
74F646SC (Note 1)		M24B	24-Lead (0.300″ Wide) Molded Small Outline, JEDEC
74F646MSA (Note 1)		MSA24	24-Lead Molded Shrink Small Outline, EIAJ, Type II
	54F646FM (Note 2)	W24C	24-Lead Cerpack
	54F646LM (Note 2)	E28A	28-Lead Ceramic Leadless Chip Carrier, Type C
74F646BSPC		N24C	24-Lead (0.300″ Wide) Molded Dual-In-Line
74F646BSC (Note 1)		M24B	24-Lead (0.300″ Wide) Molded Small Outline, JEDEC
74F648SPC		N24C	24-Lead (0.300″ Wide) Molded Dual-In-Line
	54F648SDM (Note 2)	J24F	24-Lead (0.300″ Wide) Ceramic Dual-In-Line
74F648SC (Note 1)		M24B	24-Lead (0.300″ Wide) Molded Small Outline, JEDEC
	54F648FM (Note 2)	W24C	24-Lead Cerpack
	54F648LM (Note 2)	E28A	24-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13″ reel. Use suffix = SCX.

Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

Logic Symbols

'F646/'F646B



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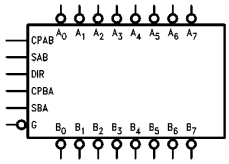
'F648



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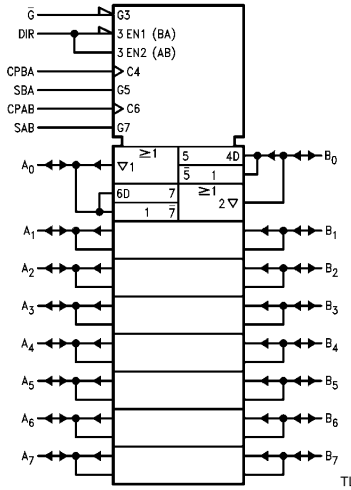
 TL/F/9580

RRD-B30M75/Printed in U. S. A.

54F/74F646 • 74F646B • 54F/74F648 Octal Transceiver/Register with TRI-STATE Outputs

Logic Symbols (Continued)

IEEE/IEC
'F646/'F646B



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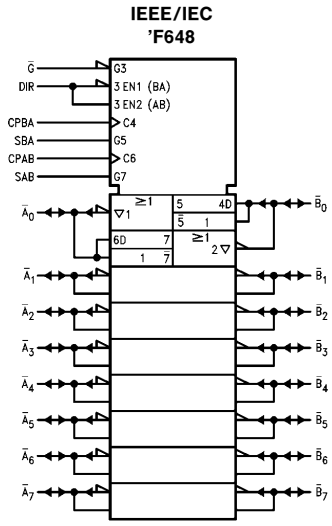
IEEE/IEC
'F648



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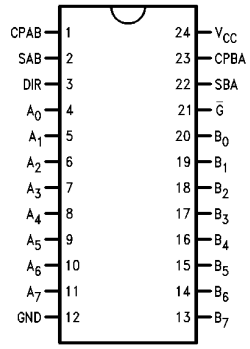
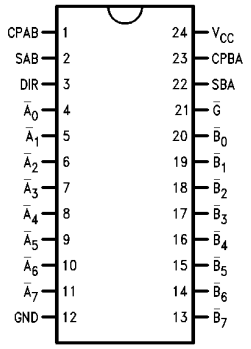
Connection Diagrams

Pin Assignment
for DIP, SOIC and Flatpak
'F646/'F646B



TL/F/9580–2

Pin Assignment
for DIP, SOIC and Flatpak
'F648



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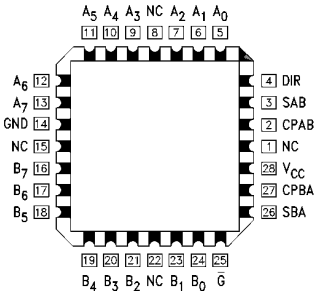
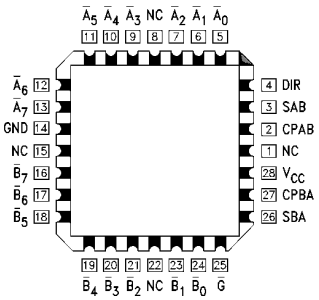
Pin Assignment
for LCC
'F646/'F646B



TL/F/9580–3

Pin Assignment
for LCC
'F648



TL/F/9580–10

Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
A_0-A_7	Data Register A Inputs/	3.5/1.083	70 μA/ -650 μA
	TRI-STATE Outputs	600/106.6 (80)	-12 mA/64 mA (48 mA)
B_0-B_7	Data Register B Inputs/	3.5/1.083	70 μA/ -650 μA
	TRI-STATE Outputs	600/106.6 (80)	-12 mA/64 mA (48 mA)
CPAB, CPBA	Clock Pulse Inputs	1.0/1.0	20 μA/ -0.6 mA
SAB, SBA	Select Inputs	1.0/1.0	20 μA/ -0.6 mA
$\overline{G}$	Output Enable Input	1.0/1.0	20 μA/ -0.6 mA
DIR	Direction Control Input	1.0/1.0	20 μA/ -0.6 mA

Function Table

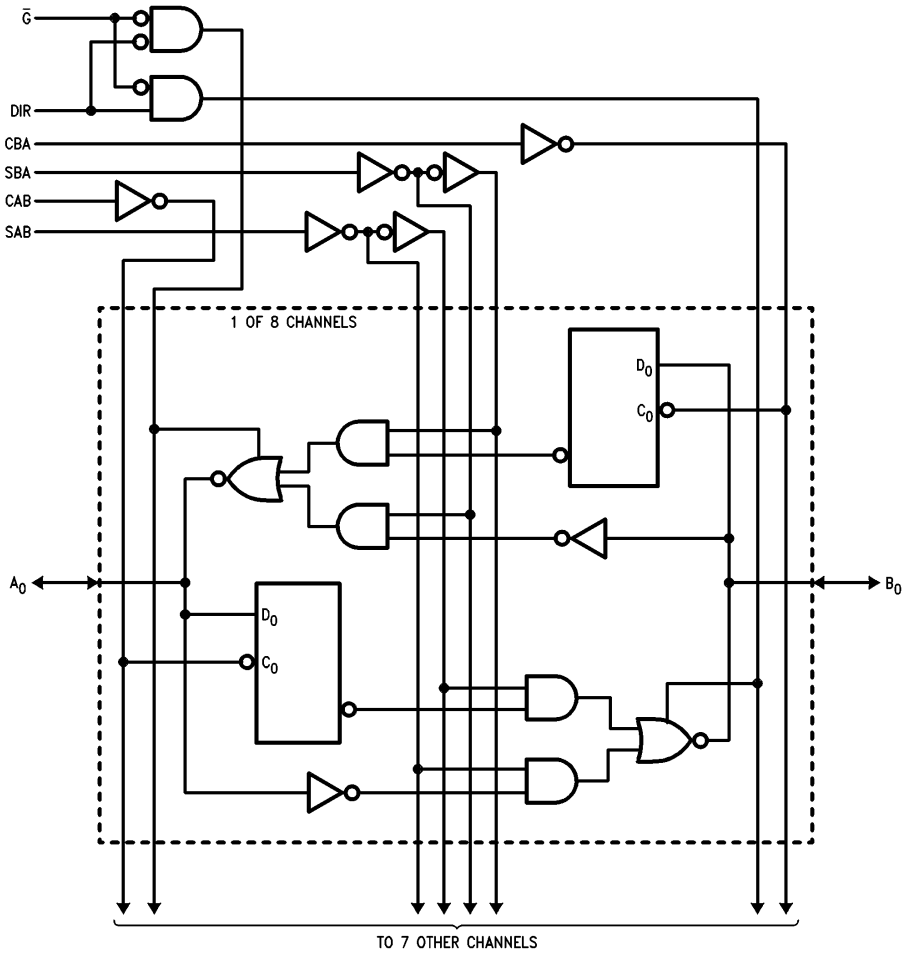
Inputs						Data I/O*		Function
$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	A_0-A_7	B_0-B_7	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	↗	X	X	X			Clock A_n Data into A Register
H	X	X	↗	X	X			Clock B_n Data into B Register
L	H	X	X	L	X	Input	Output	A_n to B_n—Real Time (Transparent Mode)
L	H	↗	X	L	X			Clock A_n Data into A Register
L	H	H or L	X	H	X			A Register to B_n (Stored Mode)
L	H	↗	X	H	X			Clock A_n Data into A Register and Output to B_n
L	L	X	X	X	L	Output	Input	B_n to A_n—Real Time (Transparent Mode)
L	L	X	↗	X	L			Clock B_n Data into B Register
L	L	X	H or L	X	H			B Register to A_n (Stored Mode)
L	L	X	↗	X	H			Clock B_n Data into B Register and Output to A_n

*The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR Inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the clock inputs.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Irrelevant
↗ = LOW-to-HIGH Transition

Logic Diagrams (Continued)

'F646/'F646B



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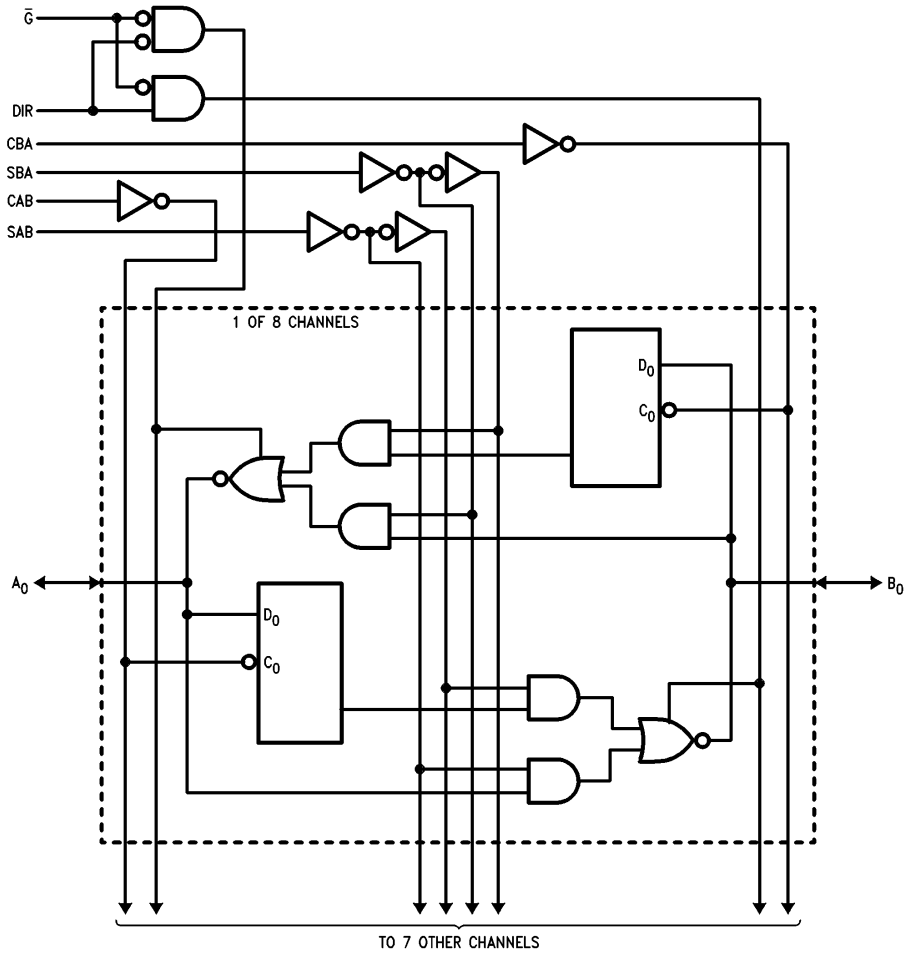
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Logic Diagrams (Continued)

'F648



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		54F/74F			Units	V_{CC}	Conditions
			Min	Typ	Max			
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA (Non I/O Pins)
V_{OH}	Output HIGH Voltage	54F 10% V_{CC} 74F 10% V_{CC}	2.0 2.0			V	Min	I_{OH} = −12 mA (A_n, B_n) I_{OH} = −15 mA (A_n, B_n)
V_{OL}	Output LOW Voltage	54F 10% V_{CC} 74F 10% V_{CC}			0.55 0.55	V	Min	I_{OL} = 48 mA (A_n, B_n) I_{OL} = 64 mA (A_n, B_n)
I_{IH}	Input HIGH Current	54F 74F			20.0 5.0	μA	Max	V_{IN} = 2.7V (Non I/O Pins)
I_{BVI}	Input HIGH Current Breakdown Test	54F 74F			100 7.0	μA	Max	V_{IN} = 7.0V (Non I/O Pins)
I_{BVIT}	Input HIGH Current Breakdown (I/O)	54F 74F			1.0 0.5	mA	Max	V_{IN} = 5.5V (A_n, B_n)
I_{CEX}	Output HIGH Leakage Current	54F 74F			250 50	μA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V (Non I/O Pins)
I_{IH} + I_{OZH}	Output Leakage Current				70	μA	Max	V_{OUT} = 2.7V (A_n, B_n)
I_{IL} + I_{OZL}	Output Leakage Current				−650	μA	Max	V_{OUT} = 0.5V (A_n, B_n)
I_{OS}	Output Short-Circuit Current		−100		−225	mA	Max	V_{OUT} = 0V
I_{ZZ}	Bus Drainage Test				500	μA	0.0V	V_{OUT} = 5.25V
I_{CCH}	Power Supply Current				135	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current				150	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current				150	mA	Max	V_O = HIGH Z

’F646/’F648

AC Electrical Characteristics

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF		54F T_A, V_{CC} = Mil $C_L = 50$ pF		74F T_A, V_{CC} = Com $C_L = 50$ pF		Units
		Min	Max	Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	90		75		90		MHz
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus	2.0 2.0	7.0 8.0	2.0 2.0	8.5 9.5	2.0 2.0	8.0 9.0	ns
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus (’F646)	1.0 1.0	7.0 6.5	1.0 1.0	8.0 8.0	1.0 1.0	7.5 7.0	ns
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus (’F648)	2.0 1.0	8.5 7.5	1.0 1.0	10.0 9.0	2.0 1.0	9.0 8.0	ns
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to A or B	2.0 2.0	8.5 8.0	2.0 2.0	11.0 10.0	2.0 2.0	9.5 9.0	ns
t_{PZH} t_{PZL}	Enable Time $\overline{OE}$ to A or B	2.0 2.0	8.5 12.0	2.0 2.0	10.0 13.5	2.0 2.0	9.0 12.5	ns
t_{PHZ} t_{PLZ}	Disable Time $\overline{OE}$ to A or B	1.0 2.0	7.5 9.0	1.0 2.0	9.0 11.0	1.0 2.0	8.5 9.5	ns
t_{PZH} t_{PZL}	Enable Time DIR to A or B	2.0 2.0	14.0 13.0	2.0 2.0	16.0 15.0	2.0 2.0	15.0 14.0	ns
t_{PHZ} t_{PLZ}	Disable Time DIR to A or B	1.0 2.0	9.0 11.0	1.0 2.0	10.0 12.0	1.0 2.0	9.5 11.5	ns

’F646/’F648

AC Operating Requirements

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$		54F T_A, V_{CC} = Mil		74F T_A, V_{CC} = Com		Units
		Min	Max	Min	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW Bus to Clock	5.0 5.0		5.0 5.0		5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW Bus to Clock	2.0 2.0		2.5 2.5		2.0 2.0		ns
$t_w(H)$ $t_w(L)$	Clock Pulse Width HIGH or LOW	5.0 5.0		5.0 5.0		5.0 5.0		ns

'F646B

AC Electrical Characteristics

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50\ pF$		54F $T_A, V_{CC} = Mil$ $C_L = 50\ pF$		74F $T_A, V_{CC} = Com$ $C_L = 50\ pF$		Units
		Min	Max	Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	165				150		MHz
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus	2.5 3.0	7.0 7.5			2.5 3.0	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	2.0 2.0	6.0 6.0			2.0 2.0	7.0 7.0	ns
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to A or B	2.5 2.5	7.5 7.5			2.5 2.5	8.5 8.5	ns
t_{PZH} t_{PZL}	Enable Time $\overline{OE}$ to A or B	2.5 2.5	6.5 9.0			2.5 2.5	8.0 10.0	ns
t_{PHZ} t_{PLZ}	Disable Time $\overline{OE}$ to A or B	1.5 2.0	6.5 7.0			1.5 2.0	7.5 8.5	ns
t_{PZH} t_{PZL}	Enable Time DIR to A or B	2.0 3.0	7.0 9.5			2.0 3.0	8.5 10.0	ns
t_{PHZ} t_{PLZ}	Disable Time DIR to A or B	1.5 2.5	7.5 8.5			1.5 2.5	8.5 9.5	ns

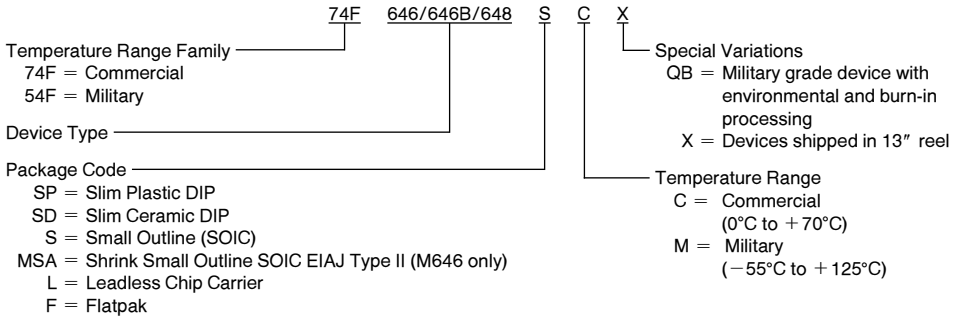
'F646B

AC Operating Requirements

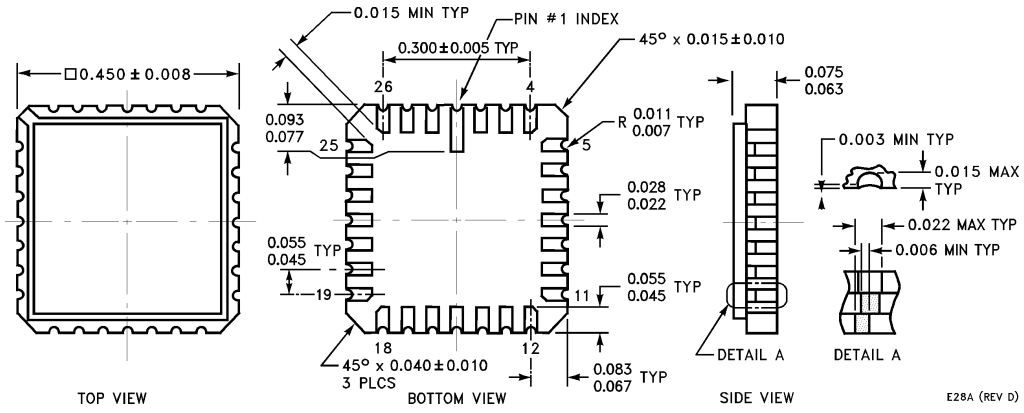
Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$		54F $T_A, V_{CC} = Mil$		74F $T_A, V_{CC} = Com$		Units
		Min	Max	Min	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW Bus to Clock	5.0 5.0				4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW Bus to Clock	1.5 1.5				1.5 1.5		ns
$t_w(H)$ $t_w(L)$	Clock Pulse Width HIGH or LOW	5.0 5.0				5.0 5.0		ns

Ordering Information

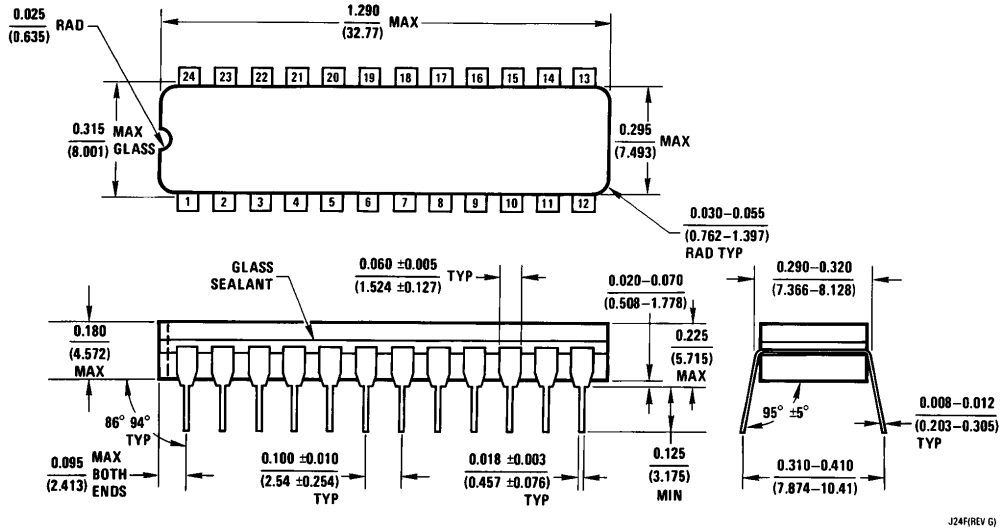
The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



Physical Dimensions inches (millimeters)

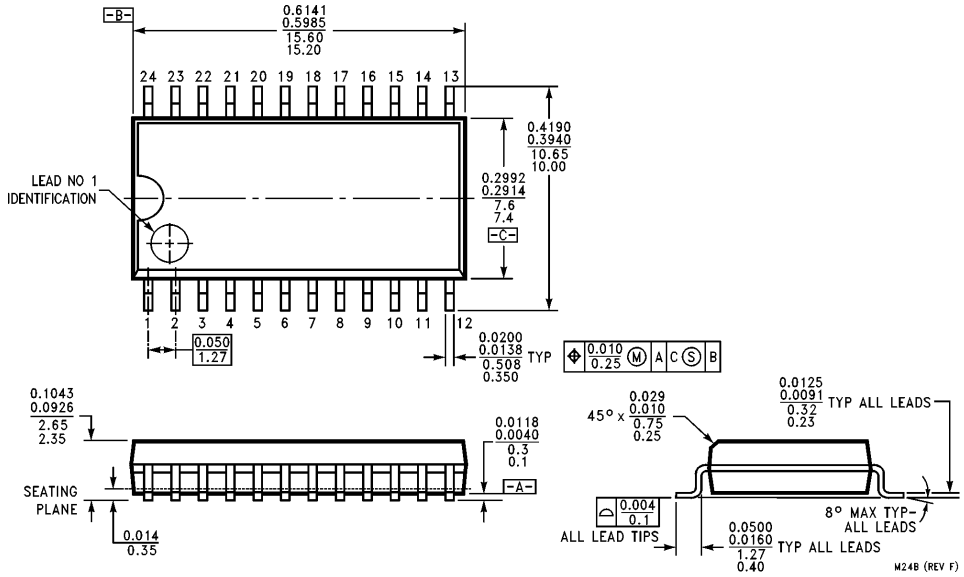


28-Lead Ceramic Leadless Chip Carrier, Type C
NS Package Number E28A



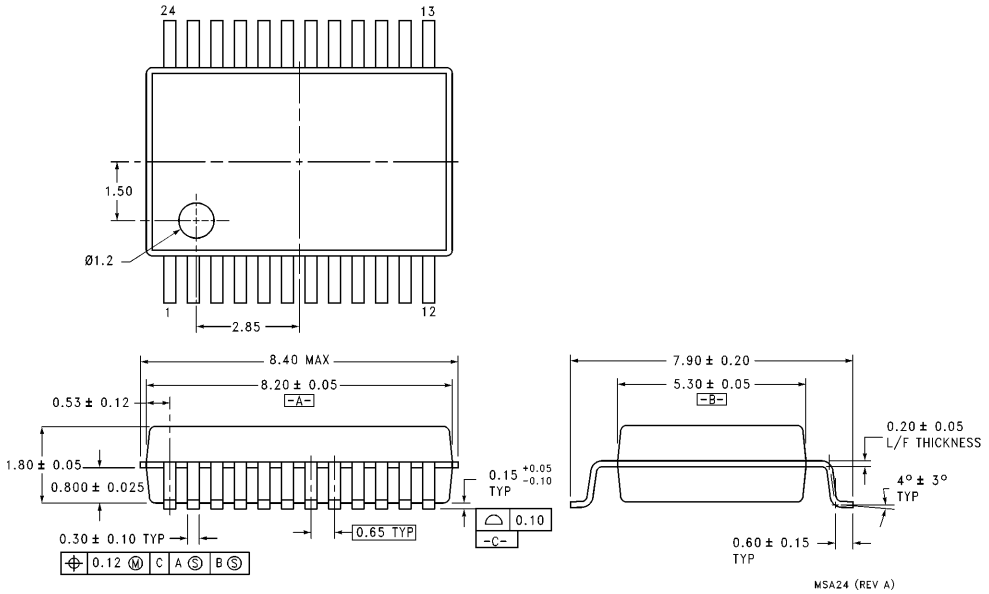
24-Lead (0.300″ Wide) Ceramic Dual-In-Line Package (SD)
NS Package Number J24F

Physical Dimensions inches (millimeters) (Continued)

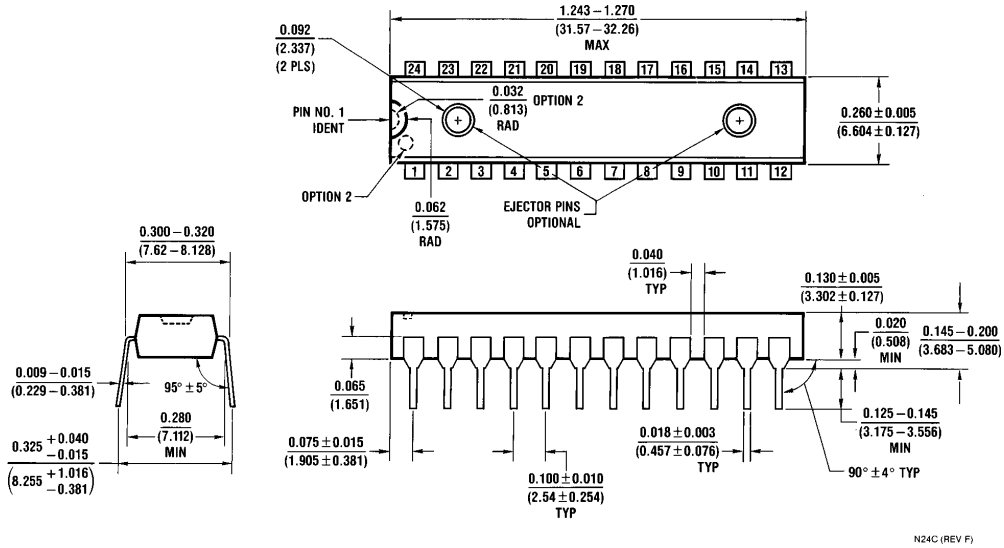


24-Lead (0.300″ Wide) Molded Small Outline Package, JEDEC (S)
NS Package Number M24B

Physical Dimensions inches (millimeters) (Continued)

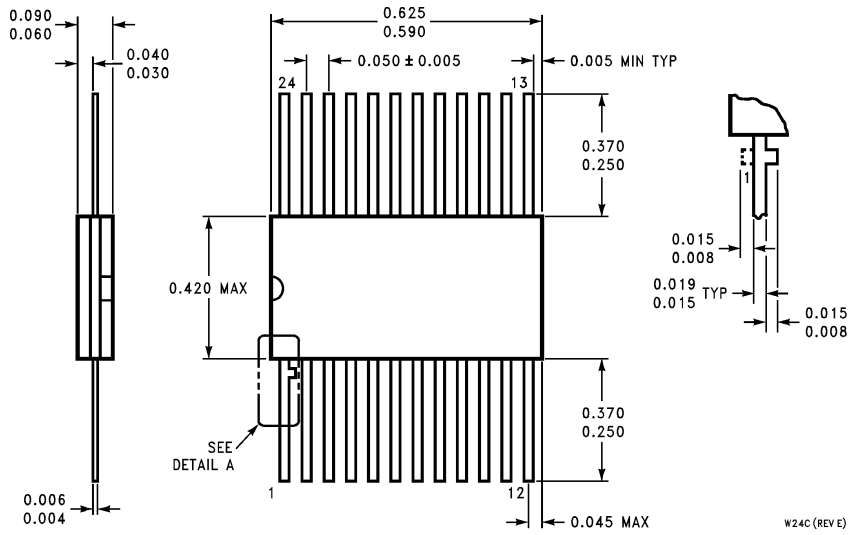


24-Lead Molded Shrink Small Outline Package, EIAJ, Type II
NS Package Number MSA24



24-Lead (0.300″ Wide) Molded Dual-In-Line Package (SP)
NS Package Number N24C

Physical Dimensions inches (millimeters) (Continued)



24-Lead Cerpack
NS Package Number W24C

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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