HT9170 Series
Tone Receiver

Features

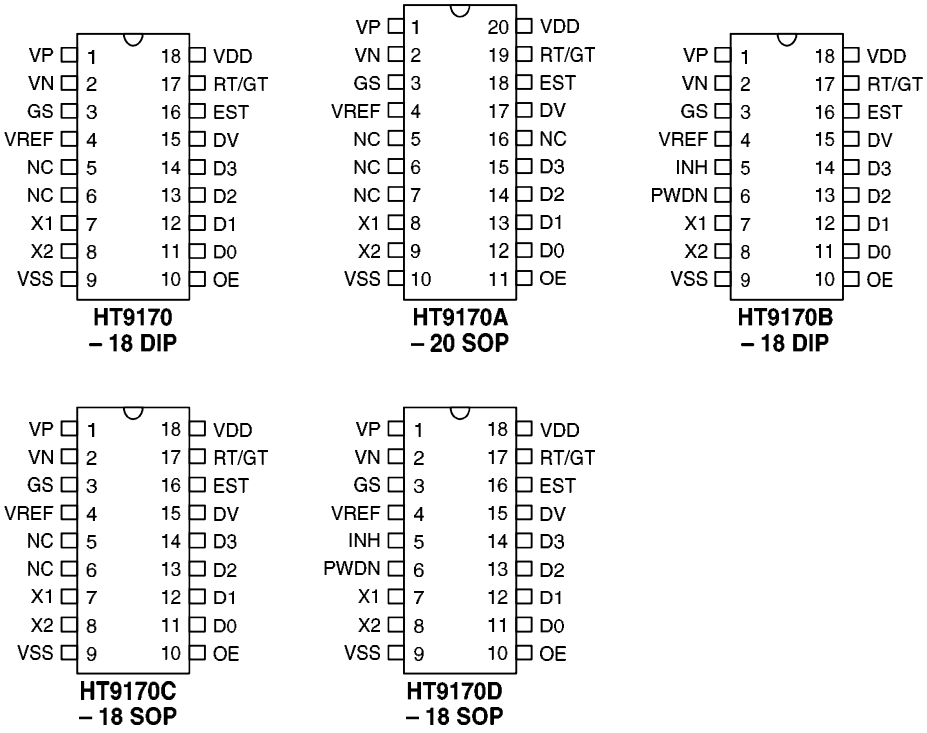
- Operating voltage: 2.5V~5.5V
- Minimal external components
- No external filter is required
- Low standby current (Power-down mode)
- Excellent performance
- Tri-state data output for μC interface use
- 3.58MHz crystal or ceramic resonator
- 1633Hz can be inhibited by INH pin

General Description

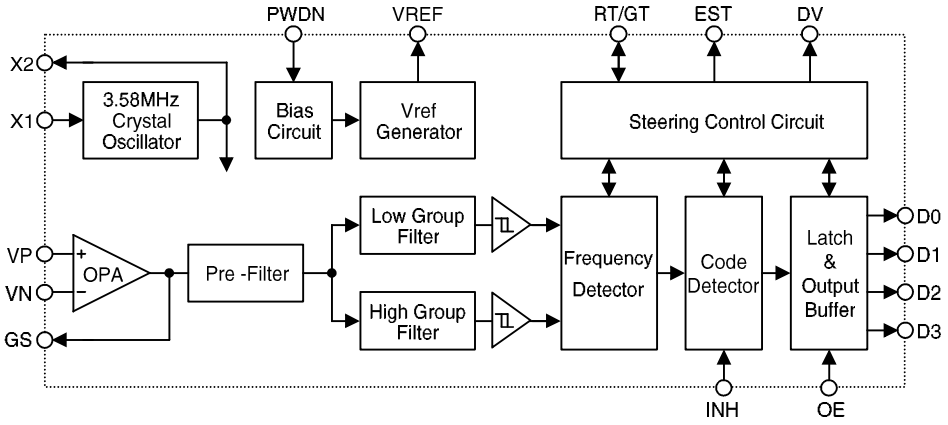
The HT9170 series are Dual Tone Multi Frequency (DTMF) receivers integrated with digital decoder and bandsplit filter functions. The HT9170B and HT9170D types supply power-down mode and inhibit mode operations. All types of the HT9170 series use digital counting techniques to detect and decode all the 16 DTMF tone pairs into a 4-bit code output.

While the high-accuracy switched capacitor filters are employed to divide tone (DTMF) signal into low and high group signals. A built-in dial tone rejection circuit is provided to eliminate the need for pre-filtering.

Pin Assignment



Block Diagram

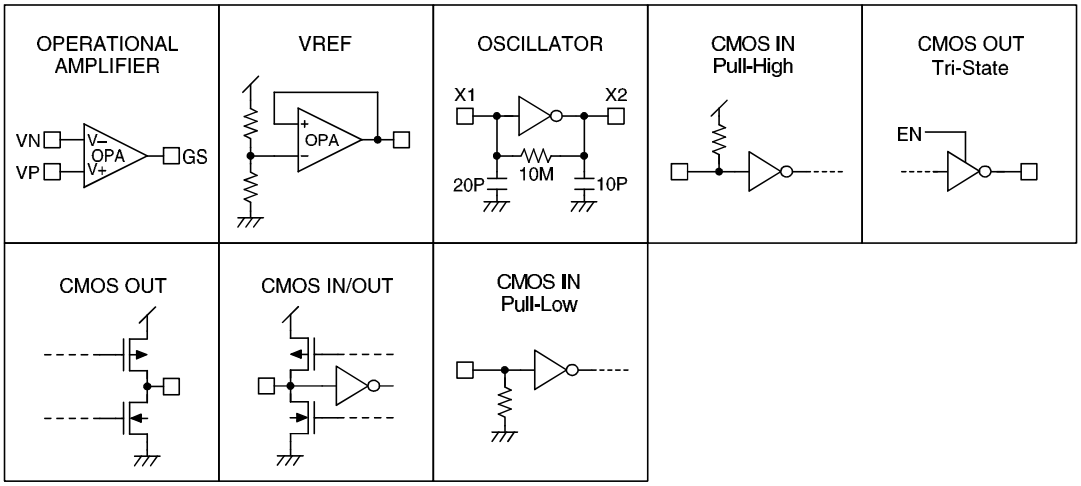


Pin Description

Pin Name	I/O	Internal Connection	Description
VP	I	OPERATIONAL AMPLIFIER	Non-inverting input of operational amplifier
VN	I		Inverting input of operational amplifier
GS	O		Output terminal of operational amplifier
VREF	O	VREF	Reference voltage output, normally VDD/2
X1	I	OSCILLATOR	The system oscillator consists of an inverter, a bias resistor and the necessary load capacitor on chip. Connecting a standard 3.579545MHz crystal to X1 and X2 terminals can implement the oscillator function.
X2	O		
PWDN	I	CMOS IN Pull-Low	Logic high, power down the device and inhibits the oscillator. This pin is internally pulled down.
INH	I	CMOS IN Pull-Low	Logic high inhibits the detection of tones representing characters A, B, C and D. This pin input is internally pulled down.
VSS	I	—	Negative power supply
OE	I	CMOS IN Pull-High	D0~D3 output enable, high active
D0~D3	O	CMOS OUT Tri-State	Output terminals of receiving data OE="H": Output enable OE="L": High impedance

Pin Name	I/O	Internal Connection	Description
DV	O	CMOS OUT	Data valid output When the chip receives a valid tone (DTMF) signal the DV goes high; otherwise the DV remains low.
EST	O	CMOS OUT	Early steering output (see Functional Description)
RT/GT	I/O	CMOS IN/OUT	Tone acquisition time and release time can be set through connection with external resistor and capacitor.
VDD	I	—	Positive power supply, 2.5V~5.5V for normal operation

Approximate internal connection circuits



Absolute Maximum Ratings*

Supply Voltage ..... –0.3V to 6V
Input Voltage..... V_{SS}–0.3V to V_{DD}+0.3V
Storage Temperature..... –50°C to 125°C
Operating Temperature..... –20°C to 75°C

*Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extened periods may affect device reliability.

D.C. Characteristics

(Ta=25°C)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operation Voltage	—	—	2.5	5	5.5	V
I_{DD}	Operation Current	5V	—	—	3.0	7	mA
I_{STB}	Standby Current	5V	PWDN=5V	—	10.5	21	μA
V_{IL}	"Low" Input Voltage	5V	—	—	—	1.0	V
V_{IH}	"High" Input Voltage	5V	—	4.0	—	—	V
I_{IL}	"Low" Input Current	5V	V_{VP}=V_{VN}=0V	—	—	0.1	μA
I_{IH}	"High" Input Current	5V	V_{VP}=V_{VN}=5V	—	—	0.1	μA
R_{OE}	Pull-High Resistance (OE)	5V	V_{OE}=0V	60	100	150	kΩ
R_{PD}	Pull-Low Resistance (for Power Down)	5V	—	—	480	—	kΩ
R_{IN}	Input Impedance (VN, VP)	5V	—	—	10	—	MΩ
I_{OH}	Source Current (D0~D3, EST, DV)	5V	V_{OUT}=4.5V	–0.4	–0.8	—	mA
I_{OL}	Sink Current (D0~D3, EST, DV)	5V	V_{OUT}=0.5V	1.0	2.5	—	mA
F_{OSC}	System Frequency	5V	Crystal=3.5795MHz	3.5759	3.5795	3.5831	MHz

A.C. Characteristics: Using Test Circuit of Figure 1.

(Ta=25°C)

Parameter	V_{DD}	Min.	Typ.	Max.	Unit
Input Signal Level	3V	–36	—	–6	dBm
	5V	–29	—	1	
Twist Accept Limit (Positive)	5V	—	10	—	dB
Twist Accept Limit (Negative)	5V	—	10	—	dB
Dial Tone Tolerance	5V	—	18	—	dB
Noise Tolerance	5V	—	–12	—	dB
Third Tone Tolerance	5V	—	–16	—	dB
Frequency Deviation Acception	5V	—	—	±1.5	%
Frequency Deviation Rejection	5V	±3.5	—	—	%
Power Up Time (t_{PU}) (See Figure 4.)	5V	—	30	—	ms

Gain Setting Amplifier Characteristics

(Ta=25°C)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
R_{IN}	Input Resistance	5V	—	—	10	—	MΩ
I_{IN}	Input Leakage Current	5V	$V_{SS}<(V_{VP},V_{VN})<V_{DD}$	—	0.1	—	μA
V_{OS}	Offset Voltage	5V	—	—	±25	—	mV
PSRR	Power Supply Rejection	5V	100 Hz $-3V<V_{IN}<3V$	—	60	—	dB
CMRR	Common Mode Rejection	5V		—	60	—	dB
A_{VO}	Open Loop Gain	5V		—	65	—	dB
f_T	Gain Band Width	5V	—	—	1.5	—	MHz
V_{OUT}	Output Voltage Swing	5V	$R_L>100k\Omega$	—	4.5	—	V_{PP}
R_L	Load Resistance (GS)	5V	—	—	50	—	kΩ
C_L	Load Capacitance (GS)	5V	—	—	100	—	PF
V_{CM}	Common Mode Range	5V	No load	—	3.0	—	V_{PP}

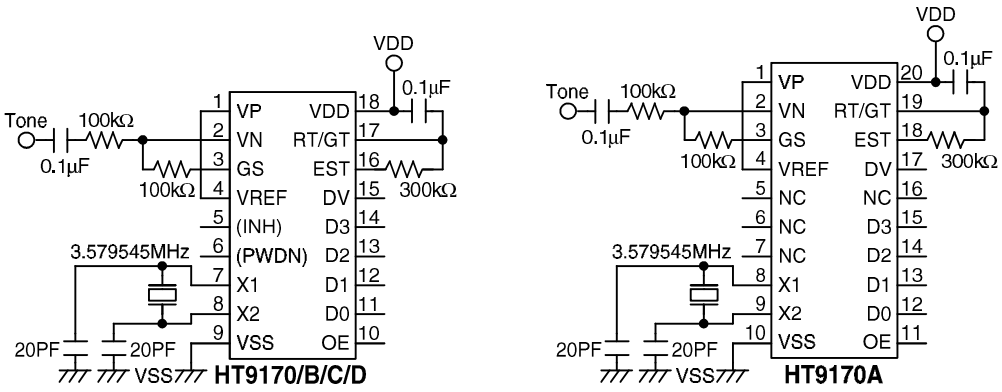


Figure 1. Test circuit

Functional Description

Overview

The HT9170 series are tone decoders. They consist of three band pass filters and two digital decode circuits to convert tone (DTMF) signal into digital code output.

An operational amplifier is built-in to adjust the input signal for users (refer to Figure 2.).

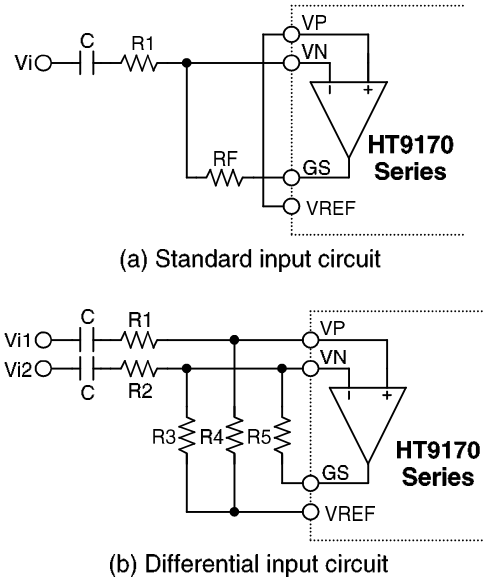


Figure 2. Input operation amplifier application circuits

The pre-filter is a band rejection filter which reduces the dialing tone which is from 350Hz to 400Hz.

The low group filter filters low group frequency signal output whereas the high group filter filters high group frequency signal output.

Each filter output is followed by a zero-crossing detector with hysteresis. When each signal amplitude at the output exceeds the specified level, it is transferred to full swing logic signal.

When input signals are recognized to be effective, DV becomes high, and the correct code of tone (DTMF) digit is transferred.

Steering control circuit

The steering control circuit is used for measureing the effect signal duration and for protecting against the drop out of valid signals. It employs the analog delay by external RC time-constant controlled by EST.

The timing is shown in Figure 3. The EST pin is normally low and draws the RT/GT pin to keep low through discharge of external RC. When a valid tone input is detected, EST goes high to charge RT/GT through RC.

When the voltage of RT/GT changes from 0 to V_{TRT} (2.35V for 5V supply), the input signal is effective, and the correct code will be created by code detector. After D0~D3 are completely latched, DV output becomes high. When the voltage of RT/GT falls down from VDD to V_{TRT} (ie., the input tone is absent), DV output becomes low, and D0~D3 keep data until next valid tone input is yielded.

By selecting adequate external RC value the minimum acceptable input tone duration (t_{ACC}) and the minimun acceptable inter-tone rejection (t_{IR}) can be set by users. External components (R, C) are chosen by the formula (refer to Figure 5.):

$t_{ACC}=t_{DP}+t_{GTP}$;

$t_{IR}=t_{DA}+t_{GTA}$;

where t_{ACC}: Tone duration acceptable time

t_{DP}: EST output delay time (“L”→“H”)

t_{GTP}: Tone present time

t_{IR}: Inter-digit pause reject time

t_{DA}: EST output delay time (“H”→“L”)

t_{GTA}: Tone absent time

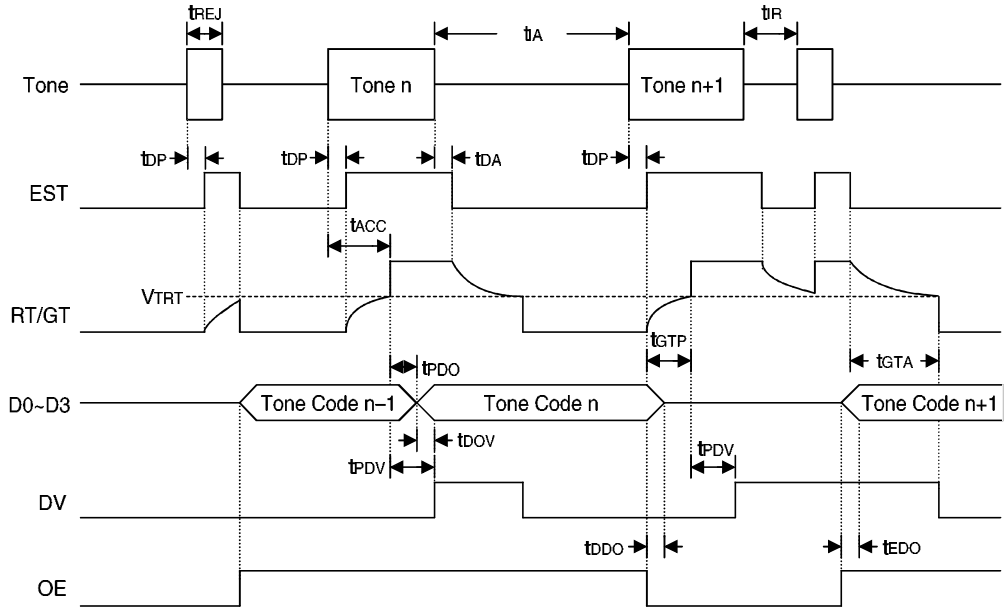


Figure 3. Steering timing

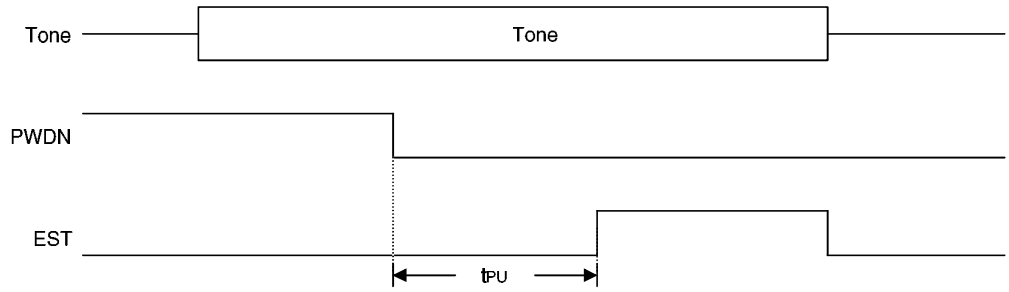
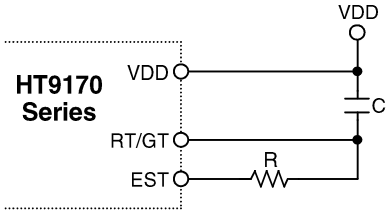


Figure 4. Power up timing

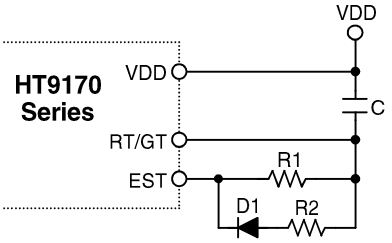
Timing Description: Using test circuit of Figure 1. (Fosc=3.5795MHz, Ta=25°C)

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{DP}	Tone Present Detection Time	5	16	22	ms
t_{DA}	Tone Absent Detection Time	—	4	8.5	ms
t_{ACC}	Acceptable Tone Duration	—	—	42	ms
t_{REJ}	Rejected Tone Duration	20	—	—	ms
t_{IA}	Acceptable Inter-digit Pause	—	—	42	ms
t_{IR}	Rejected Inter-digit Pause	20	—	—	ms
t_{PDO}	Propagation Delay (RT/GT to DO)	—	8	11	μs
t_{PDV}	Propagation Delay (RT/GT to DV)	—	12	—	μs
t_{DOV}	Output Data Set Up (DO to DV)	—	4.5	—	μs
t_{DDO}	Disable Delay (OE to DO)	—	50	60	ns
t_{EDO}	Enable Delay (OE to DO)	—	300	—	ns

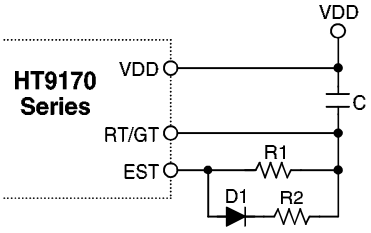
Note: DO=D0~D3.



(a) Fundamental circuit:
$t_{GTP} = R \bullet C \bullet Ln (V_{DD} / (V_{DD} - V_{TRT}))$
$t_{GTA} = R \bullet C \bullet Ln (V_{DD} / V_{TRT})$



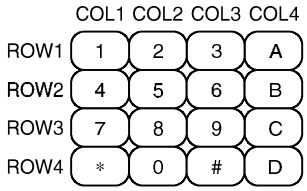
(c) $t_{GTP} > t_{GTA}$:
$t_{GTP} = R1 \bullet C \bullet Ln (V_{DD} / (V_{DD} - V_{TRT}))$
$t_{GTA} = (R1 // R2) \bullet C \bullet Ln (V_{DD} / V_{TRT})$



(b) $t_{GTP} < t_{GTA}$:
$t_{GTP} = (R1 // R2) \bullet C \bullet Ln (V_{DD} - V_{TRT}))$
$t_{GTA} = R1 \bullet C \bullet Ln (V_{DD} / V_{TRT})$

Figure 5. Steering time adjust circuits

Tone (DTMF) Dialing Matrix



Tone (DTMF) Data Output Table

Low Group (Hz)	High Group (Hz)	Digit	OE	D3	D2	D1	D0
697	1209	1	H	L	L	L	H
697	1336	2	H	L	L	H	L
697	1477	3	H	L	L	H	H
770	1209	4	H	L	H	L	L
770	1336	5	H	L	H	L	H
770	1477	6	H	L	H	H	L
852	1209	7	H	L	H	H	H
852	1336	8	H	H	L	L	L
852	1477	9	H	H	L	L	H
941	1336	0	H	H	L	H	L
941	1209	*	H	H	L	H	H
941	1477	#	H	H	H	L	L
697	1633	A	H	H	H	L	H
770	1633	B	H	H	H	H	L
852	1633	C	H	H	H	H	H
941	1633	D	H	L	L	L	L
—	—	ANY	L	Z	Z	Z	Z

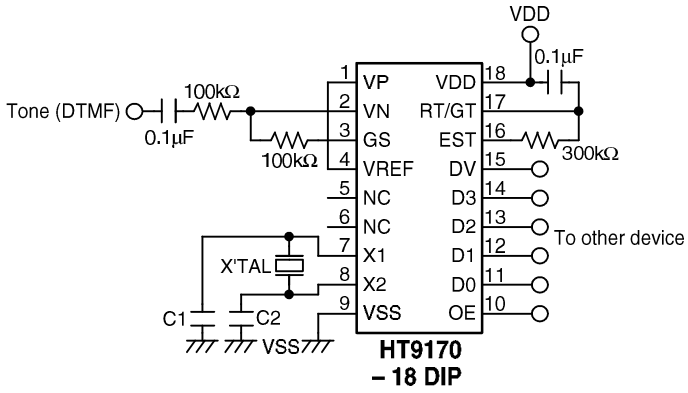
Z: High impedance

Data output

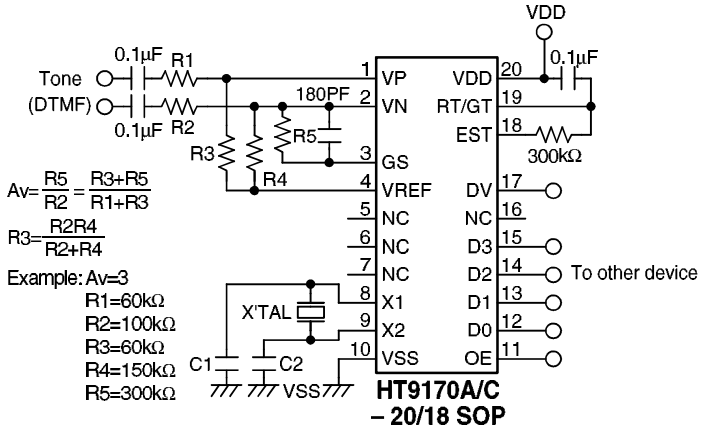
The data outputs (D0~D3) are tri-state outputs. When OE input becomes low, the data outputs (D0~D3) are high impedance.

Application Circuits

Application circuit 1



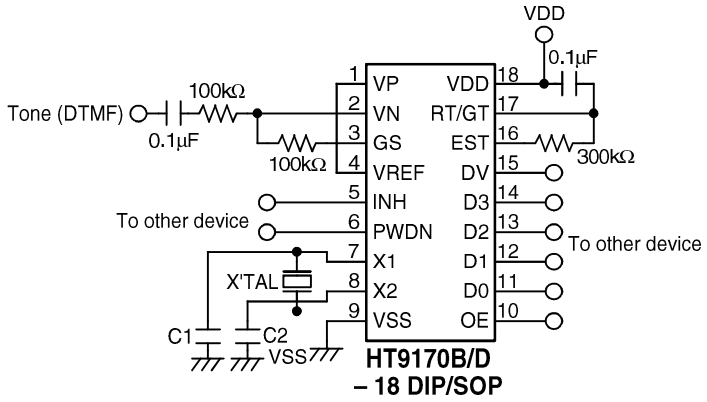
Application circuit 2



Note: (a) X'TAL = 3.579545MHz crystal
C1 = C2 ≅ 20PF

(b) X'TAL = 3.58MHz ceramic resonator
C1 = C2 ≅ 39PF

Application circuit 3



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C1 = C2 ≅ 20PF

(b) X'TAL = 3.58MHz ceramic resonator
C1 = C2 ≅ 39PF