NCP1231

Low-Standby Power High Performance PWM Controller

The NCP1231 represents a major leap towards achieving low standby power in medium−to−high power Switched−Mode Power Supplies such as notebook adapters, off−line battery chargers and consumer electronics equipment. Housed in SOIC−8 or PDIP−8, the NCP1231 contains all needed control functionality to build a rugged and efficient power supply. Among the unique features offered by the NCP1231 is an event management scheme that can disable the front−end PFC circuit during standby, thus reducing the no load power consumption. The NCP1231 itself goes into cycle skipping at light loads while limiting peak current (to 25% of nominal peak) so that no acoustic noise is generated and while in the skip cycle mode.

The NCP1231 also features an internal latching function that can be used for Overvoltage Protection (OVP). The latch is triggered when the voltage on Pin 8 rises above 4.0 V. During an OVP condition, the output drive pulses are immediately stopped and the NCP1231 stays in the latched off condition until V_{CC} drops below 4.0 V ($V_{CCreset}$). In addition, Pin 8 also serves as a Brown−Out input which provides the necessary safety feature when the SMPS faces low mains situations.

Features

- Current−Mode Operation with Internal Ramp Compensation
- **Extremely Low Startup Current** of 30 μA Typical
- Skip−Cycle Capability at Low Peak Currents
- Adjustable Soft−Start
- **Overvoltage** and **Brown−Out Protection**
- Short−Circuit Protection Independent of Auxiliary Level
- Internal Frequency Dithering for Improved EMI Signature
- Go−To−Standby Signal for PFC Front Stage
- Extremely Low No−Load, Noiseless, Standby Power
- Internal Leading Edge Blanking
- +500 mA/−800 mA Peak Current Drive Capability
- Available in Three Frequency Options: 65 kHz, 100 kHz, and 133 kHz
- Direct Optocoupler Connection
- SPICE Models Available for TRANsient and AC Analysis
- Pb−Free Packages are Available

Typical Applications

- High Power AC−DC Adapters for Notebooks, etc.
- Offline Battery Chargers
- Set−Top Boxes Power Supplies, TV, Monitors, etc.

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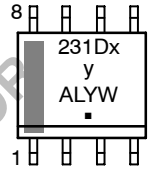
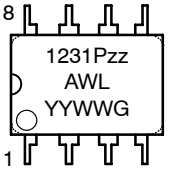
MARKING DIAGRAMS

SOIC−8
D SUFFIX
CASE 751

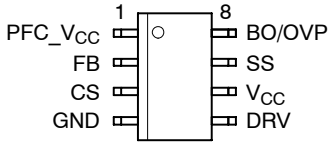


PDIP−8
P SUFFIX
CASE 626



231Dxy	= Device Code x = 1 or 6 y = 0 or 3
1231Pzz	= Device Code zz = 65, 100 or 133
A	= Assembly Location
L, WL	= Wafer Lot
Y, YY	= Year
W, WW	= Work Week
▪ or G	= Pb−Free Package

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 19 of this data sheet.

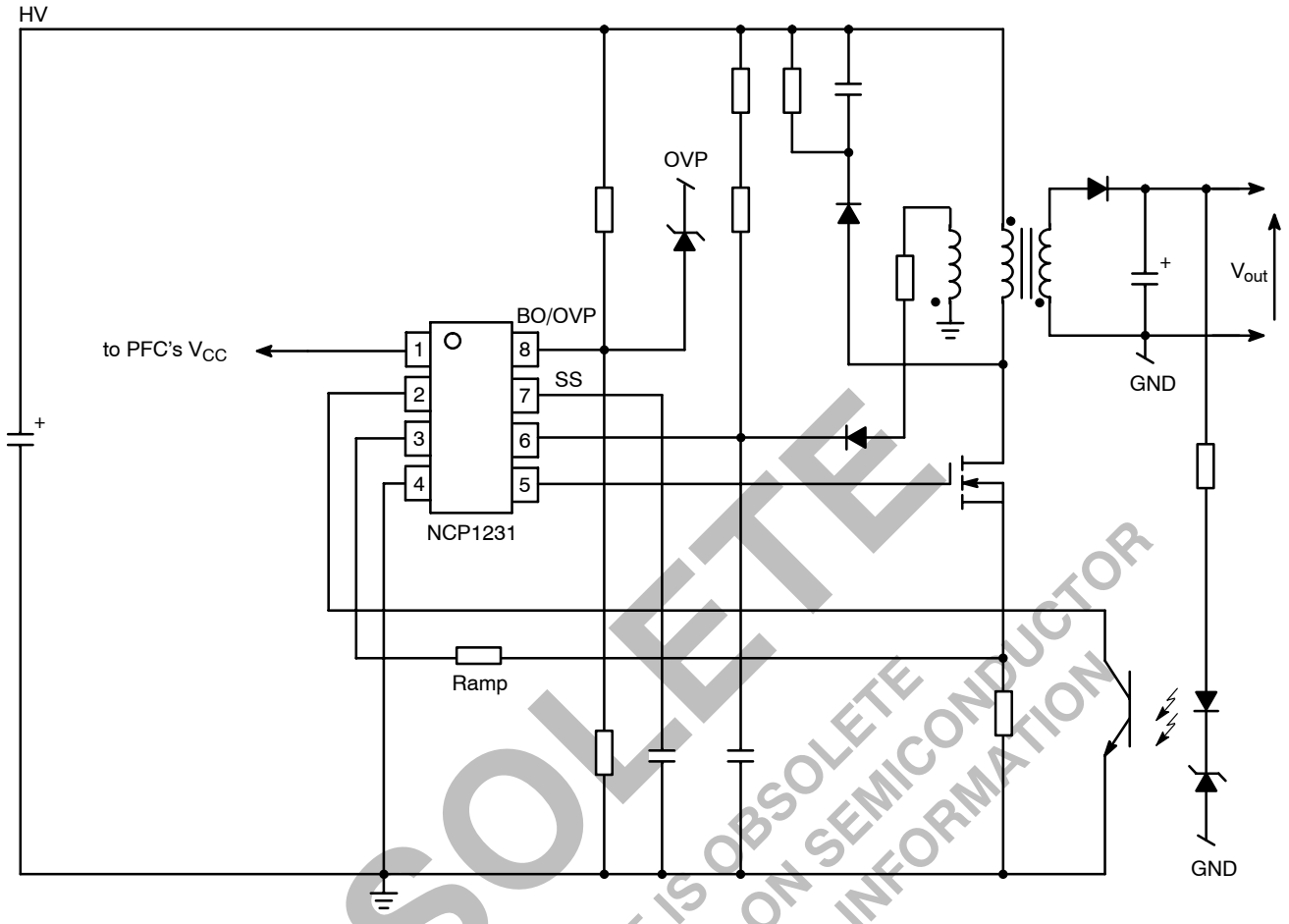


Figure 1. Typical Application Example

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Function	Pin Description
1	PFC V_{CC}	Directly powers the PFC front−end stage	This pin is a direct connection to the V_{CC} pin (Pin 6) via a low impedance switch. In standby and during the startup sequence, the switch is open and the PFC V_{CC} is shutdown. As soon as the aux. winding is stabilized, Pin 1 connects to the V_{CC} pin and provides bias to the PFC controller. It goes down in standby and fault conditions.
2	FB	Feedback Signal	An optocoupler collector pulls this pin low to regulate. When the current setpoint falls below 25% of the maximum peak, the controller skips cycles.
3	CS	Current Sense	This pin incorporates two different functions: the standard sense function and an internal ramp compensation signal.
4	GND	IC Ground	−
5	DRV	Driver Output	With a drive capability of +500 mA / −800 mA, the NCP1231 can drive large Qg MOSFETs.
6	V_{CC}	V_{CC} Input	The controller accepts voltages up to 18 V and features a UVLO of 7.7 V typical.
7	SS (Soft−Start)	To provide an internal ramp timing for different usages	This pin provides three different functions, via a capacitor to ground, saw tooth signal whose function is to create a soft−start, frequency dithering and 100 msec fault timer.
8	BO/OVP	Brown−Out and OVP	By connecting this pin to a resistive divider, the controller ensures operation at a safe mains level. If an external event brings this pin above 4 V, the controller is permanently latched−off.

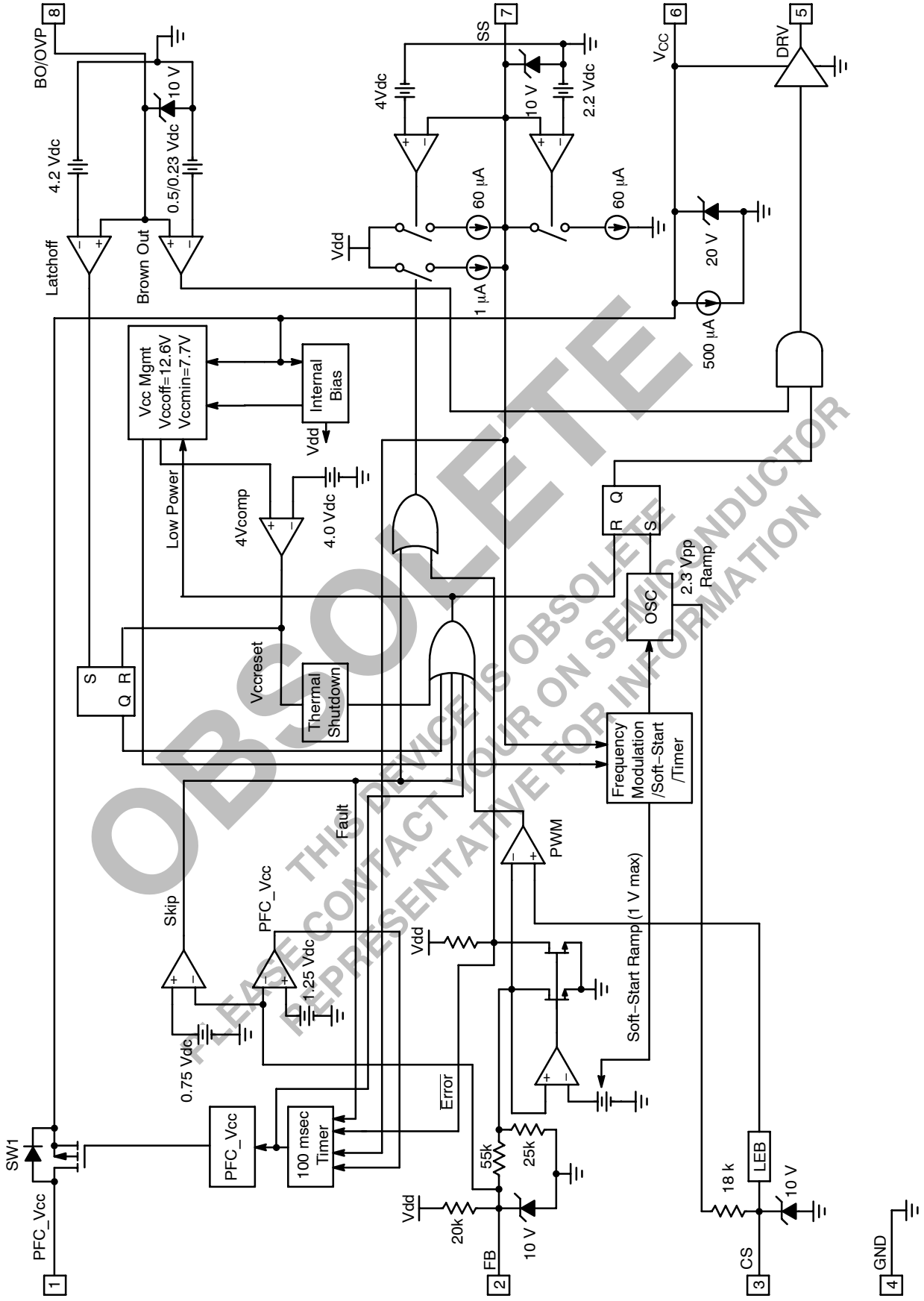


Figure 2. Internal Circuit Architecture

MAXIMUM RATINGS (Notes 1 and 2)

Rating		Symbol	Value	Unit
Voltage BO/OVP Pin 8 Current		BO/OVP	10 100	V mA
Voltage Pin 7 Current		SS	10 100	V mA
Power Supply Voltage, Pin 6 Maximum Current		V_{CC} I_C	−0.3 to 18 100	V mA
Drive Output Voltage, Pin 5 Drive Current		V_{DV} I_o	18 1.0	V A
Voltage Current Sense Pin, Pin 3 Current		V_{cs} I_{cs}	10 100	V mA
Voltage Feedback, Pin 2 Current		V_{fb} I_{fb}	10 100	V mA
Voltage, Pin 1 Maximum Continuous Current Flowing from Pin 1		V_{PFC} I_{PFC}	18 35	V mA
Thermal Resistance, Junction−to−Air, PDIP Version		$R_{\theta JA}$	100	°C/W
Thermal Resistance, Junction−to−Air, SOIC Version		$R_{\theta JA}$	178	°C/W
Maximum Power Dissipation @ T_A = 25°C	PDIP SOIC	P_{max}	1.25 0.702	W
Maximum Junction Temperature		T_J	150	°C
Storage Temperature Range		T_{stg}	−60 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device series contains ESD protection and exceeds the following tests:
   Pin 1−6: Human Body Model 2000 V per Mil−Std−883, Method 3015.
   Machine Model Method 200 V
2. This device contains latchup protection and exceeds 100 mA per JEDEC Standard JESD78.

ELECTRICAL CHARACTERISTICS (For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 13 V, unless otherwise noted.)

Rating	Symbol	Pin	Min	Typ	Max	Unit
Supply Section (All frequency versions, otherwise noted)						
Turn−On Threshold Level, V_{CC} going up (V_{fb} = 2.0 V)	V_{CCON}	6	11.3	12.6	13.8	V
Minimum Operating Voltage after Turn−On	$V_{CC(min)}$	6	7.0	7.7	8.4	V
V_{CC} Level at which the Internal Logic gets Reset (Note 4)	$V_{CCreset}$	6	–	4.0	–	V
Startup Current (V_{CCON} −0.2 V)	$I_{startup}$	6	–	30	50	μA
Internal IC Consumption, No Output Load on Pin 6 (V_{fb} = 2.5 V)	I_{CC1}	6	0.75	1.3	2.0	mA
Internal IC Consumption, 1.0 nF Output Load on Pin 5, F_{SW} = 65 kHz	I_{CC2}	6	1.4	2.0	2.6	mA
Internal IC Consumption, 1.0 nF Output Load on Pin 5, F_{SW} = 100 kHz	I_{CC2}	6	1.4	2.4	3.1	mA
Internal IC Consumption, 1.0 nF Output Load on Pin 5, F_{SW} = 133 kHz	I_{CC2}	6	1.4	2.9	3.7	mA
Internal IC Consumption, Latch−Off Phase	I_{CC3}	6	300	500	800	μA
Drive Output						
Output Voltage Rise−Time @ C_L = 1.0 nF, 10−90% of Output Signal (Note 4)	T_r	5	–	40	–	ns
Output Voltage Fall−Time @ C_L = 1.0 nF, 10−90% of Output Signal (Note 4)	T_f	5	–	15	–	ns
Source Resistance (R_{Load} = 300 Ω, V_{fb} = 2.5 V)	R_{OH}	5	6.0	12.3	25	Ω
Sink Resistance, at 1.0 V on Pin 5 (V_{fb} = 3.5 V)	R_{OL}	5	3.0	7.5	18	Ω
Pin1 Output Impedance (or R_{dson} between Pin 1 and Pin 6 when SW1 is closed) R_{load} on Pin 1= 680 Ω	RPFC	1	6.0	11.7	23	Ω
Current Comparator (Pin 5 unloaded)						
Input Bias Current @ 1.0 V Input Level on Pin 3	I_{IB}	3	–	0.02	–	μA
Maximum Internal Current Set Point T_J = +25°C T_J = −40°C to +125°C	I_{Limit}	3	0.95 0.93	1.00 –	1.05 1.07	V
Default Internal Set Point for Skip Cycle Operation and Standby Detection	V_{skip}	3	600	750	900	mV
Default Internal Set Point to Leave Standby	$V_{stby-out}$	–	1.0	1.25	1.5	V
Propagation Delay from CS Detected to Gate Turned Off (Pin 5 Loaded by 1.0 nF)	$T_{DEL\ CS}$	3	–	90	200	ns
Leading Edge Blanking Duration	T_{LEB}	3	100	250	350	ns
Internal Oscillator						
Oscillation Frequency, 65 kHz version (V_{fb} = 2.5 V)	f_{OSC}	–	56	65	69	kHz
Oscillation Frequency, 100 kHz version (V_{fb} = 2.5 V)	f_{OSC}	–	88	100	108	kHz
Oscillation Frequency, 133 kHz version (V_{fb} = 2.5 V)	f_{OSC}	–	118	133	140	kHz
Internal Modulation Swing, in Percentage of Fsw) (Typical) (Note 4)	–	–	–	±4.0	–	%
Internal Swing Period with a 82 nF Capacitor to Pin 7) (Typical) (Note 4)	–	–	–	5.0	–	ms
Maximum Duty−Cycle	D_{max}	–	75	80	85	%
Typical Soft−Start Period with a 82 nF to Pin 7 (Note 4)	SS	7	–	5.0	–	ms
SS Charging/Discharging Current	–	7	35	60	75	μA
Timer Charging Current (Typical) (Note 4)	–	7	–	1.36	–	μA
Timer Peak Voltage	–	7	3.5	4.0	4.5	V
Timer Valley Voltage	–	7	1.9	2.2	2.6	V
Feedback Section (V_{CC} = 13 V)						
Opto Current Source (V_{fb} = 0.75 V)	–	2	190	235	270	μA
Pin 3 to Current Setpoint Division Ratio (Note 3)	I_{ratio}	–	–	3.0	–	–

ELECTRICAL CHARACTERISTICS (For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 13 V, unless otherwise noted.)

Rating	Symbol	Pin	Min	Typ	Max	Unit
Internal Ramp Compensation (V_{CC} = 13 V)						
Internal Resistor (Note 3)	R_{up}	3	9.0	18	36	kΩ
Internal Sawtooth Amplitude (Note 4)	–	3	–	2.3	–	Vpp
Protection (V_{CC} = 13 V)						
Timeout before Validating Short−Circuit or PFC V_{CC} with an 82 nF cap. to Pin 7 (Note 4)	T_{delay}	–	–	110	–	ms
Latch−Off Level	V_{latch}	8	3.7	4.2	4.5	V
Propagation Delay from Latch Detected to Gate Turned Off (Pin 5 Loaded by 1.0 nF)	$T_{DEL\ LATCH}$	–	–	100	–	ns
Brown−Out Level High	V_{BOhigh}	8	0.40	0.50	0.55	V
Brown−Out Level Low	V_{BOlow}	8	0.180	0.230	0.285	V
Temperature Shutdown, Maximum Value (Note 4)	T_{SD}	–	–	160	–	°C
Hysteresis while in Temperature Shutdown (Note 4)	$T_{SD\ hyste}$	–	–	30	–	°C

3. Guaranteed by Design.
4. Verified by Design.

TYPICAL PERFORMANCE CHARACTERISTICS

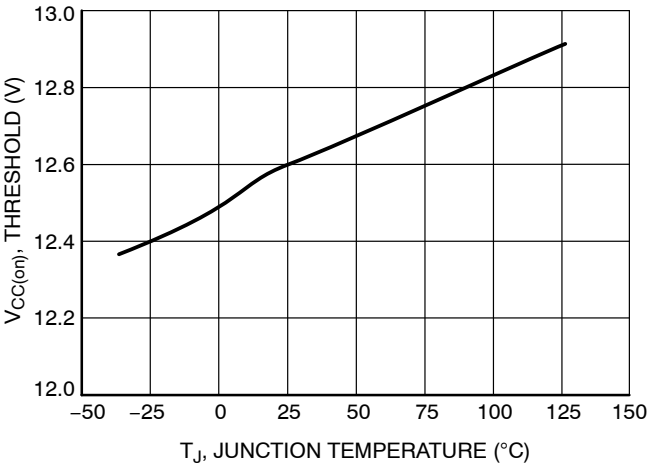


Figure 3. $V_{CC(on)}$ Threshold vs. Temperature

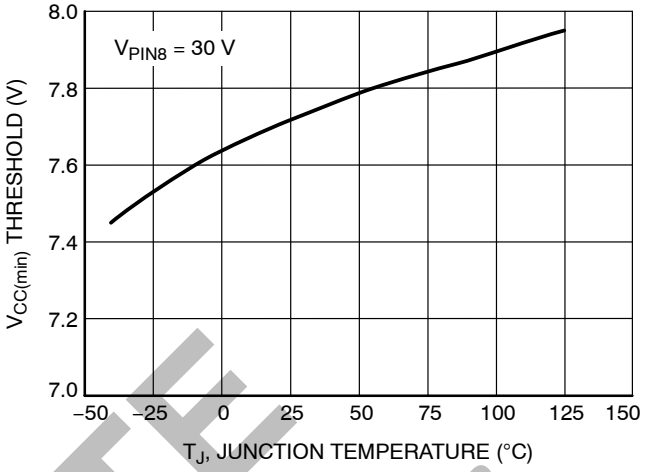


Figure 4. $V_{CC(min)}$ Threshold vs. Temperature

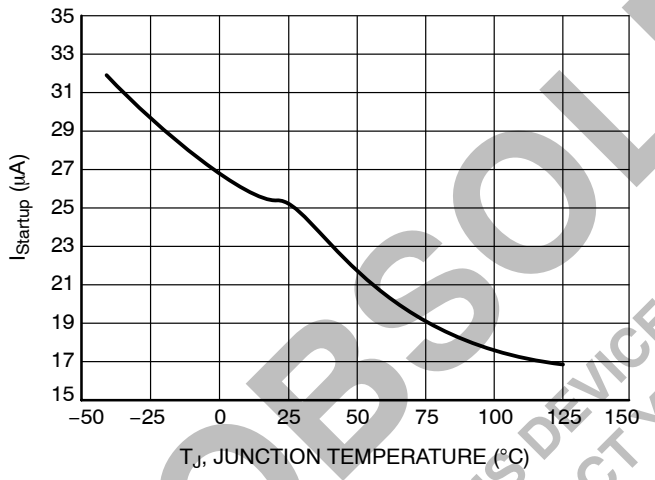


Figure 5. $I_{startup}$ vs. Temperature

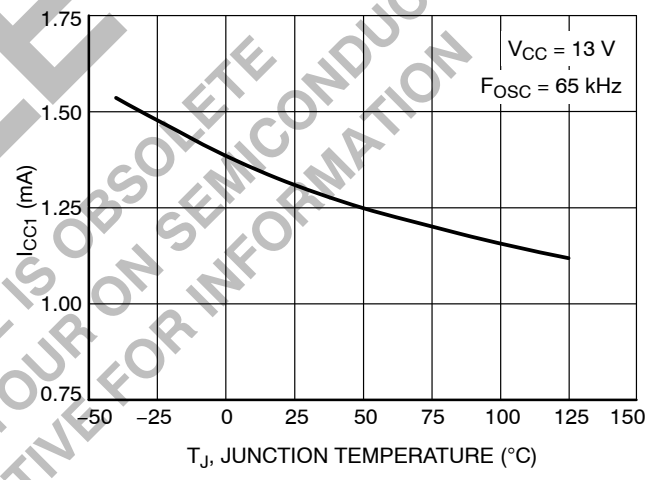


Figure 6. I_{CC1} Internal Current Consumption, No Load vs. Temperature

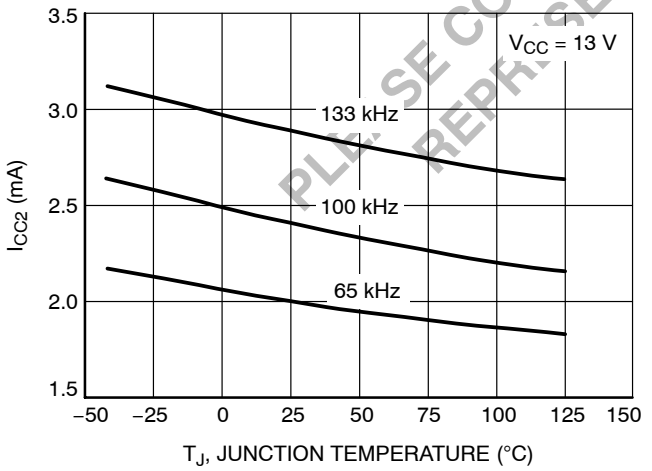


Figure 7. I_{CC2} Internal Current Consumption, 1.0 nF Load vs. Temperature

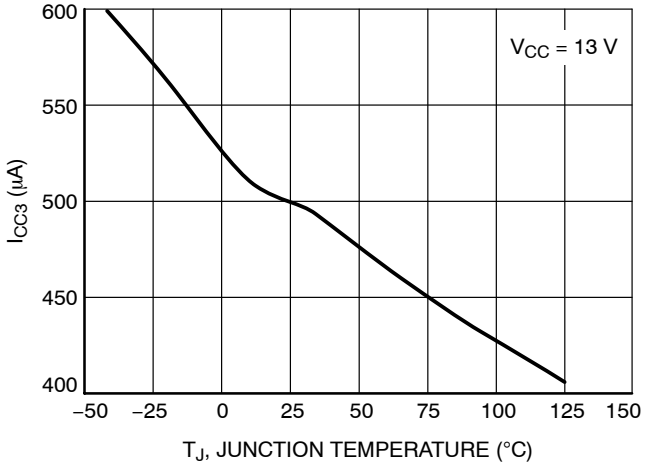


Figure 8. I_{CC3} Internal Consumption, Latch−Off Phase vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

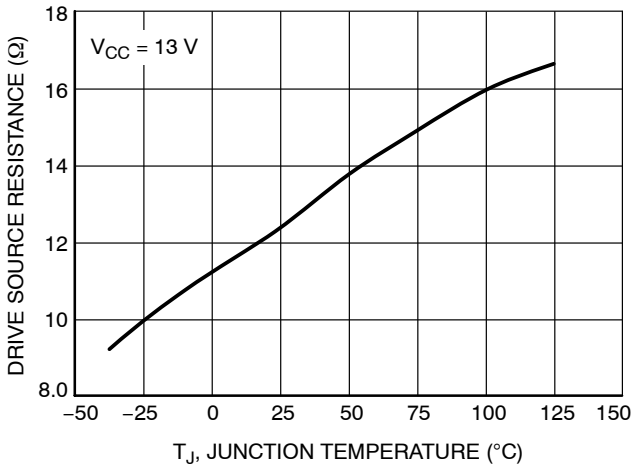


Figure 9. Drive Source Resistance vs. Temperature

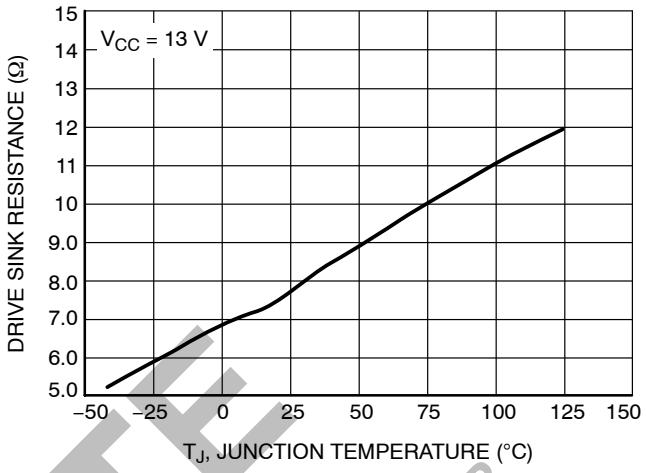


Figure 10. Drive Sink Resistance vs. Temperature

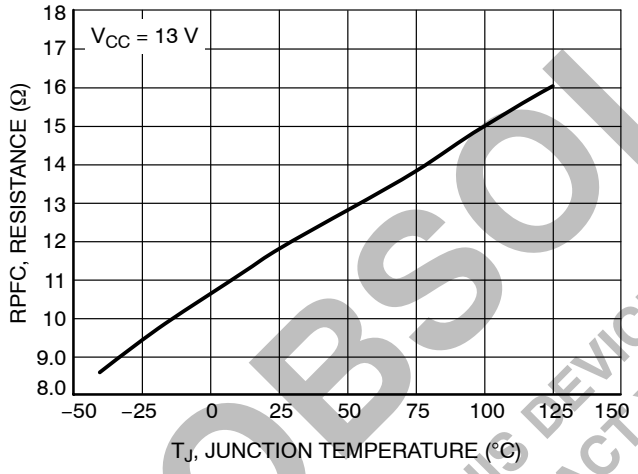


Figure 11. RPFC vs. Temperature

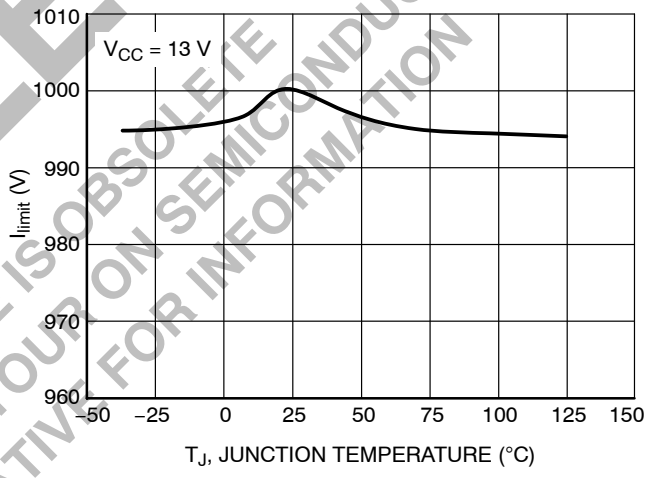


Figure 12. I_{Limit} vs. Temperature

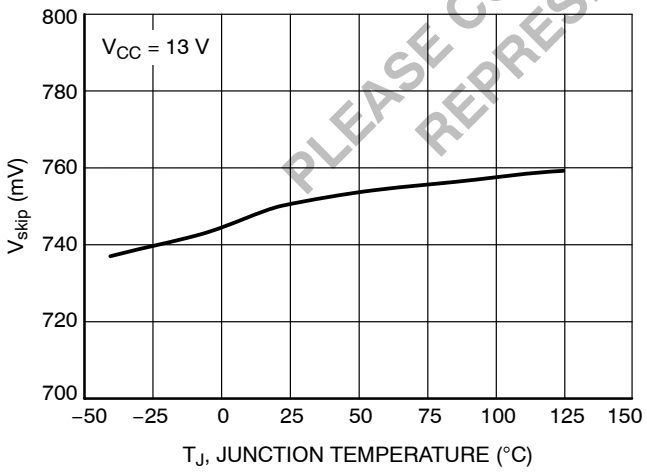


Figure 13. V_{Skip} vs. Temperature

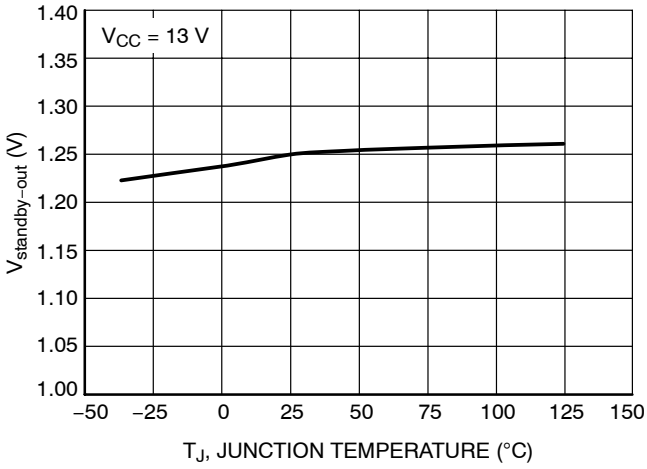


Figure 14. $V_{standby-out}$ vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

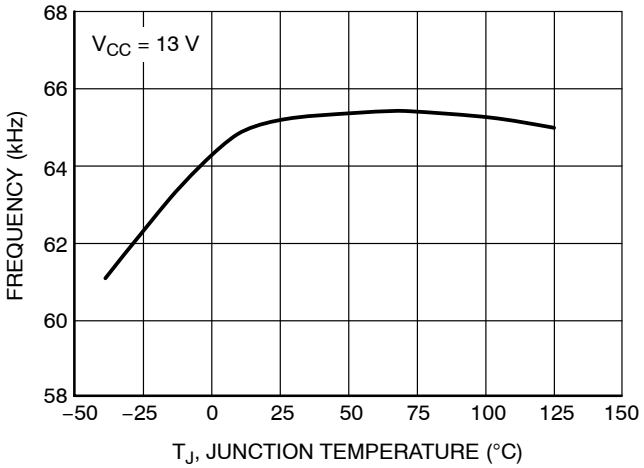


Figure 15. Frequency (65 kHz) vs. Temperature

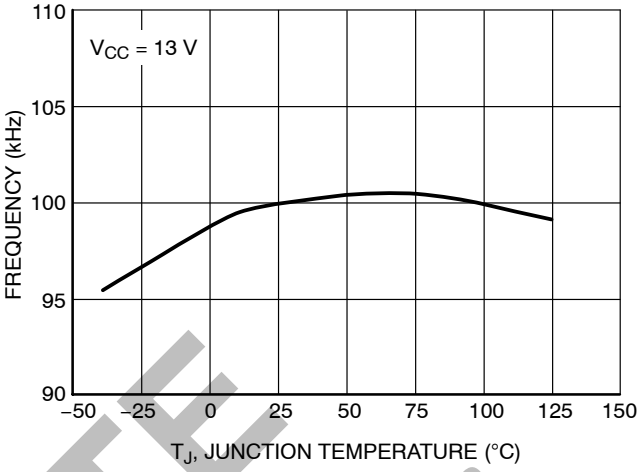


Figure 16. Frequency (100 kHz) vs. Temperature

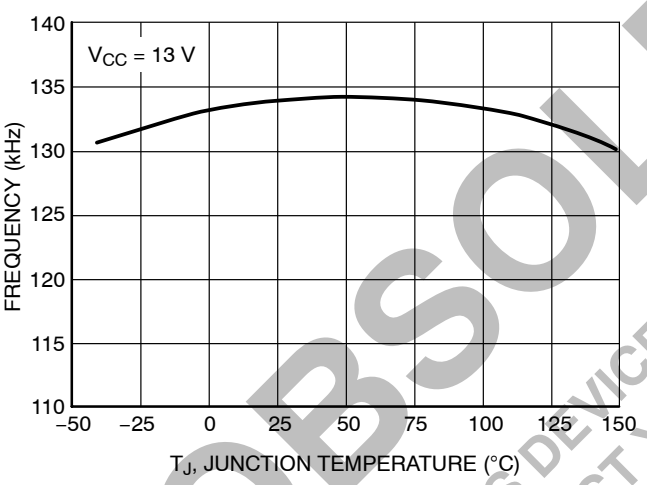


Figure 17. Frequency (133 kHz) vs. Temperature

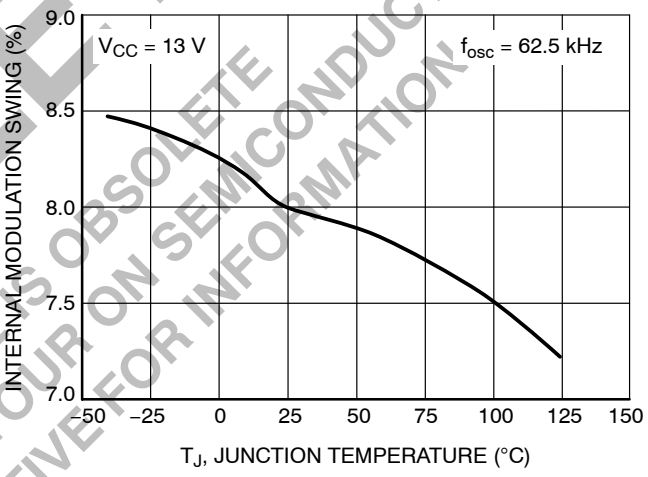


Figure 18. Internal Modulation Swing vs. Temperature

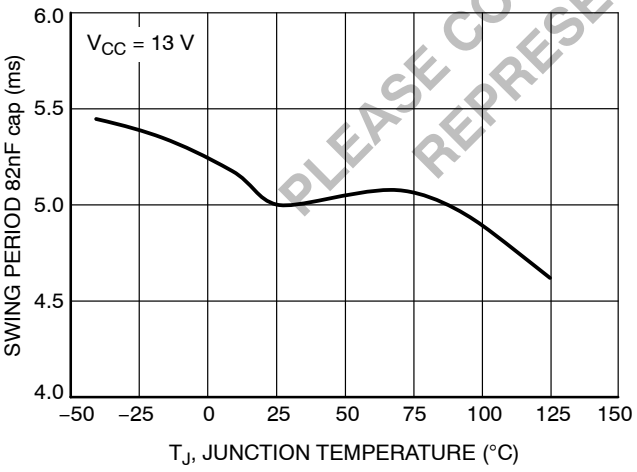


Figure 19. Internal Swing Period vs. Temperature

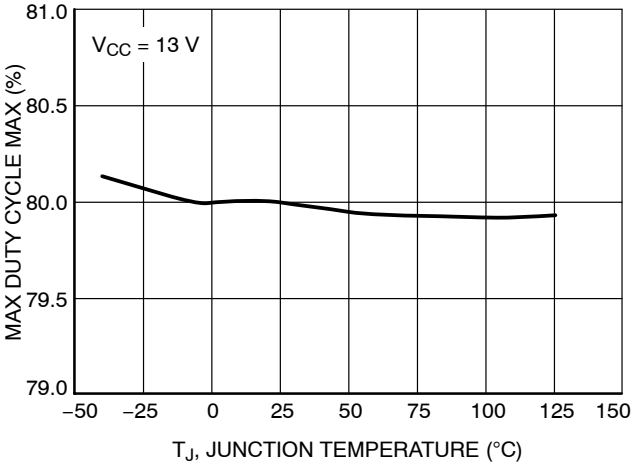


Figure 20. Maximum Duty Cycle vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

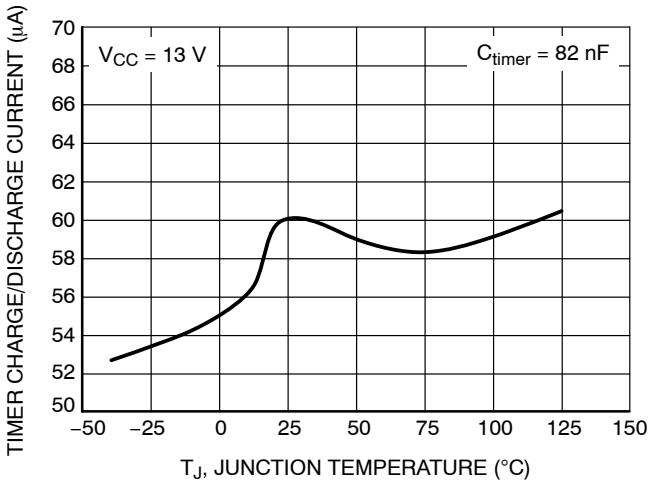


Figure 21. Timer Charge/Discharge Current vs. Temperature

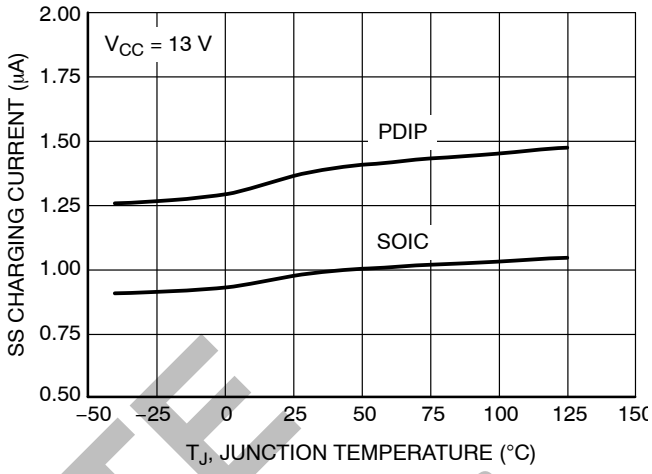


Figure 22. Soft−Start Charging Current vs. Temperature

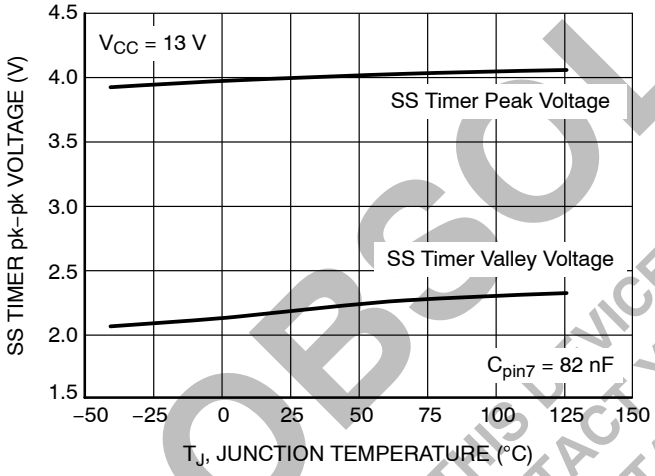


Figure 23. SS Timer Peak and Valley Voltages vs. Temperature

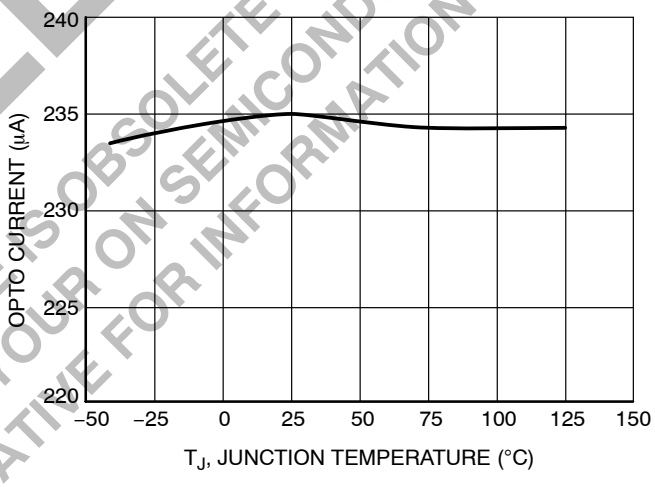


Figure 24. Opto−Coupler Current vs. Temperature

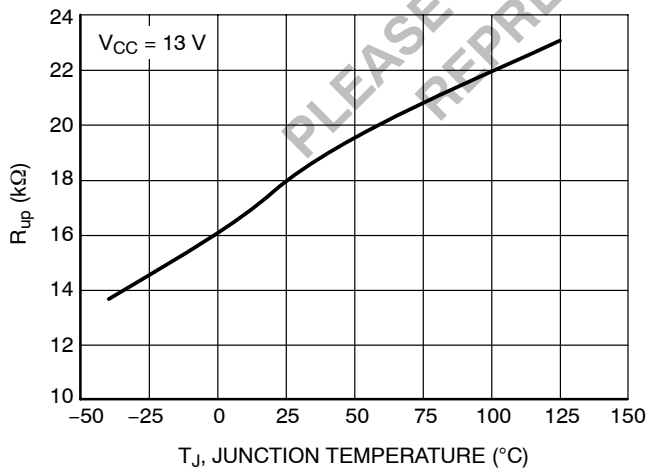


Figure 25. Internal Ramp Compensation Resistor vs. Temperature

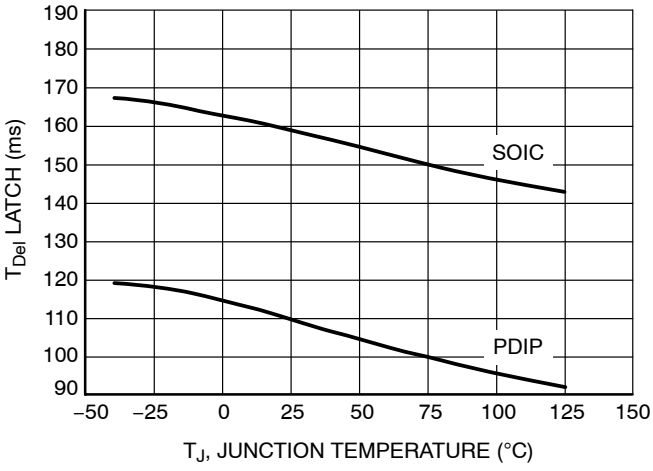


Figure 26. Time Delay vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

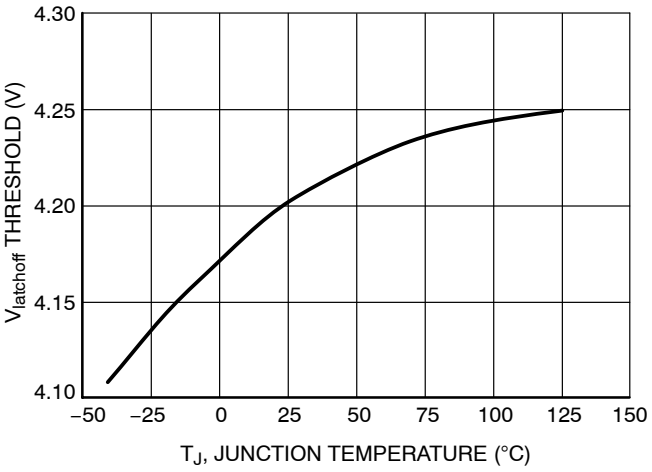


Figure 27. $V_{latchoff}$ Threshold vs. Temperature

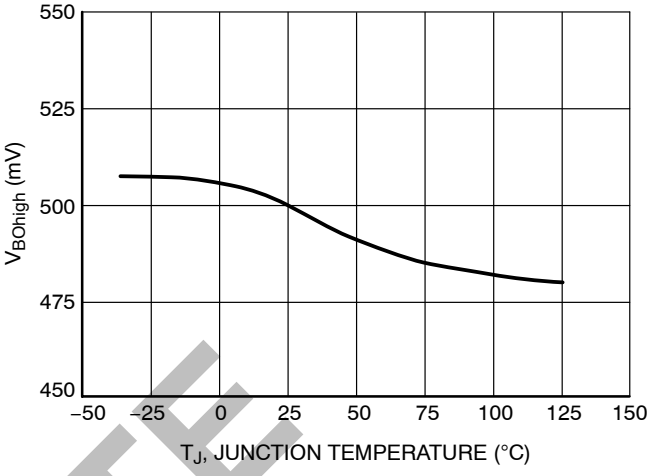


Figure 28. V_{BOhigh} vs. Temperature

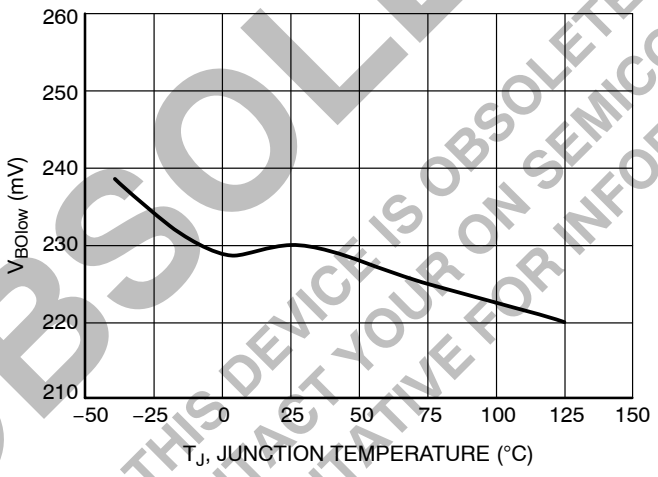


Figure 29. V_{BOlow} vs. Temperature

OPERATING DESCRIPTION

Introduction

The NCP1231 is a current mode controller which provides a high level of integration by providing all the required control logic, protection, and a PWM Drive Output into a single chip which is ideal for low cost, medium to high power off−line application, such as notebook adapters, battery chargers, set−boxes, TV, and computer monitors.

The NCP1231 has a low startup current (30 μA) allowing the controller to be connected directly to a high voltage source through a resistor, providing low loss startup, and reducing external circuitry. In addition, the NCP1231 has a PFC_V_{CC} output pin which provides the bias supply power for a Power Factor Correction controller, or other logic. The NCP1231 has an event management scheme which disables the PFC_V_{CC} output during standby, and overload conditions.

PFC_V_{CC}

As shown on the internal NCP1231 internal block diagram, an internal low impedance switch SW1 routes Pin 6 (V_{CC}) to Pin 1 when the power supply is operating under nominal load conditions. The PFC_V_{CC} signal is capable of delivering up to 35 mA of continuous current for a PFC Controller, or other logic.

Connecting the NCP1231 PFC_V_{CC} output to a PFC Controller chip is very straight forward, refer to the “Typical Application Example” (Figure 30) all that is generally required is a small decoupling capacitor (0.1 μF) near the PFC controller.

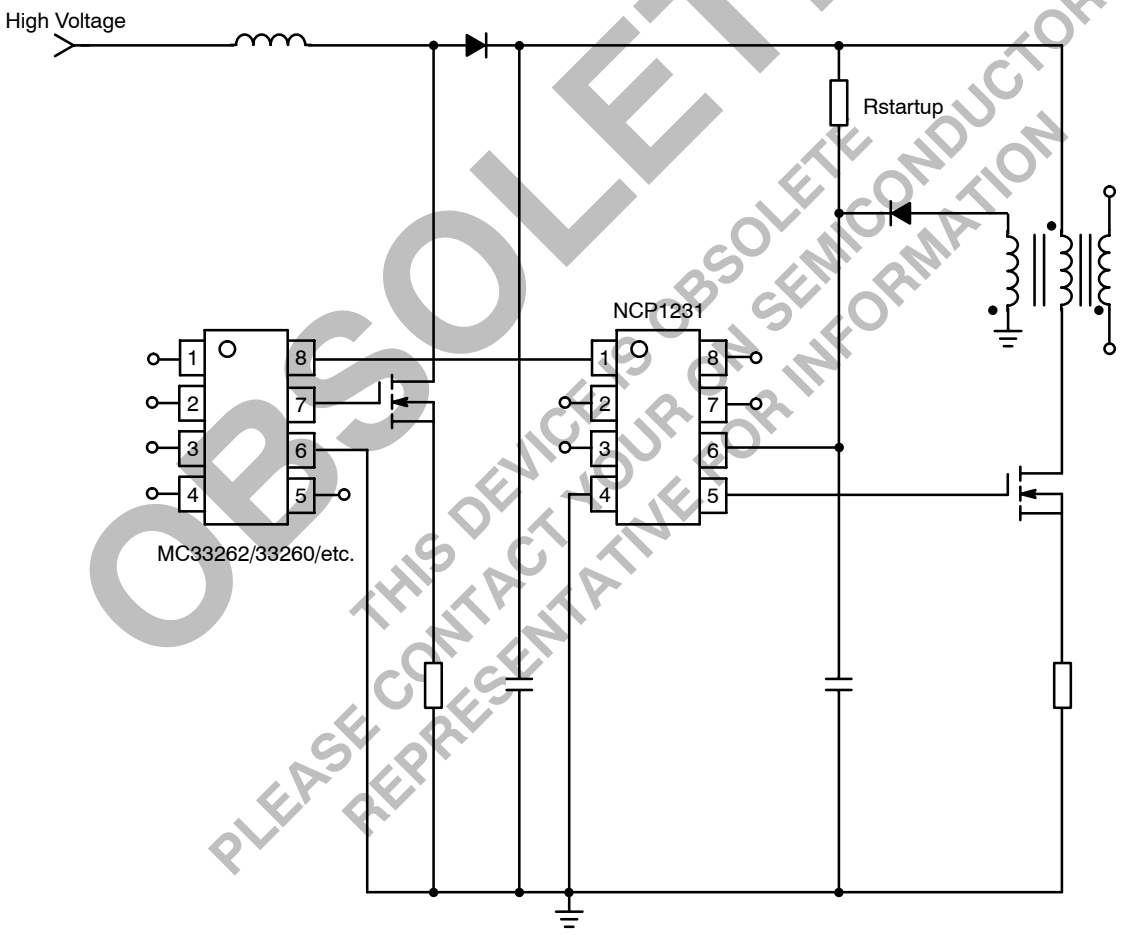


Figure 30. Typical Application Example

Feedback

The feedback pin has been designed to be connected directly to the open−collector output of an optocoupler. The pin is pulled−up through a 20 kΩ resistor to the internal Vdd supply (6.5 volts nominal). The feedback input signal is divided down, by a factor of three, and connected to the negative (−) input of the PWM comparator. The positive (+) input to the PWM comparator is the current sense signal (Figure 31).

The NCP1231 is a peak current mode controller, where the feedback signal is proportional to the output power. At the beginning of the cycle, the power switch is turns−on and the current begins to increase in the primary of the transformer, when the peak current crosses the feedback voltage level, the PWM comparators switches from a logic level low, to a logic level high, resetting the PWM latching Flip−Flop, turning off the power switch until the next oscillator clock cycle begins.

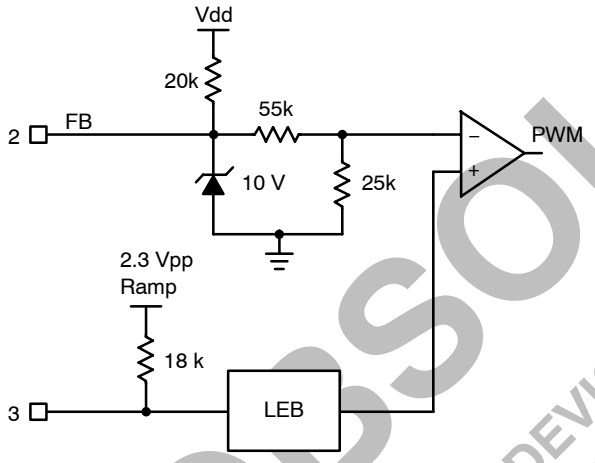


Figure 31.

The feedback pin input is clamped to a nominal 10 volt for ESD protection.

Skip Mode

The feedback input is connected in parallel with the skip cycle logic (Figure 32). When the feedback voltage drops below 25% of the maximum peak current (1 V/Rsense) the IC prevents the current from decreasing any further and starts to blank the output pulses. This is called the skip cycle mode. While the controller is in the burst mode the power transfer now depends upon the duty cycle of the pulse burst width which reduces the average input power demand.

$$V_C = I_{pk} \cdot R_s \cdot 3$$

where:

V_c = control voltage (Feedback pin input),

I_{pk} = Peak primary current,

R_s = Current sense resistor,

3 = Feedback divider ratio.

$$SkipLevel = 3V \cdot 25\% = 0.75V$$

$$I_{pk} = \frac{0.75}{R_s \cdot 3}$$

where:

$$I_{pk} \cdot R_s = 1V$$

$$I_{pk} = \sqrt{\frac{2 \cdot P_{in}}{L_p \cdot f}}$$

where:

P_{in} = is the power level where the NCP1231 will go into the skip mode

L_p = Primary inductance

f = NCP1231 controller frequency

$$P_{in} = \frac{L_p \cdot f \cdot I_{pk}^2}{2}$$

$$P_{in} = \frac{P_{out}}{Eff}$$

where:

Eff = the power supply efficiency

$$R_{out} = \frac{E_{out}^2}{P_{out}}$$

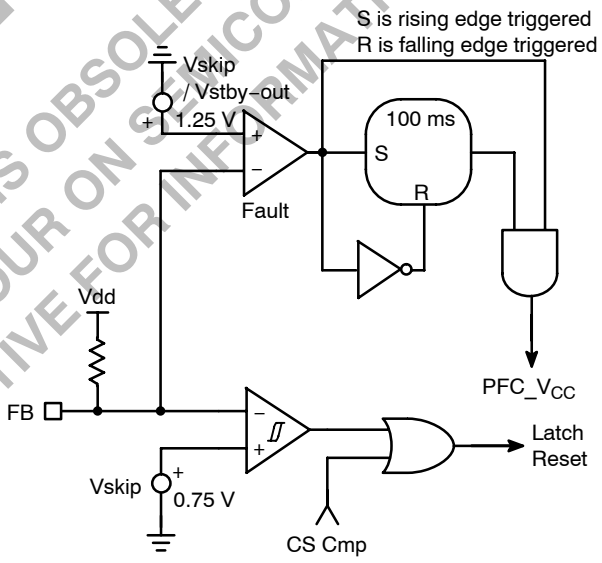


Figure 32.

During the skip mode the PFC_Vcc signal (pin 1) is asserted into a high impedance state when a light load condition is detected and confirmed, Figure 33 shows typical waveforms. The first section of the waveform shows a normal startup condition, where the output voltage is low, as a result the feedback signal will be high asking the controller to provide the maximum power to the output. The second phase is under normal loading, and the output is in regulation. The third phase is when the output power drops below the 25% threshold (the feedback voltage drops to 0.75 volts). When this occurs, the 100 mses timer starts, and if the conditions is still present after the time output period, the

NCP1231 confirms that the low output power condition is present, and the internal SW1 opens. After the NCP1231 confirms that it is in a low power mode, versus a load transient, the PFC_Vcc signal output is shuts down. While the NCP1231 is in the skip mode the FB pin will move around the 750 mV threshold level, with approximately 100 mVp−p of hysteresis on the skip comparator, at a period which depends upon the (light) loading of the power supply and its various time constants. Since this ripple amplitude superimposed over the FB pin is lower than the second threshold (1.25 volt), the PFC_Vcc comparator output stays high (PFC_Vcc output Pin 1 is low).

In Phase four**,** the output power demands have increases and the feedback voltage rises above the 1.25 volts threshold, the NCP1231 exits the skip mode, and returns to normal operation.

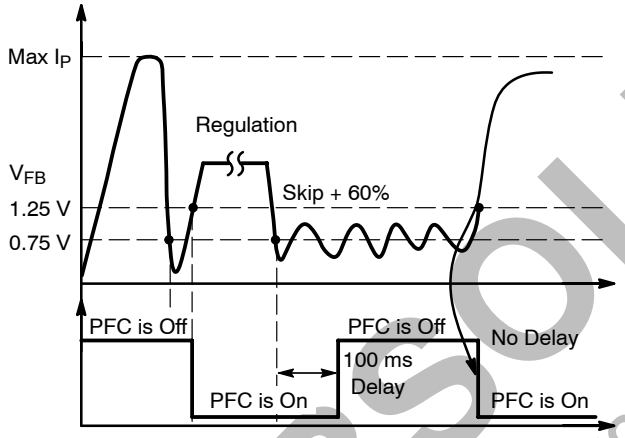


Figure 33. Skip Mode

Leaving standby (Skip Mode)

When the feedback voltage rises above the 1.25 volts reference (leaving standby) the skip cycle activity stops and SW1 immediately closes and restarts the PFC, there is no delay in turning on SW1 under these conditions.

Current Sense

The NCP1231 is a peak current mode controller, where the current sense input is internally clamped to 1 V, so the sense resister is determined by Rsense = 1 V/Ipk maximum.

There is a 18k resistor connected to the CS pin, the other end of the 18k resistor is connect to the output of the internal oscillator for ramp compensation (refer to Figure 34).

Ramp Compensation

In Switch Mode Power Supplies operating in Continuous Conduction Mode (CCM) with a duty−cycle greater than 50%, oscillation will take place at half the switching frequency. To eliminate this condition, Ramp Compensation can be added to the current sense signal to cure sub harmonic oscillations. To lower the current loop gain one typically injects between 50 and 100% of the inductor down slope.

The NCP1231 provides an internal 2.3 Vpp ramp which is summed internally through a 18 kΩ resistor to the current sense pin. To implement ramp compensation a resistor needs to be connected from the current sense resistor, to the current sense pin 3.

Example:

If we assume we are using the 65 kHz version of the NCP1231, at 65 kHz the dv/dt of the ramp is 130 mV/μs. Assuming we are designing a FLYBACK converter which has a primary inductance, Lp, of 350 μH, and the SMPS has a +12 V output with a Np:Ns ratio of 1:0.1. The OFF time primary current slope is given by:

$$\frac{(V_{out} + V_f) \cdot \frac{Ns}{Np}}{L_p} = 371 \text{ mA/μs or } 37 \text{ mV/μs}$$

when imposed on a current sense resistor (Rsense) of 0.1 Ω. If we select 75% of the inductor current downslope as our required amount of ramp compensation, then we shall inject 27 mV/μs.

With our internal compensation being of 130 mV, the divider ratio (*divratio*) between Rcomp and the 18 kΩ is 0.207. Therefore:

$$R_{comp} = \frac{18k \cdot divratio}{(1 - divratio)} = 4.69\ k\Omega$$

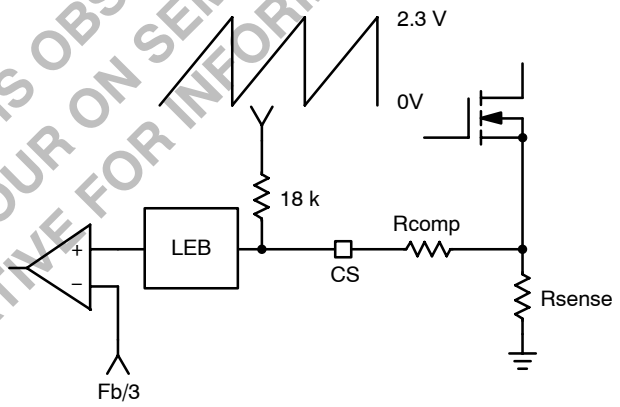


Figure 34.

Leading Edge Blanking

In Switch Mode Power Supplies (SMPS) there can be a large current spike at the beginning of the current ramp due to the Power Switch gate to source capacitance, transformer interwinding capacitance, and output rectifier recovery time. To prevent prematurely turning off the PWM drive output, a Leading Edges Blanking (LEB) (Figure 35) circuit is place is series with the current sense input, and PWM comparator. The LEB circuit masks the first 250 ns of the current sense signal.

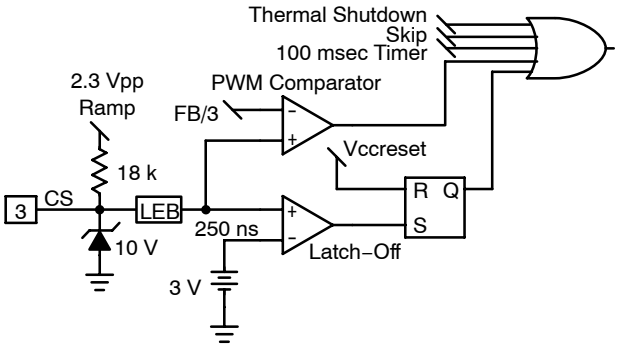


Figure 35.

Short−Circuit Condition

The NCP1231 is different from other controllers which uses auxiliary windings to detect events on the isolated secondary output. There maybe some conditions (for example when the leakage inductance is high) where it can be extremely difficult to implement short−circuit and overload protection. This occurs because when the power switch opens, the leakage inductance superimposes a large spike on the switch drain voltage. This spike is seen on the isolated secondary output and on the auxiliary winding. Because the auxiliary winding and diode form a peak rectifier, the auxiliary V_{CC} capacitor voltage can be charged up to the peak value rather than the true plateau which is proportional to the output level.

To resolve these issues the NCP1231 monitors the 1.0 V error flag. As soon as the internal 1.0 V error flag is asserted high, a 100 ms timer starts. If at the end of the 100 ms timeout period, the error flag is still asserted then the controller determines that there is a true fault condition and stops the PWM drive output, refer to Figure 36. When this occurs, V_{CC} starts to decrease because the power supply is locked out. When V_{CC} drops below UVLOlow (7.7 V typical), it enters a latch−off phase where the internal consumption is reduced down to 30 μA. This reduction in current allows the V_{CC} capacitor to be charged up through the external startup resistor, when V_{CC} reaches V_{CC}ON (12.6 V), the soft−start circuit is activated and the controller goes through a normal startup. If the fault has gone and the error flag is low, the controller resumes normal operations.

Under transient load conditions, if the error flag is asserted, the error flag will normally drop prior to the 100 ms timeout period and the controller continues to operate normally.

If the 100 msec timer expires while the NCP1231 is in the Skip Mode, SW1 opens and the PFC_Vcc output will shut down and will not be activated until the fault goes away and the power supply resumes normal operations.

While in the Skip Mode, to avoid any thermal runaway it is desirable for the skip duty cycle to be kept below 20%(the burst duty−cycle is defined as Tpulse / Tfault).

The latch−off phase can also be initiated, more classically, when V_{CC} drops below UVLO (7.7 V typical). During this fault detection method, the controller will not wait for the 100 ms time−out, or the error flag before it goes into the latch−off phase, operating in the skip mode under these conditions.

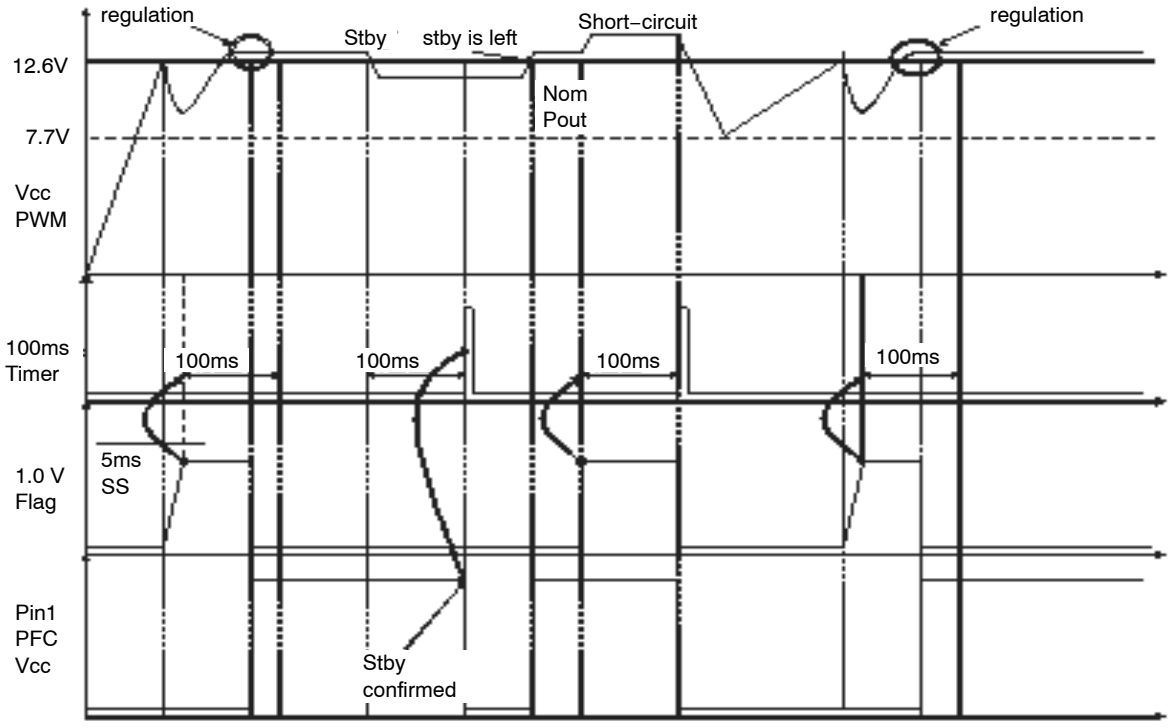


Figure 36.

Drive Output

The NCP1231 provides a Drive Output which can be connected through a current limiting resistor to the gate of a MOSFET. The Driver output is capable of delivering drive pulses with a rise time of 40 ns, and a fall time of 15 ns through its internal source and sink resistance of 12.3 ohms (typical), measured with a 1.0 nF capacitive load.

Startup Sequence

When the power supply is first connected to the mains outlet, current flows through Rstartup, charging the Vcc capacitor (refer to Figure 37). When the voltage on the Vcc capacitors reaches VccON level (typically 12.6 V), the NCP1231 then turns on the drive output to the external MOSFET in an attempt to increase the output voltage and charge up the Vcc capacitor through the Vaux winding in the transformer.

During the startup sequence, the controller pushes for the maximum peak current, which is reached after the 5 ms soft−start period (adjustable). As soon as the maximum peak set point is reached, the internal 1.0 V clamp actively limits the current amplitude to 1.0 V/Rsense and asserts an error flag indicating that a maximum current condition is being observed. In this mode, the controller must determine if it is a normal startup period (or transient load) or is the controller is facing a fault condition. To determine the difference between a normal startup sequence, and a fault condition, the error flag is asserted, and the 100 ms timer starts to count down. If the error flag drops prior to the 100 ms time−out period, the controller resets the timer and determines that it was a normal star−up sequence and enables the low impedance switch (SW1), enabling the PFC_Vcc output.

If at the end of the 100 ms period the error flag is still asserted, then the controller assumes that it is a fault condition and the PWM controller enters the skip mode and does not enable the PFC_Vcc output.

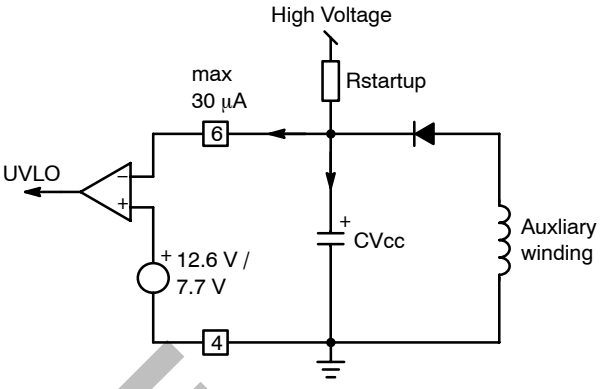


Figure 37.

Soft−Start

The NCP1231 features an adjustable soft−start circuit. As soon as Vcc reaches a nominal 12.6 V, the soft−start circuit is activated. The soft−start circuit output controls a reference on the minus (−) input to an amplifier (refer to Figure 38), the positive (+) input to the amplifier is the feedback input (divided by 3). The output of the amplifier drives a FET which clamps the feedback signal. As the soft−start circuit output ramps up, it allow the feedback pin input to the PWM comparator to gradually increased from near zero up to the maximum clamping level of 1 V/Rsense. This occurs over the entire 5 ms soft−start period until the supply enters regulation. The soft−start is also activated every time a restart is attempted. Figure 39 shows a typical soft−start up sequence (with soft−start), normal operation (frequency jittering), and a confirmed over load conditon (100 msec timeout).

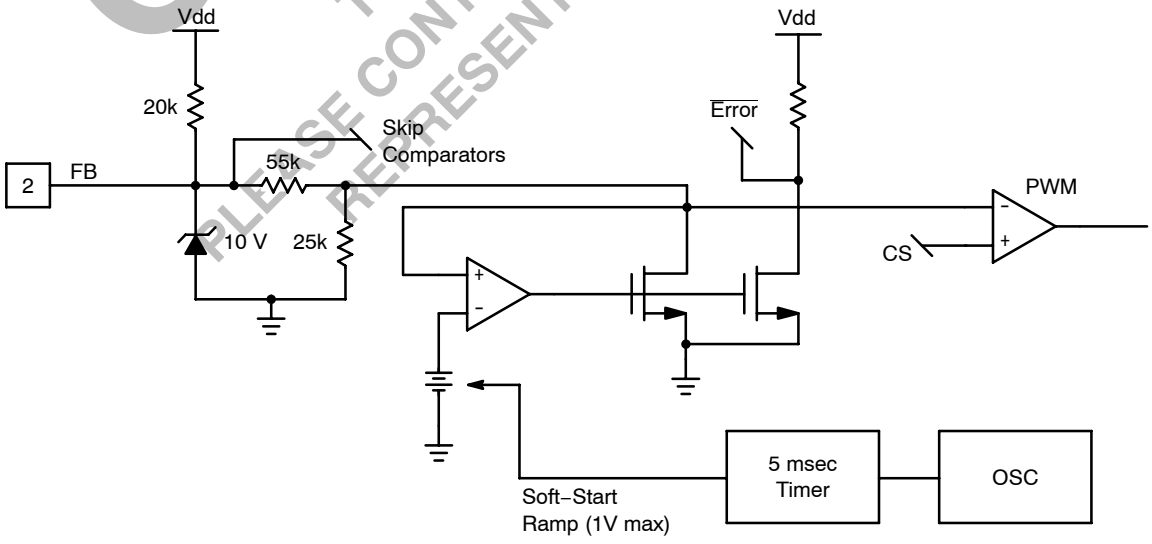


Figure 38.

Figure 39 shows the details of the internal circuitry implemented in the NCP1231. The NCP1231 Pin 7 can perform three different functions; 1) soft−start 2) EMI jittering and 3) short−circuit timeout (Fault Timer). The charge and discharge current sources are 60 μa (typical), so if a 82 nF capacitor is connected to Pin 7, one can achieve a typical soft−start of 5 ms, a frequency modulation of 5 ms and a fault timeout of 100 ms.

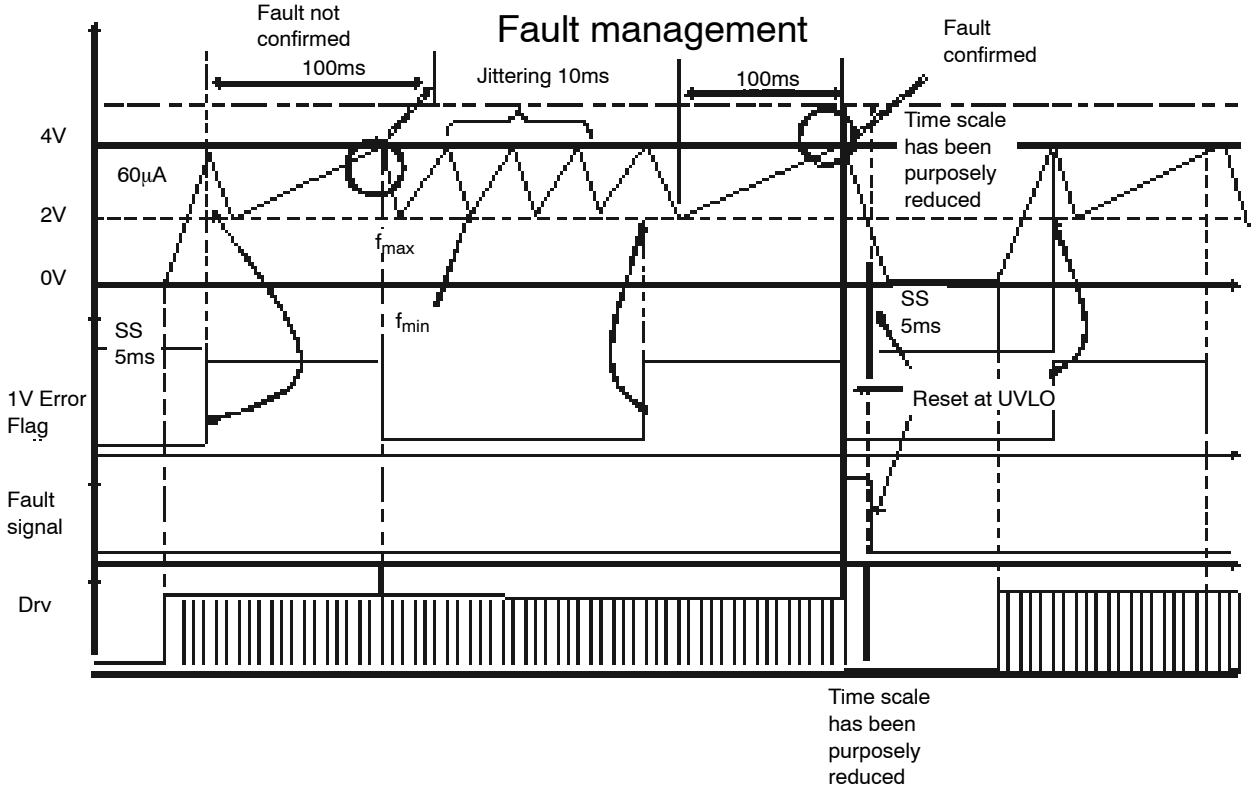


Figure 39. Soft−Start is Activated during a Startup Sequence an OCP Condition

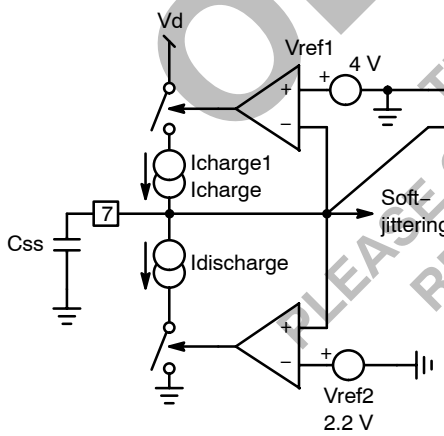


Figure 40. Internal Soft−Start, 100 msec Timer and Frequency Jittering

Frequency Jittering

Frequency jittering is a method used to soften the EMI signature by spreading out the average switching energy around the controller operating switching frequency. The NCP1231 offers a nominal ±4% deviation of the nominal switching frequency. The sweep sawtooth is internally generated and modulates the clock up and down with a 4 ms period. Figure 41 illustrates the NCP1231 behavior:

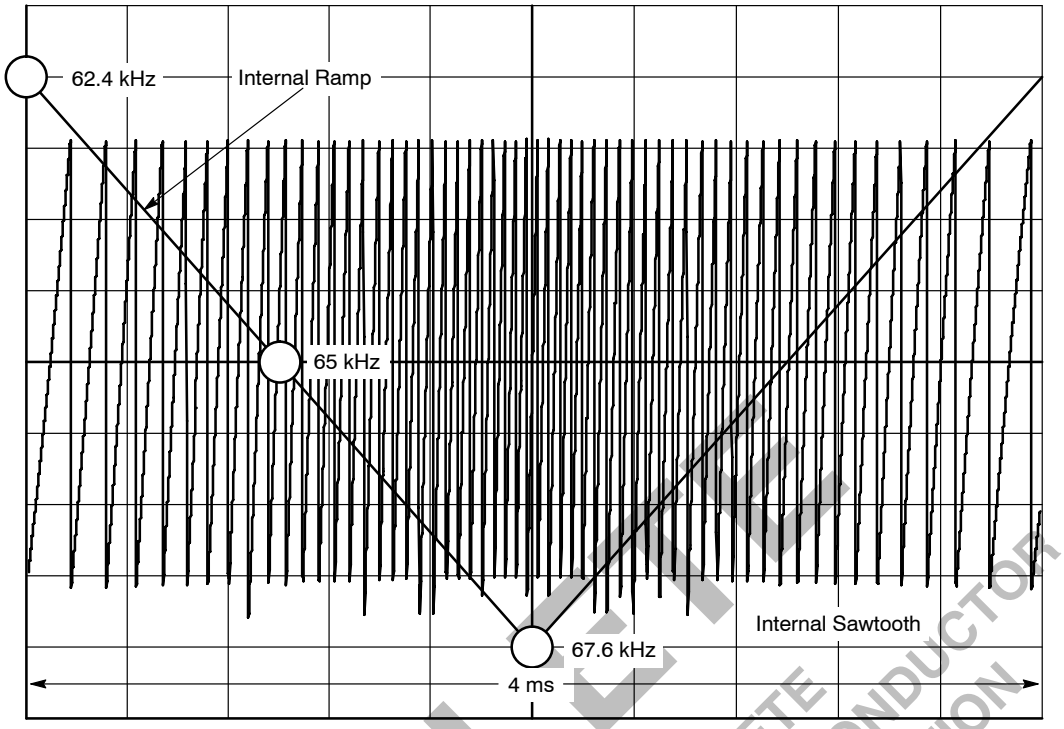
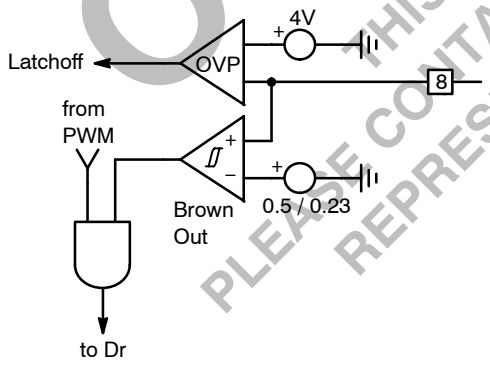


Figure 41. An Internal Ramp is used to Introduce Frequency Jittering on the Oscillator Saw Tooth

Overvoltage Protection

The NCP1231 combines an over and under−voltage protection on Pin 8. Figure 39 shows the internal component configuration inside the chip. When the voltage on Pin 8 is above 4.2 V then an OVP signal permanently latches off the controller; all output drive pulses are stopped and the Vcc Pin 6 ramps up and down between Vccon and Vccmin until the user unplugs the converter power allows Vcc to drop below Vccreset (4.0 V). By bringing Vcc down to the reset voltage (around 4.0 V), the latch is released and the IC can restart.



By arranging two comparators on the same pin, both OVP and under voltage sensing can be implemented.

Figure 42.

Brown−Out Protection

A Brown−Out (BO) protection feature prevents the power supply for being over stressed when the main input power drops below the typical universal input range of 85−265 Vac. When this occurs, the controller stops the drive output and waits for normal power to resume. Hysteresis is used on the BO comparators because the voltage on the bulk energy storage capacitor ripple voltage is affected by the input voltage and output power level. For this reason when BO comparator toggles, the internal reference changes from 500 mV to 230 mV. This effect is not latched, as soon as the input ac voltage in back within the normal operating range and the voltage on the bulk energy storage capacitor is back to normal range, the controller resume normal operation.

The lower threshold (VBLow) is the level at which the drive output is disabled. This level is dependent on the ripple voltage on Pin 8. A capacitor can be added between Pin 8 and ground to select the amount of ripple voltage. The larger the capacitor, the lower the ripple voltage, the greater the amount of hysteresis.

Thermal Protection

An internal Thermal Shutdown is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated (160 °C typically) the controller turns off the PWM Drive Output. When this occurs, Vcc will drop (the rate is dependent on the NCP1231 loading and the size of the Vcc capacitor) because the controller is no longer delivering drive pulses to the auxiliary winding charging up the Vcc capacitor. When Vcc drops below 4.0 volts and the Vccreset circuit is activated, the controller will restart. If the user is using a fixed bias supply (the bias supply is provided from a source other than from an auxiliary winding, refer to the typical application) and Vcc is not allow to drop below 4.0 volts under a thermal shutdown condition, the NCP1231 will not restart. This feature is provided to prevent catastrophic failure from accidentally overheating the device.

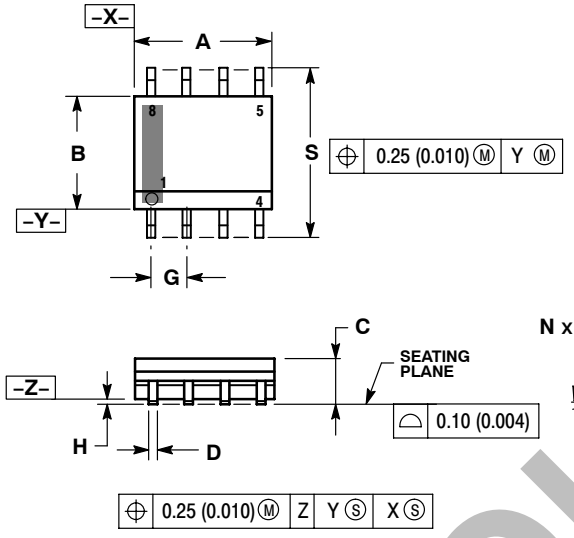
ORDERING INFORMATION

Device	Package	Shipping†
NCP1231D65R2	SOIC−8	2500/Tape & Reel
NCP1231D65R2G	SOIC−8 (Pb−Free)	
NCP1231D100R2	SOIC−8	
NCP1231D100R2G	SOIC−8 (Pb−Free)	
NCP1231D133R2	SOIC−8	
NCP1231D133R2G	SOIC−8 (Pb−Free)	
NCP1231P65	PDIP−8	50 Units/Rail
NCP1231P65G	PDIP−8 (Pb−Free)	
NCP1231P100	PDIP−8	
NCP1231P100G	PDIP−8 (Pb−Free)	
NCP1231P133	PDIP−8	
NCP1231P133G	PDIP−8 (Pb−Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

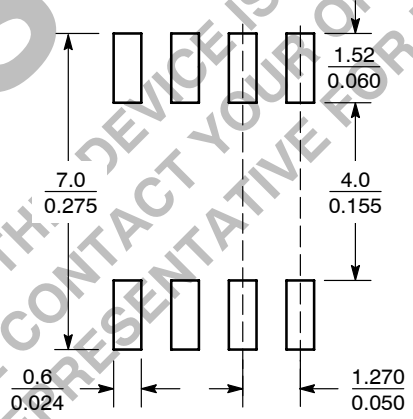
SOIC−8 NB
CASE 751−07
ISSUE AH



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*

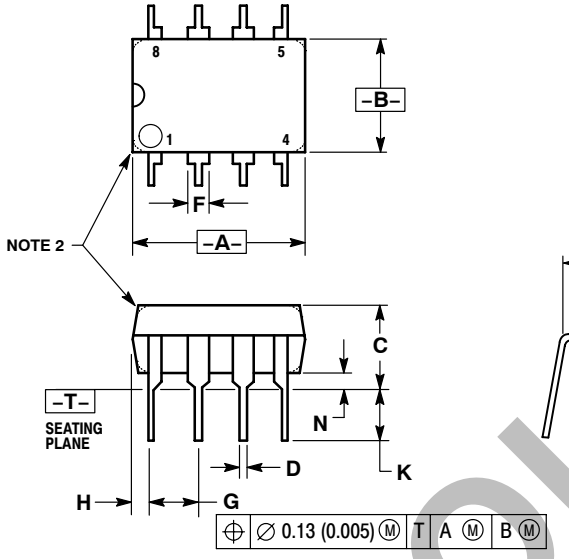


SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

8–LEAD PDIP
P SUFFIX
CASE 626–05
ISSUE L



NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	---	10°	---	10°
N	0.76	1.01	0.030	0.040

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