AND8082/D

ESD Protection for Dual USB 2.0 Port Using the Low Capacitance TVS Diode Array, NUP4201DR2 Device

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APPLICATION NOTE

ABSTRACT

Even though ESD protection is not yet required by the USB 1.1 and USB 2.0 specifications, it is extremely important and necessary that all USB ports have protection against ESD conditions because USB components are subject to electrostatic discharge conditions since USB is a hot plugging and unplugging system.

Our modern society has rapidly come to fully depend on electronics. And modern computers are based increasingly on low power logic chips, all with ESD sensitivity due to MOS dielectric breakdowns and bipolar reverse junction current limits. The USB ICs are not an exception since the majority of them are designed and manufactured based in CMOS processes which make them extremely sensitive to damage from ESD conditions. Because USB is a hot insertion and removal system, it is extremely vulnerable to receive ESD conditions possibly generated by the users or by air discharges. Users can induce ESD conditions while plugging or unplugging any USB peripherals. Air discharges can happen a few inches away from the conducting surface. Static electricity can cause damage to the USB interface, USB ICs malfunction, and worst of all, ghost data bits. Product damage or product malfunction results in a “Hard failure” or destroyed component. It is easy to isolate and replace the failed component and put the system back in service, however, if a “soft failure” occurs (CMOS component degraded), the system anomaly is not detected in retesting, and hours are wasted in troubleshooting because the system continues to produce irregular data bits, so this is why, ESD protection in USB components is now a MUST.

Through time, industrial standards have been developed to standardize the ESD compliance of semiconductor devices, some of the most common standards are described below:

- IEC 61000–4–2. This International Standard relates to the immunity requirements and test methods for electrical and electronic equipment subjected to static electricity discharges, from operators directly, and to adjacent objects.
- IEC 61000–4–4. This International Standard relates to the immunity requirements and test methods for electrical and electronic equipment subjected to EFT conditions.
- IEC 61000–4–5. This International Standard relates to the immunity requirements and test methods for electrical and electronic equipment subjected to Lighting conditions (surge 8 x 20 μsec).

ESD protection for USB components not only implicates compliance with the ESD industrial standards previously listed, but it also implicates the usage of very sophisticated semiconductor devices capable to operate under conditions of high speed data transmission and the high technology of the USB controller, so conventional methods to protect serial ports would be obsolete and non–efficient for USB applications.

Having said the implications of the ESD protection for USB components, it is possible to define what are the key characteristics that semiconductor devices intended for USB applications must have:

- Low capacitance (< 5.0 pf) to minimize the signal attenuation at *high speed data rate (480 Mbs, USB 2.0).*
- Fast time operation response (nanosecond) to protect the USB components against the fast rise time of the ESD pulses.
- Low leakage current to minimize the power consumption under normal operation conditions.
- Robustness to drive and absorb repetitive ESD conditions without damage.
- Integrated and reduced package.

The purpose of the present application note is to describe and explain in detail the usage and future of the *new Low Capacitance TVS Diode Array (NUP4201DR2 device)* to be used for ESD protection for either ***USB 2.0 or USB 1.1 components.***

NUP4201DR2 ON Semiconductor Device

ON Semiconductor has developed a unique Low Capacitance TVS Diode Array (NUP4201DR2 device) designed to protect sensitive electronics such as communications systems, computers, and computer peripherals against damage due to ESD conditions or transient voltage conditions. *Because of its very low capacitance array configuration, it can be used in high speed I/O data lines such as USB 2.0 components.*

The integrated design of the NUP4201DR2 offers surge rated, low capacitance steering diodes and a TVS diode integrated in a single package (SO–8). If a transient condition occurs, the steering diodes will drive the transient condition either to the positive polarity of the power supply or to ground. The TVS device protects the power line against overvoltage conditions to avoid damage in any downstream components. In addition to its low capacitance characteristics, the NUP4201DR2 from ON Semiconductor complies with the most common industrial standards for ESD Protection: IEC61000–4–2, IEC61000–4–4 and IEC61000–4–5.

Figure 1 shows the NUP4201DR2 device's schematic and the equivalent circuit of this device is shown in Figure 2.

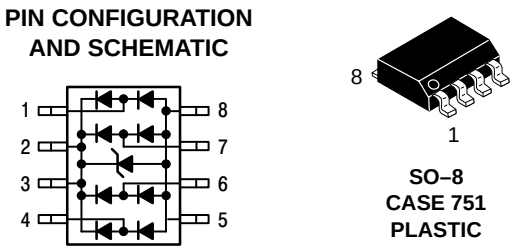


Figure 1. NUP4201DR2 Device's Schematic

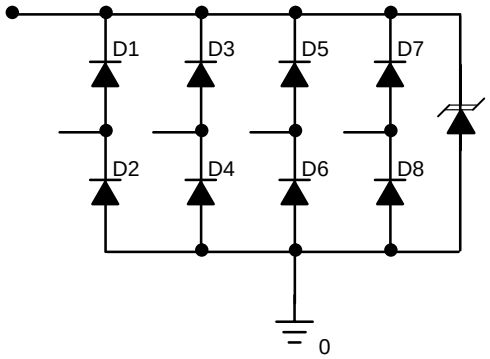


Figure 2. Equivalent Circuit of the NUP4201DR2 Device

DC Parameters

As previously mentioned, one of the most important characteristics that any device intended to be used for ESD protection in USB components is to have low leakage current to minimize the power consumption of the system. The NUP4201DR2 devices actually offer very low values of leakage current which make them fully useful for USB applications.

Table 1 shows some measurements of the dc parameters made in some NUP4201DR2 devices, the dc parameters of the NUP4201DR2 are the reverse breakdown voltage (VBR) and the reverse leakage current (IR).

Table 1. DC Parameter Measurements

Serial #	IR1 @ 5 V	IR2 @ 5 V	IR3 @ 5 V	IR4 @ 5 V	VZ1 @ 1 mA	VZ2 @ 1 mA	VZ3 @ 1 mA	VZ4 @ 1 mA
1	1.67E–07	1.65E–07	1.49E–07	1.64E–07	7.81	7.81	7.81	7.81
2	2.01E–07	1.67E–07	3.01E–07	1.57E–07	7.81	7.81	7.81	7.81
3	1.61E–07	1.51E–07	1.64E–07	1.22E–07	7.80	7.80	7.81	7.81
4	1.92E–07	1.24E–07	1.60E–07	1.49E–07	7.82	7.82	7.82	7.82
5	1.33E–07	1.40E–07	1.88E–07	1.25E–07	7.80	7.80	7.81	7.81
6	1.52E–07	1.22E–07	1.50E–07	1.27E–07	7.81	7.81	7.81	7.81
7	1.56E–07	1.49E–07	1.26E–07	1.51E–07	7.81	7.81	7.81	7.81
8	1.23E–07	1.51E–07	1.30E–07	1.24E–07	7.81	7.81	7.81	7.81
9	1.35E–07	1.24E–07	1.70E–07	1.27E–07	7.81	7.81	7.81	7.81
10	1.16E–07	1.35E–07	1.66E–07	1.92E–07	7.80	7.80	7.81	7.81
11	1.46E–07	1.35E–07	1.40E–07	1.33E–07	7.81	7.81	7.81	7.81
12	2.23E–07	1.25E–07	2.99E–07	1.52E–07	7.81	7.81	7.81	7.81
13	2.06E–07	1.27E–07	1.45E–07	1.56E–07	7.81	7.81	7.82	7.82
14	1.40E–07	1.92E–07	1.47E–07	1.23E–07	7.81	7.81	7.81	7.81
15	1.22E–07	1.33E–07	1.68E–07	1.64E–07	7.82	7.82	7.82	7.82
16	1.49E–07	1.52E–07	1.39E–07	1.60E–07	7.80	7.80	7.81	7.81
17	1.25E–07	1.56E–07	1.25E–07	1.64E–07	7.83	7.83	7.83	7.83
18	1.27E–07	1.23E–07	1.08E–07	1.60E–07	7.81	7.81	7.81	7.81
19	1.51E–07	1.35E–07	1.40E–07	1.88E–07	7.82	7.82	7.82	7.82
20	1.24E–07	1.16E–07	1.22E–07	1.50E–07	7.82	7.82	7.82	7.82
21	1.35E–07	1.46E–07	1.49E–07	1.26E–07	7.82	7.82	7.82	7.82
22	1.35E–07	1.92E–07	1.51E–07	1.30E–07	7.81	7.81	7.81	7.81
23	1.25E–07	1.33E–07	1.24E–07	1.70E–07	7.82	7.82	7.82	7.82
24	1.27E–07	1.52E–07	1.35E–07	1.40E–07	7.81	7.81	7.81	7.81
25	1.39E–07	1.25E–07	1.35E–07	1.22E–07	7.81	7.81	7.81	7.81

IR1, VZ1 measured from pin 1 to pin 5/8
IR2, VZ2 measured from pin 4 to pin 5/8
IR3, VZ3 measured from pin 6 to pin 5/8
IR4, VZ4 measured from pin 7 to pin 5/8

The previous data only shows typical values of the NUP4201DR2 device's DC characteristics, users should refer to the data sheet specifications for designing purposes.

Based in our data sheet specifications for V_{BR} and I_R, it's possible to observe that all devices showed results within spec.

Capacitance Between I/O Lines and Between I/O Lines and Ground

As previously mentioned, *"low capacitance (< 5.0 pf)"* is one of the most important characteristics that any device intended to be used in USB applications must have in order to minimize the signal attenuation at high speed data rate (480 Mbs, USB 2.0). This characteristic is critical, otherwise, the functionality of the USB system could be affected dramatically during high speed operation. Since the NUP4201DR2 is a low capacitance TVS diode array, it can be used either in USB 2.0 or USB 1.1 components. The following paragraphs describe the capacitance measurement between I/O lines and between I/O lines and ground.

Capacitance Measurement Between I/O Lines

This measurement needs to be made between two I/O pins, so different combinations can be made between different I/O lines pairs, however, for explanation purposes, it will be described in the measurement between pin 1 and pin 7 in Figures 3 and 4.

Conditions:
Frequency generator: 20 mVrms @ 1.0 MHZ
DC Bias: 0 V

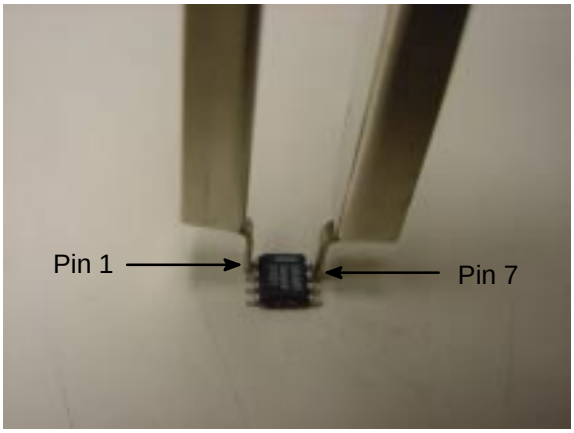


Figure 3. Measurement Between Pins 1 and 7

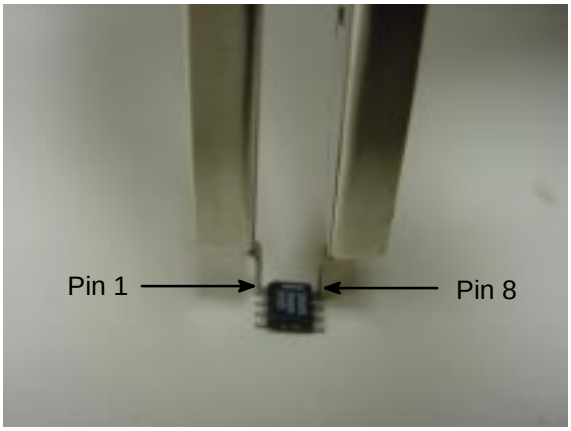


Figure 5. Measurement Between Pins 1 and 8

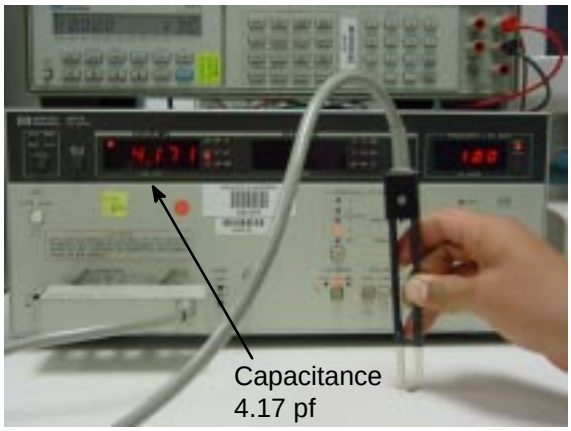


Figure 4. Capacitance Measurement Between I/O Lines

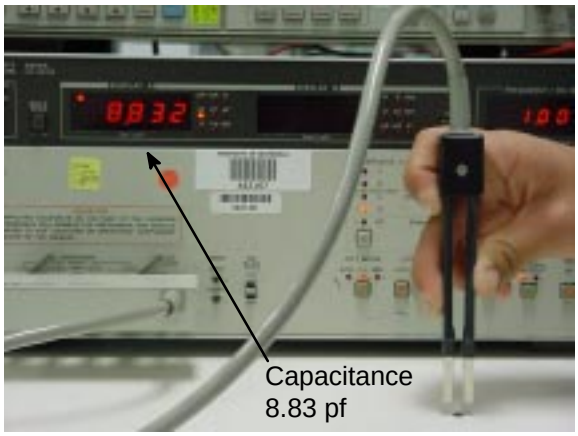


Figure 6. Capacitance Measurement Between I/O Lines and Ground

The total devices characterized showed an average capacitance value of around ***4.45 pf*** between I/O lines which complies with the USB 2.0 specification (5.0 pf maximum).

Capacitance Measurement Between I/O Lines and Ground

This measurement needs to be made between any of the I/O pins and ground, so different combinations can be made between the I/O lines and ground, however, for explanation purposes, it will be described in the measurement between pin 1 and pin 8 in Figures 5 and 6.

Conditions:

Frequency generator: 20 mVrms @ 1.0 MHZ
DC Bias: 0 V

The total devices characterized showed an average capacitance value of around ***8.9 pf*** between I/O lines and ground which complies with the USB 2.0 specification (10 pf maximum).

It is important to mention that all the capacitance measurements were made without supplying Vcc voltage to the devices since this is one of the most common standard methods for measuring capacitance, so if Vcc is applied to the parts, the capacitance is expected to be a little bit lower than 4.5 pf between I/O lines and 9.0 pf between I/O lines and ground. Also no PCB board was used in order to avoid parasitic inductance effects during the measurements.

Compliance with IEC 61000–4–2, ESD International Standard

IEC 61000–4–2, 8.0 KV (Contact)
IEC 61000–4–2, 15 KV (Air)

The IEC6100–4–2 International Standard relates to the immunity requirements and test methods for electrical and electronic equipment subjected to static electricity discharges, from operators directly, and to adjacent objects. It additionally defines ranges of test levels which relate to different environmental and installation conditions and establishes test procedures. The object of this standard is to establish a common and reproducible basis for evaluating the performance of electrical and electronic equipment when subjected to electrostatic discharges. In addition, it includes electrostatic discharges which may occur from personnel to objects near vital equipment.

The IEC6100–4–2 specification defines the preferential range of test levels for the ESD test which is described in Table 2.

Table 2. Test Levels

1a – Contact Discharge		1b – Air Discharge	
Level	**Test Voltage (KV)**	**Level**	**Test Voltage (KV)**
1	2.0	1	2.0
2	4.0	2	4.0
3	6.0	3	8.0
4	8.0	4	15
X*	special	X*	special
* “X” is an open level. The level has to be specified in the dedicated equipment specification. If higher voltages than those shown are specified, special test equipment may be needed.			

The IEC6100–4–2 specification also defines what should be the characteristics and performance of the ESD generator, these characteristics are listed below.

Specifications

- Energy Storage Capacitance (Cs + Cd): 150 pF ± 10%
- Discharge Resistance (Rd): 330 Ohms ± 10%
- Charging Resistance (Rc): between 50 Mohms and 100 Mohms
- Output Voltage (see Note 1): up to 8.0 kV (nominal) for contact discharge; up to 15 kV (nominal) for air discharge

NOTE:

1. Open circuit voltage measured at the energy storage capacitor.

Figure 7 illustrates the simplified diagram of the ESD generator. Figure 8 illustrates the typical waveform of the ESD generator (information taken from the IEC61000–4–2 spec):

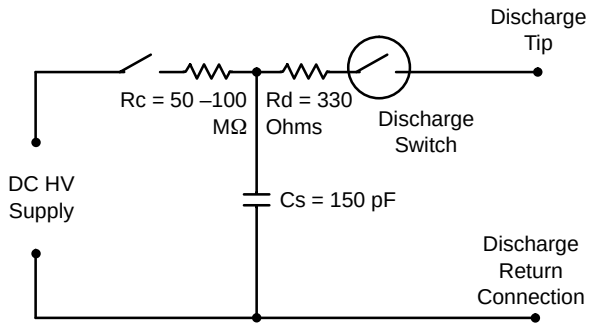


Figure 7. ESD Generator, Simplified Diagram

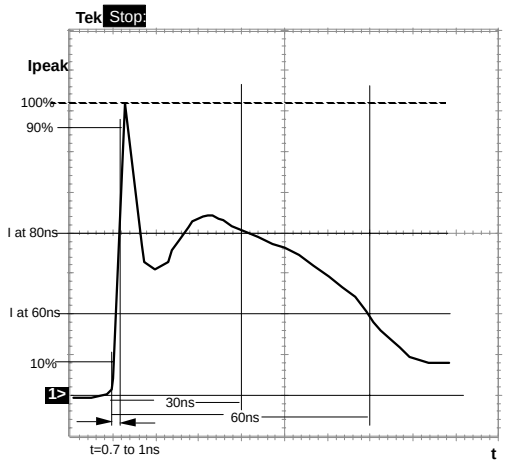


Figure 8. Typical Output’s Waveform of the ESD Generator

The equipment used for these ESD tests is shown in Figure 9. Figure 10 shows an oscilloscope plot that illustrates a real waveform sample taken from the output of this ESD generator.

Figure 9. ESD Generator, NoiseKen ESS−2000

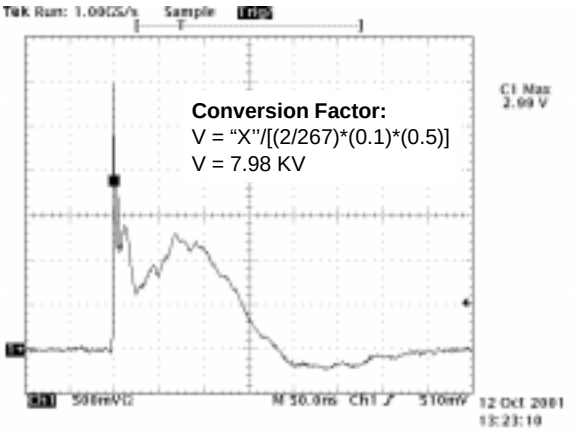


Figure 10. Real Waveform Sample Taken from ESD Generator

Some NUP4201DR2 devices were tested under the IEC6100−4−2 specifications (8.0 kV contact and 15 kV air) and the results observed are listed in Table 3.

Table 3. ESD Characterization Results

IEC Rating (10P) IEC 61000−4−2	Contact		Air	
	Serial Number	Pass/ Fail	Serial Number	Pass/ Fail
8.0 KV	1	P		
8.0 KV	2	P		
8.0 KV	3	P		
15 KV			4	P
15 KV			5	P
15 KV			6	P

NOTE: All the devices characterized under the IEC61000−4−2 conditions passed the test.

Compliance with IEC 61000–4–4, EFT International Standard

IEC 61000–4–4, 40 A (5/50 ns)

In this case, the IEC6100–4–4 International Standard relates to the immunity requirements and test methods for electrical and electronic equipment subjected to EFT conditions. The technical characteristics of the equipment used for these characterization purposes is described in Figure 11.

Technical Data

The PEFT Junior, has the following technical characteristics:

Impulse Shape

Definition in accordance with the standard IEC 1000–4–4 (IEC 801–4).

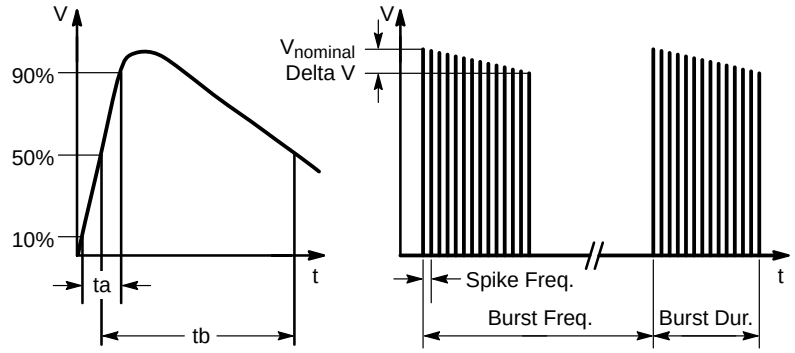


Figure 11. EFT Tester's Technical Characteristics

Voltage impulse form open circuit and into 50 Ω	ta tb	5.0 ns ± 30% 50 ns ± 30%
Output impedance	–	50 Ω ± 20%
Polarity	Polarity	Positive/Negative

Voltage Test Levels

Open circuit test voltage delta V for 75 impulses per burst	Vnominal Frequency = 10 kHz Frequency = 100 kHz Frequency = 1.0 MHz	0.22 to 4.5 kV ± 10% ≤ 1% ≤ 2% ≤ 10%

Figure 12 shows the EFT tester equipment.

Figure 12. EFT Generator

Some NUP4201DR2 devices were tested under the IEC6100–4–4 specification (40 A, 5/50 ns) and the results observed are listed in Table 4.

Table 4. EST Characterization Results

EFT IEC 61000–4–4 (3P)	Serial Number	Pass/Fail
40 A	7	P
40 A	8	P
40 A	9	P

NOTE: All the devices characterized under the IEC61000–4–4 conditions passed the test.

Compliance with IEC 61000–4–5, Lighting International Standard

IEC 61000–4–5 (Surge 8 x 20 μsec)

The IEC61000–4–5 International Standard relates to the immunity requirements and test methods for electrical and electronic equipment subjected to Lighting conditions (surge 8 x 20 μsec).

Figure 13 shows an oscilloscope plot that illustrates and describes an 8 x 20 μsec pulse condition.

This pulse is defined as double exponential since it is composed by two exponential factors, one of them defines the Rise time of the waveform (which in this case is 8.0 μsec) and the other one defines the decay time (which in this case is 20 μsec), this decay time is measured at 50% of the peak current value since it is the region in which the highest energy is dissipated.

According to the industrial standard IEC61000–4–5, this kind of waveform represents the waveform conditions generated due to lighting conditions.

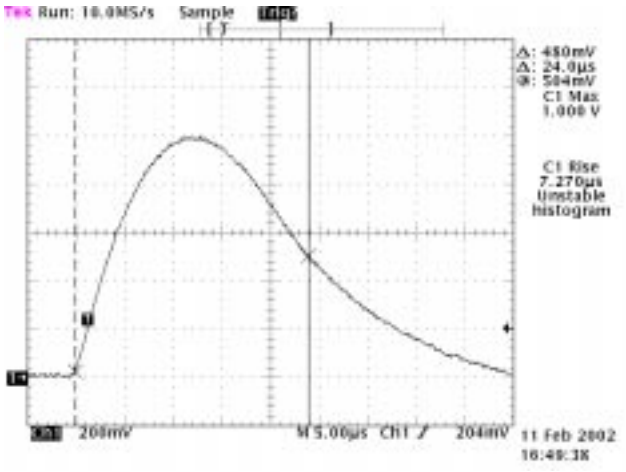


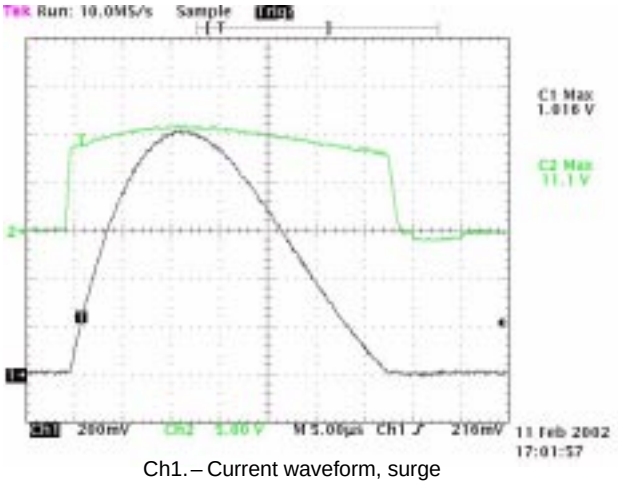
Figure 13. Double Exponential Pulse 8 x 20 μsec

For these characterization purposes, a standard surge generator (8 x 20 μsec waveform) known as KeyTek tester model 424 was used. The surge test pulse is applied to the device between any of its I/O lines and ground, and the measurements to be taken are the peak current value (Ipp) and the clamping voltage (Vc) in the device.

Our NUP4201DR2 devices specify two different conditions for clamping voltage (Vp), these conditions are shown below:

- 9.8 V Maximum @ IPP = 1.0 A (8 x 20 μsec waveform)
- 12 V Maximum @ IPP = 10 A (8 x 20 μsec waveform)

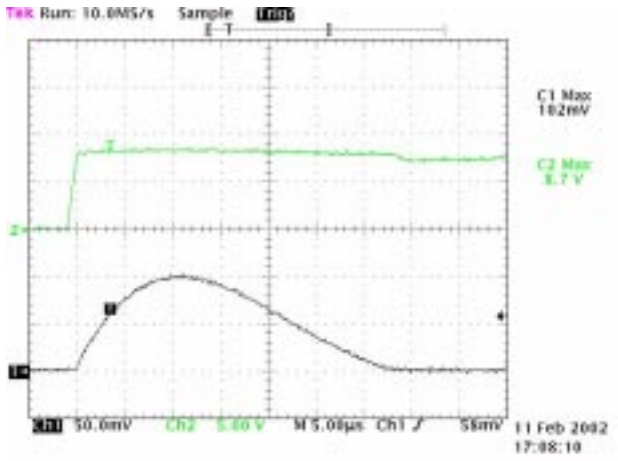
Figures 14 and 15 illustrate two oscilloscope waveforms that show the clamping voltage performance of our NUP4201DR2 devices when the two different current levels of surge 8 x 20 μsec are applied to them.



Ch1. – Current waveform, surge
8 x 20 μsec, IPP = 10.16 A
Ch2. – Clamping Voltage
Vc = 11.1 V

NOTE: The pulse current was measured with a current monitor with conversion factor of 100 mV = 1.0 Amp.

Figure 14.



Ch1. – Current waveform, surge
8 x 20 μsec, IPP = 1.02 A
Ch2. – Clamping Voltage
Vc = 8.7 V

NOTE: The pulse current was measured with a current monitor with conversion factor of 100 mV = 1.0 Amp.

Figure 15.

As shown in the above figures, our NUP4201DR2 devices showed a clamping voltage according to the specifications shown in the device's data sheet either for 1.0 A and 10 A of surge current 8 x 20 μsec.

In addition, it has been learned that most of the devices tested showed a higher peak power dissipation than 500 Watts (8 x 20 μsec pulse) before they failed, so it shows by itself that the surge capability of our NUP4201DR2 devices is high enough to cover and exceed our actual spec of 500 Watts. Some of the data taken is shown in Table 5.

Table 5. Surge 8 x 20 μsec Characterization Results

Serial #	Peak V	Peak I	PPK
1	30	79	2329
2	30	80	2365
3	30	78	2279
4	30	80	2366
5	29	80	2291

Upon the previous device's characterizations and studies, it has been shown that the NUP4201DR2 device from ON Semiconductor fully covers the main important features that any semiconductor products to be used in USB applications for ESD protection must have.

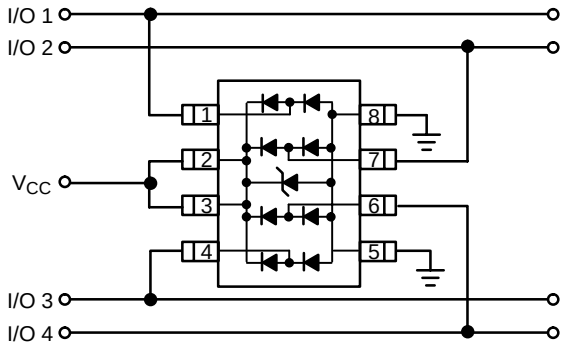
Typical Connection Schemes

The NUP4201DR2 is able to protect up to four data lines against transient overvoltage conditions by driving them to a fixed reference point for clamping purposes. The steering diodes will be forward biased whenever the voltage on the protected line exceeds the reference voltage (Vcc + Vf). The diodes will drive the transient current away from the sensitive circuit.

Data lines are connected at pins 1, 4, 6 and 7. The negative reference is connected at pins 5 and 8. These pins must be connected directly to ground by using a ground plane to minimize the PCB's ground inductance. It is very important to reduce as much as possible the PCB trace lengths to minimize parasitic inductances.

Scheme 1.

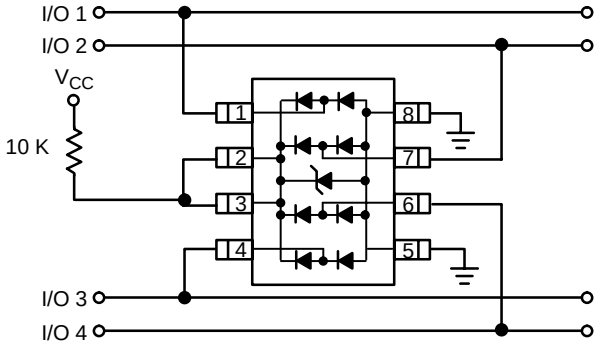
Four Data lines protection and power supply protection using Vcc as reference.



For this configuration, connect pins 2 and 3 directly to the positive supply rail (Vcc), the data lines are referenced to the supply voltage. The internal TVS diode prevents overvoltage on the supply rail.

Scheme 2.

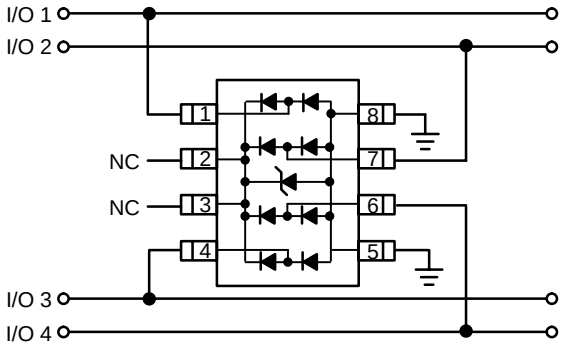
Four Data lines protection with Bias and power supply isolation resistor.



The NUP4201DR2 can be isolated from the power supply by connecting a series resistor between pins 2 and 3 and Vcc. A resistor of 10 Kohms is recommended for isolation purposes. The internal TVS and steering diodes remain biased, which provides the advantage of lower capacitance.

Scheme 3.

Four Data lines protection using internal TVS diode as reference.



In the case of applications in which a positive supply reference is not available or full isolation is required, the internal TVS could be used as the reference, so for this purpose, pins 2 and 3 are not connected. In this case, the steering diodes will conduct whenever the voltage on the protected line exceeds the working voltage of the TVS plus one diode drop ($Vc = Vf + V_{TVS}$).

ON Semiconductor's NUP4201DR2 provides a concept named "RailClamp" which is designed to eliminate the disadvantages of the usage of discrete diodes for ESD protection. The RailClamp concept is achieved with the integration of the TVS device, together with the steering diodes.

During an ESD condition, the ESD current will be driven to ground through the TVS device, so the resulting clamping voltage on the protected IC will be:

$$Vc = VF\ (RailClamp) + V_{TVS}.$$

The clamping voltage of the TVS device is shown as part of the specifications of the NUP4201DR2 data sheet. The clamping voltage will depend on the magnitude of the ESD current. The steering diodes are fast switching devices with unique forward voltage and low capacitance characteristics.

Typical Application Scheme for ESD Protection in USB Port

As known, a USB port is composed of four lines. The lines D+ & D– are used for bi–directional data transmission, and the remaining two lines are reserved for bus voltage and ground. Since USB is a hot plugging and unplugging system, all its four lines have the risk to receive ESD conditions in the real field of the application.

Typical ESD protection techniques are commonly formed by the combination of different discrete semiconductor products which make this technique obsolete and non–efficient because the interconnections of the discrete devices increase the parasitic inductance effects during a transient condition which reduces significantly the performance of the ESD protection circuit. The NUP4201DR2 provides a unique integrated Low Capacitance TVS Diode Array designed to protect multiple I/O lines and the power supply line against damage due to ESD conditions or transient voltage conditions. Because of its very low capacitance array configuration, it can be used in high speed I/O data lines such as USB 2.0 components. In addition to its low capacitance characteristics, the NUP4201DR2 device from ON Semiconductor complies with the most common industrial standards for ESD, EFT and surge protection: IEC61000–4–2, IEC61000–4–4, IEC61000–4–5.

Figure 16 illustrates how to connect the NUP4201DR2 to protect two USB ports.

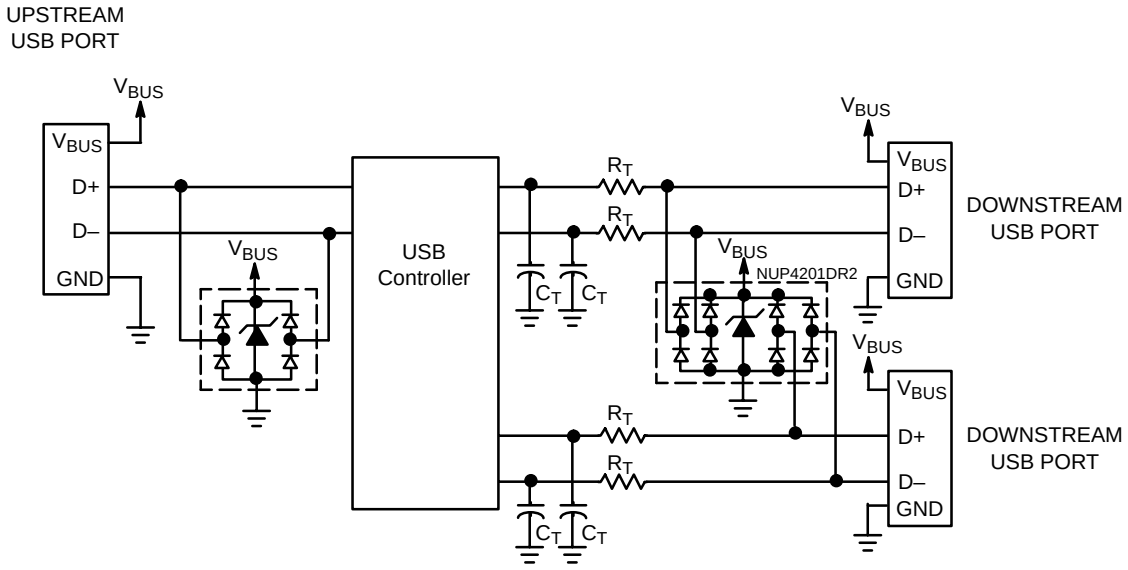


Figure 16. ESD Protection for USB Port

If a transient voltage condition occurs, the steering diodes drive the transient current away from the protected IC while the integrated TVS device drives the surge to ground. The TVS device will also suppress the ESD conditions induced on the voltage bus (V_{BUS}).

PCB Design Considerations

PCB design activities for USB applications is critical to meet the USB 2.0 and 1.1 requirements, so standard high frequency PCB design rules should be used in the layout to minimize any parasitic inductance and capacitance that may degrade the device's performance. It requires optimum component placement and good practices in circuit designing. Some general design guidelines are listed below to optimize the performance of the NUP4201DR2. Some of these guidelines were derived from the ON Semiconductor application note AND8026/D:

- Use ground planes to minimize the PCB's ground inductance.
- Critical signal lines should not be operated near board edges.
- D+ and D– signal line traces must not be operated near similar signal lines or high speed data–transferring lines.
- Locate the NUP4201DR2 device as close to the USB connector as possible to avoid transient coupling.
- Minimize the PCB trace lengths between the USB connector and the NUP4201DR2 device.
- Minimize the PCB trace lengths for the ground return connections.

Bibliography References

1. Universal Serial Bus Specifications, Revision 2.0, April 27, 2000.
2. International Standards IEC61000–4–2, IEC61000–4–4, IEC61000–4–5.
3. Forum Web Site: www.usb.org.com.
4. Article about ESD Considerations for Electronic Manufacturing by Donald E. Frank.
5. ON Semiconductor Application Note AND8026/D.

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