UMA4NT1, UMA6NT1

Preferred Devices

Dual Common Emitter Bias Resistor Transistors

PNP Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base−emitter resistor. These digital transistors are designed to replace a single device and its external resistor bias network. The BRT eliminates these individual components by integrating them into a single device. In the UMC2NT1 series, two BRT devices are housed in the SOT−353 package which is ideal for low power surface mount applications where board space is at a premium.

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- Available in 8 mm, 7 inch/3000 Unit Tape and Reel

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted, common for Q_1 and Q_2, − minus sign for Q_1 (PNP) omitted)

Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	50	Vdc
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector Current	I_C	100	mAdc

THERMAL CHARACTERISTICS

Thermal Resistance − Junction-to-Ambient (surface mounted)	$R_{\theta JA}$	833	°C/W
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to +150	°C
Total Package Dissipation @ T_A = 25°C (Note 1.)	P_D	150	mW

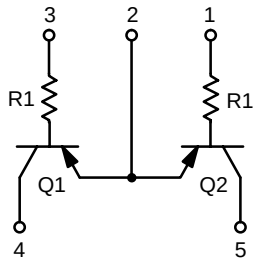
DEVICE MARKING AND RESISTOR VALUES

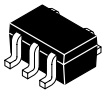
Device	Marking	R1 (K)	R2 (K)
UMA4NT1	U0	10	∞
UMA6NT1	U1	47	∞

1. Device mounted on a FR-4 glass epoxy printed circuit board using the minimum recommended footprint.

ON Semiconductor®

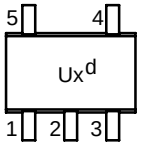
http://onsemi.com





SC−88A/SOT−353
CASE 419A
STYLE 7

MARKING DIAGRAM



Ux = Device Marking
x = 0 or 1
d = Date Code

ORDERING INFORMATION

Device	Package	Shipping†
UMA4NT1	SOT−323	3000/Tape & Reel
UMA6NT1	SOT−323	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Preferred devices are recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Base Cutoff Current (V_{CB} = 50 V, I_E = 0)		I_{CBO}	−	−	100	nAdc
Collector-Emitter Cutoff Current (V_{CB} = 50 V, I_B = 0)		I_{CEO}	−	−	500	nAdc
Emitter-Base Cutoff Current (V_{EB} = 6.0, I_C = 5.0 mA)	UMA4NT1 UMA6NT1	I_{EBO}	− −	− −	0.9 0.2	mAdc
ON CHARACTERISTICS						
Collector-Base Breakdown Voltage (I_C = 10 μA, I_E = 0)		$V_{(BR)CBO}$	50	−	−	Vdc
Collector-Emitter Breakdown Voltage (I_C = 2.0 mA, I_B = 0)		$V_{(BR)CEO}$	50	−	−	Vdc
DC Current Gain (V_{CE} = 10 V, I_C = 5.0 mA)	UMA4NT1 UMA6NT1	h_{FE}	160 160	250 250	− −	
Collector−Emitter Saturation Voltage (I_C = 10 mA, I_B = 0.3 mA)		$V_{CE(SAT)}$	−	−	0.25	Vdc
Output Voltage (on) (V_{CC} = 5.0 V, V_B = 2.5 V, R_L = 1.0 kΩ)		V_{OL}	−	−	0.2	Vdc
Output Voltage (off) (V_{CC} = 5.0 V, V_B = 0.5 V, R_L = 1.0 kΩ)		V_{OH}	4.9	−	−	Vdc
Input Resistor	UMA4NT1 UMA6NT1	R1	7.0 33	10 47	13 61	kΩ

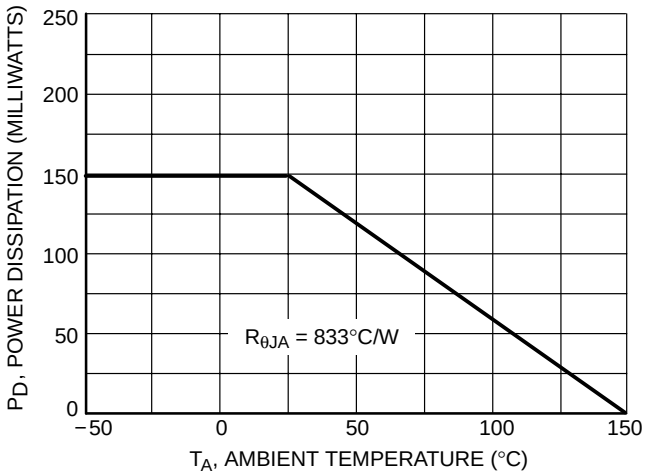


Figure 1. Derating Curve

TYPICAL ELECTRICAL CHARACTERISTICS − UMA4NT1

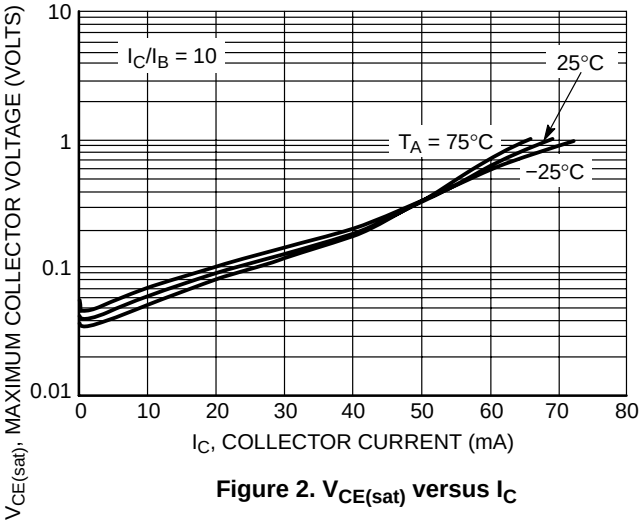


Figure 2. $V_{CE(sat)}$ versus I_C

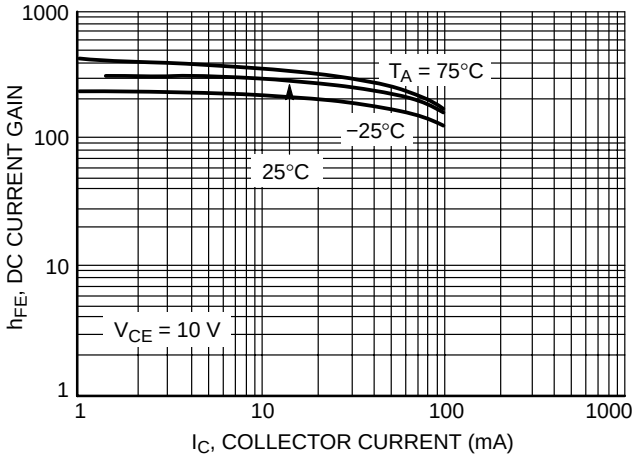


Figure 3. DC Current Gain

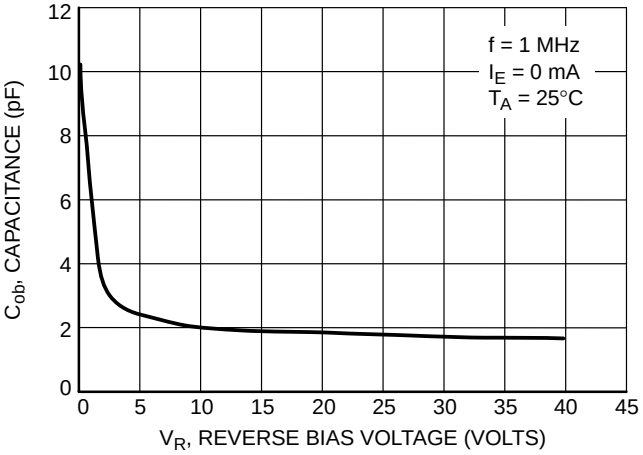


Figure 4. Output Capacitance

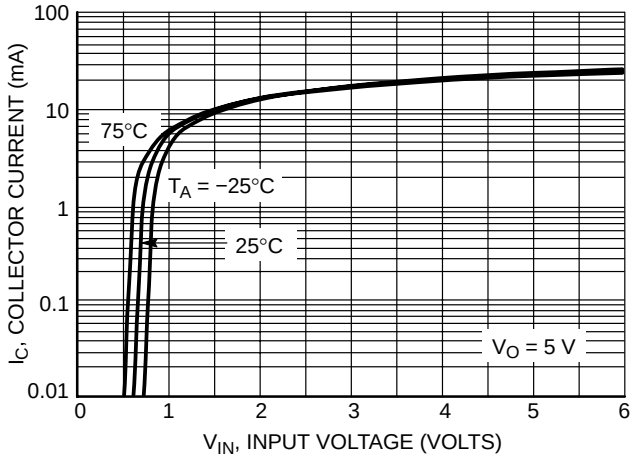


Figure 5. Output Current versus Input Voltage

TYPICAL ELECTRICAL CHARACTERISTICS − UMA6NT1

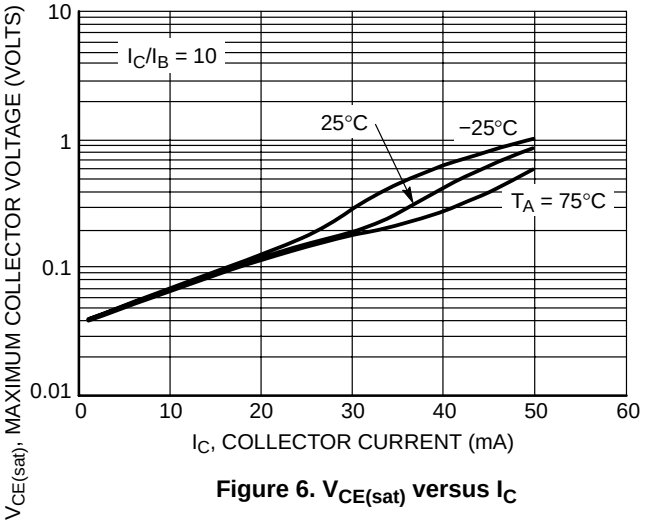


Figure 6. $V_{CE(sat)}$ versus I_C

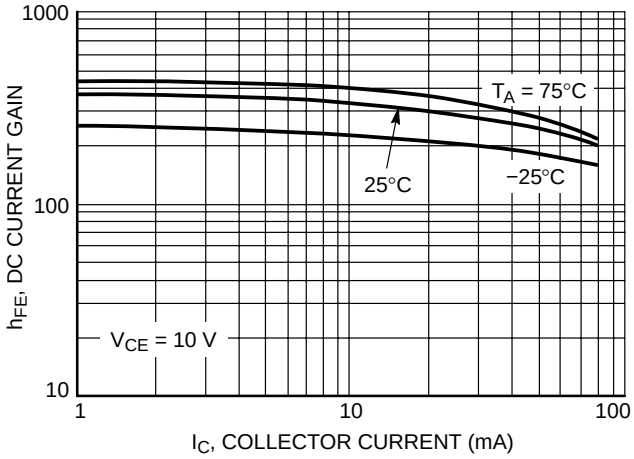


Figure 7. DC Current Gain

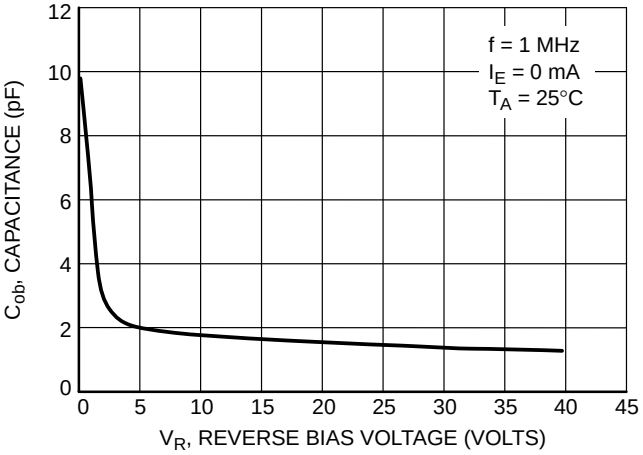


Figure 8. Output Capacitance

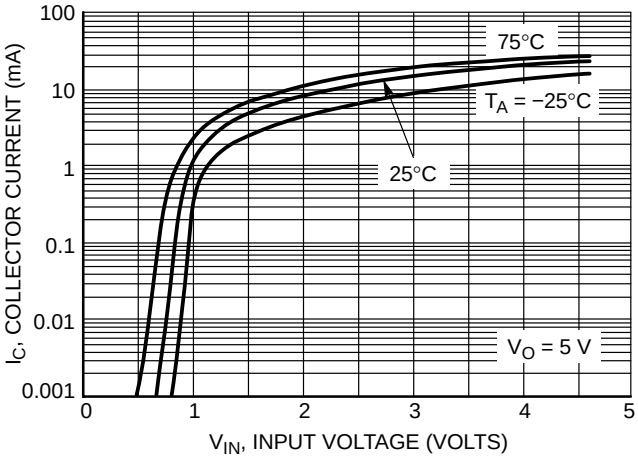
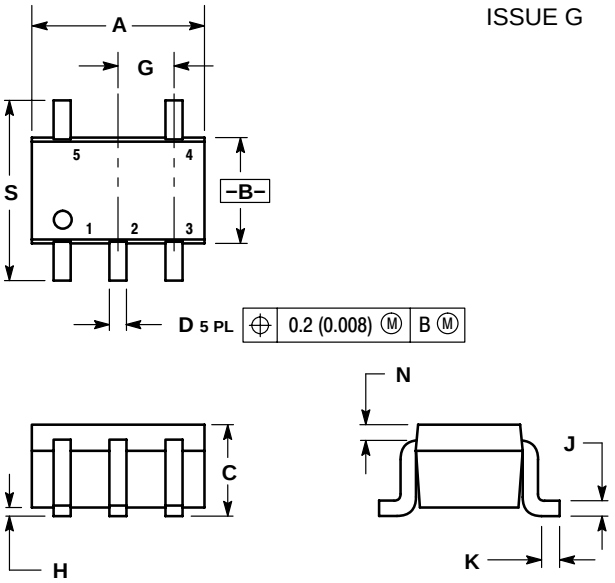


Figure 9. Output Current versus Input Voltage

PACKAGE DIMENSIONS

SC−88A/SOT−353
5−LEAD PACKAGE
CASE 419A−02
ISSUE G

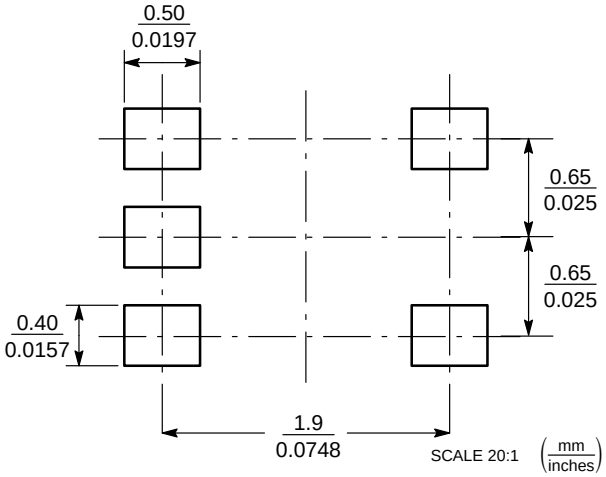


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

STYLE 7:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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UMA4NT1/D