MMBV2101LT1 Series, MV2105, MV2101, MV2109, LV2205, LV2209

Silicon Tuning Diodes

6.8–100 pF, 30 Volts
Voltage Variable Capacitance Diodes

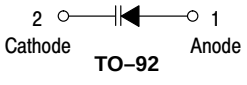
ON Semiconductor™

http://onsemi.com

These devices are designed in popular plastic packages for the high volume requirements of FM Radio and TV tuning and AFC, general frequency control and tuning applications. They provide solid–state reliability in replacement of mechanical tuning methods. Also available in a Surface Mount Package up to 33 pF.

- High Q
- Controlled and Uniform Tuning Ratio
- Standard Capacitance Tolerance – 10%
- Complete Typical Design Curves

SOT–23



TO–92

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Reverse Voltage		V_R	30	Vdc
Forward Current		I_F	200	mAdc
Forward Power Dissipation		P_D		mW
@ T_A = 25°C	MMBV21xx		225	mW/°C
Derate above 25°C			1.8	
@ T_A = 25°C	MV21xx		280	
Derate above 25°C	LV22xx		2.8	
Junction Temperature		T_J	+150	°C
Storage Temperature Range		T_{stg}	–55 to +150	°C

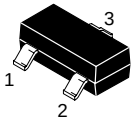
DEVICE MARKING

MMBV2101LT1 = M4G	MMBV2108LT1 = 4X	MV2109 = MV2109
MMBV2103LT1 = 4H	MMBV2109LT1 = 4J	LV2205 = LV2205
MMBV2105LT1 = 4U	MV2101 = MV2101	LV2209 = LV2209
MMBV2107LT1 = 4W	MV2105 = MV2105	

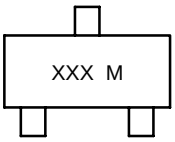
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μAdc)	$V_{(BR)R}$				Vdc
MMBV21xx, MV21xx		30	–	–	
LV22xx		25	–	–	
Reverse Voltage Leakage Current (V_R = 25 Vdc, T_A = 25°C)	I_R	–	–	0.1	μAdc
Diode Capacitance Temperature Coefficient (V_R = 4.0 Vdc, f = 1.0 MHz)	TC_C	–	280	–	ppm/°C

MARKING DIAGRAM

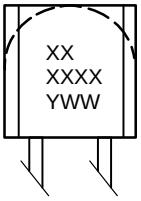


TO–236AB, SOT–23
CASE 318–08
STYLE 8



XXX = Device Code*
M = Date Code
* See Table

TO–226AC, TO–92
CASE 182
STYLE 1



XX = Device Code Line 1*
XXXX = Device Code Line 2*
M = Date Code
* See Table

Preferred devices are recommended choices for future use and best overall value.

Device	C_T, Diode Capacitance V_R = 4.0 Vdc, f = 1.0 MHz pF			Q, Figure of Merit V_R = 4.0 Vdc, f = 50 MHz	TR, Tuning Ratio C_2/C_{30} f = 1.0 MHz		
	Min	Nom	Max	Typ	Min	Typ	Max
MMBV2101LT1/MV2101	6.1	6.8	7.5	450	2.5	2.7	3.2
MMBV2103LT1	9.0	10	11	400	2.5	2.9	3.2
LV2205/MMBV2105LT1/MV2105	13.5	15	16.5	400	2.5	2.9	3.2
MMBV2107LT1	19.8	22	24.2	350	2.5	2.9	3.2
MMBV2108LT1	24.3	27	29.7	300	2.5	3.0	3.2
LV2209MMBV2109LT1/MV2109	29.7	33	36.3	200	2.5	3.0	3.2

MMBV2101LT1, MMBV2103LT1, MMBV2105LT1, MMBV2107LT1 thru MMBV2109LT1, are also available in bulk. Use the device title and drop the "T1" suffix when ordering any of these devices in bulk.

PARAMETER TEST METHODS

1. C_T, DIODE CAPACITANCE

($C_T = C_C + C_J$). C_T is measured at 1.0 MHz using a capacitance bridge (Boonton Electronics Model 75A or equivalent).

2. TR, TUNING RATIO

TR is the ratio of C_T measured at 2.0 Vdc divided by C_T measured at 30 Vdc.

3. Q, FIGURE OF MERIT

Q is calculated by taking the G and C readings of an admittance bridge at the specified frequency and substituting in the following equations:

$$Q = \frac{2\pi fC}{G}$$

(Boonton Electronics Model 33AS8 or equivalent). Use Lead Length $\approx$ 1/16".

4. TC_C, DIODE CAPACITANCE TEMPERATURE COEFFICIENT

TC_C is guaranteed by comparing C_T at V_R = 4.0 Vdc, f = 1.0 MHz, T_A = –65°C with C_T at V_R = 4.0 Vdc, f = 1.0 MHz, T_A = +85°C in the following equation, which defines TC_C:

$$TC_C = \left|\frac{C_T(+85°C) - C_T(-65°C)}{85 + 65}\right| \cdot \frac{10^6}{C_T(25°C)}$$

Accuracy limited by measurement of C_T to ±0.1 pF.

TYPICAL DEVICE CHARACTERISTICS

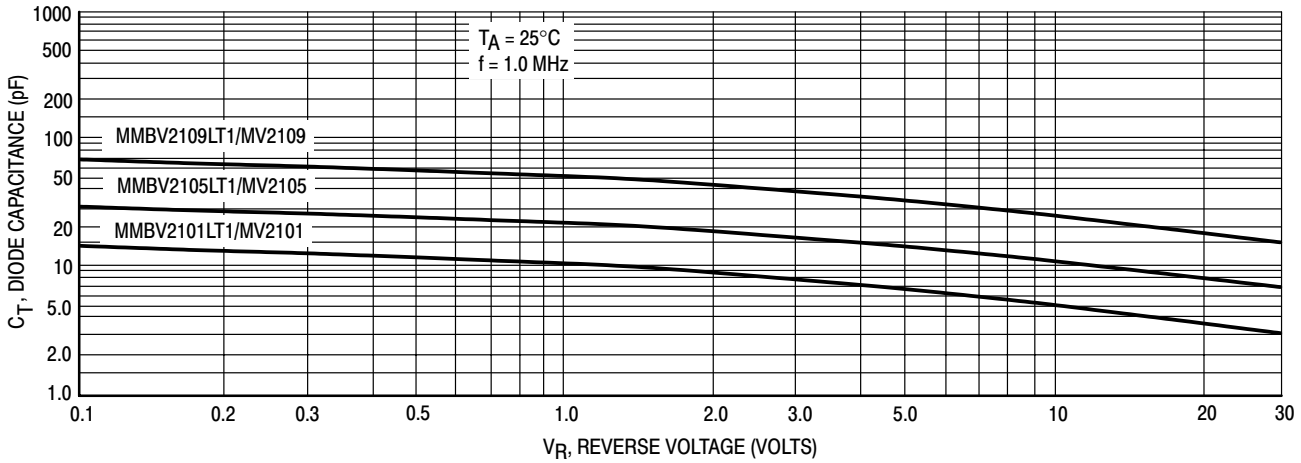


Figure 1. Diode Capacitance versus Reverse Voltage

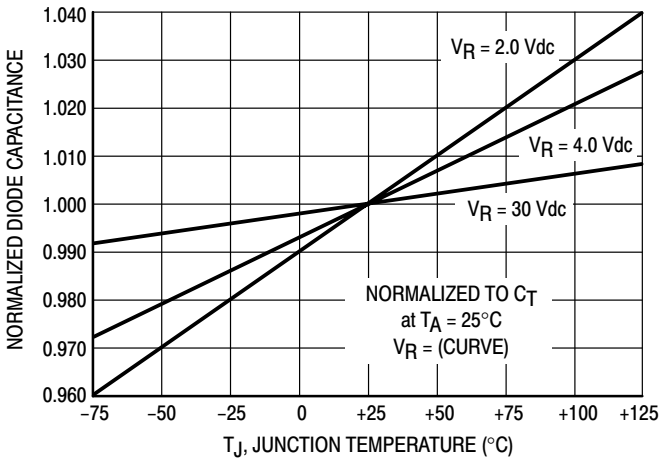


Figure 2. Normalized Diode Capacitance versus Junction Temperature

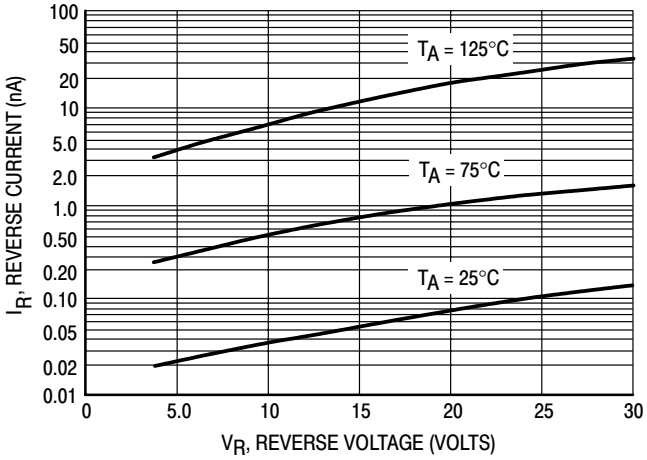


Figure 3. Reverse Current versus Reverse Bias Voltage

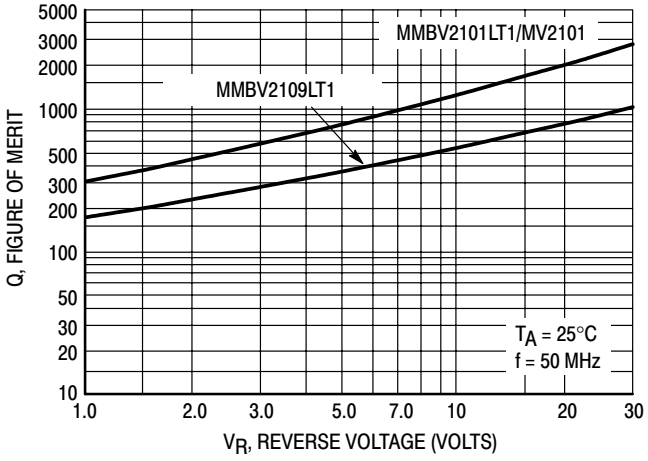


Figure 4. Figure of Merit versus Reverse Voltage

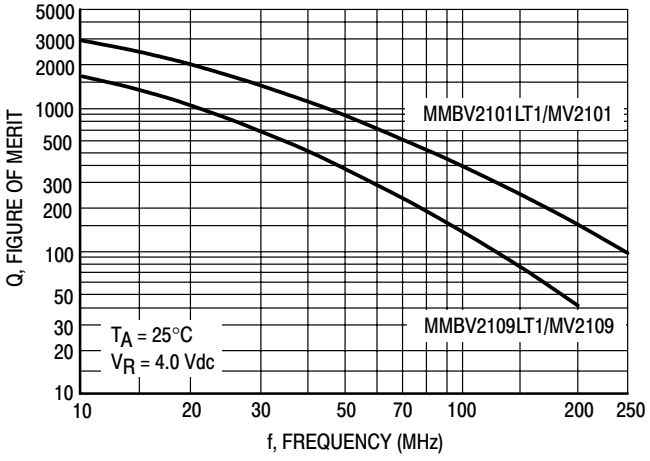
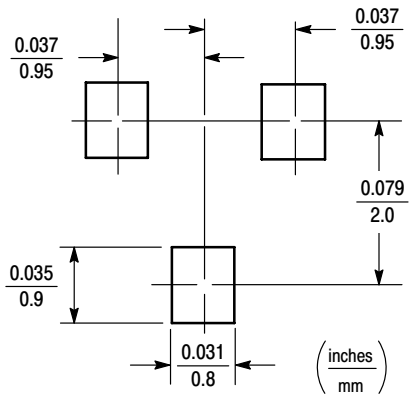


Figure 5. Figure of Merit versus Frequency

INFORMATION FOR USING THE SOT–23 SURFACE MOUNT PACKAGE

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



SOT–23

SOT–23 POWER DISSIPATION

The power dissipation of the SOT–23 is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A. Using the values provided on the data sheet for the SOT–23 package, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device which in this case is 225 milliwatts.

$$P_D = \frac{150°C - 25°C}{556°C/W} = 225 \text{ milliwatts}$$

The 556°C/W for the SOT–23 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 225 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT–23 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. A solder stencil is required to screen the optimum amount of solder paste onto the footprint. The stencil is made of brass or stainless steel with a typical thickness of 0.008 inches.

The stencil opening size for the surface mounted package should be the same as the pad size on the printed circuit board, i.e., a 1:1 registration.

TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 7 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

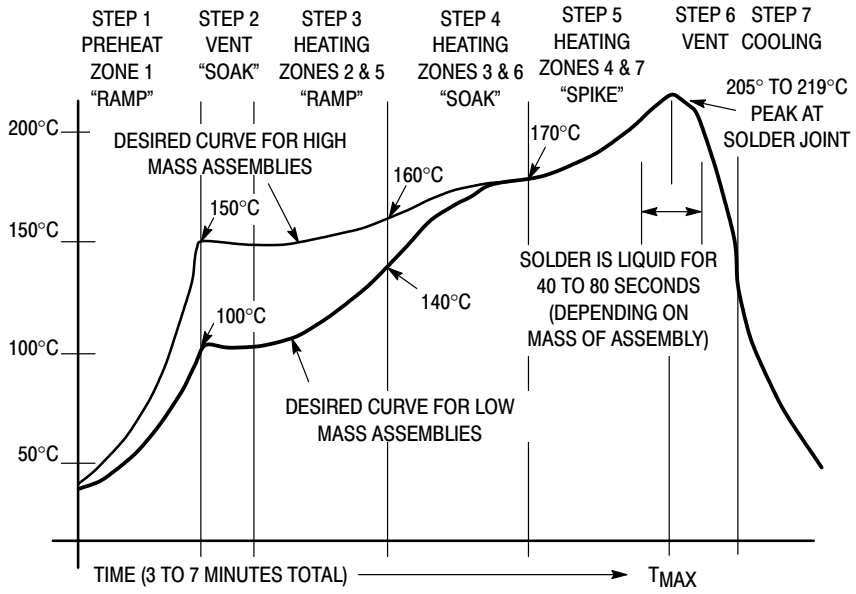
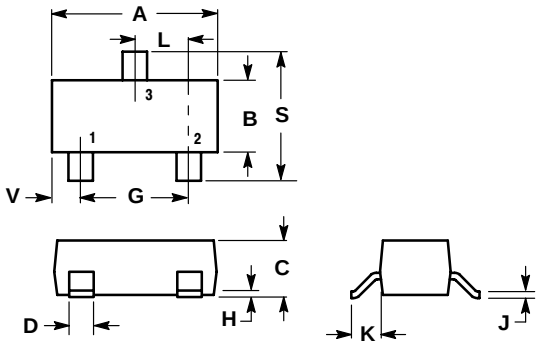


Figure 6. Typical Solder Heating Profile

PACKAGE DIMENSIONS

SOT−23 (TO−236AB)
CASE 318−08
ISSUE AF



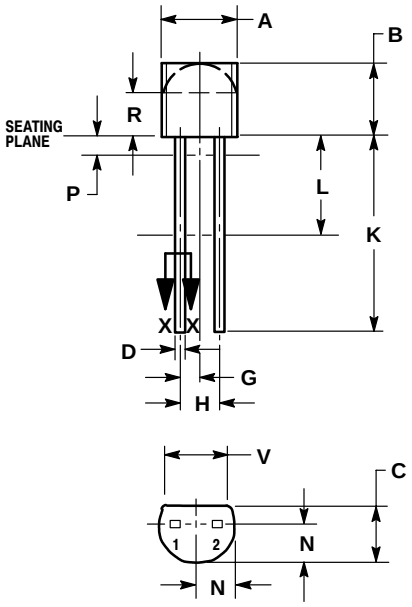
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

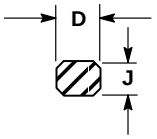
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0140	0.0285	0.35	0.69
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.1039	2.10	2.64
V	0.0177	0.0236	0.45	0.60

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

PACKAGE DIMENSIONS

TO–92 (TO–226AC)
CASE 182–06
ISSUE L





SECTION X–X

STYLE 1:
PIN 1. ANODE
2. CATHODE

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND ZONE R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.21
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.021	0.407	0.533
G	0.050 BSC		1.27 BSC	
H	0.100 BSC		2.54 BSC	
J	0.014	0.016	0.36	0.41
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.03	2.66
P	---	0.050	---	1.27
R	0.115	---	2.93	---
V	0.135	---	3.43	---

Thermal Clad is a trademark of the Bergquist Company.

PUBLICATION ORDERING INFORMATION

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Email: r14525@onsemi.com

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