# MJB44H11 (NPN), MJB45H11 (PNP)

Preferred Devices

## **Complementary Power Transistors**

## D<sup>2</sup>PAK for Surface Mount

... for general purpose power amplification and switching such as output or driver stages in applications such as switching regulators, converters and power amplifiers.

- Low Collector–Emitter Saturation Voltage V<sub>CE(sat)</sub> = 1.0 V (Max) @ 8.0 A
- Fast Switching Speeds
- Complementary Pairs Simplifies Designs
- Epoxy Meets UL 94, V-O @ 0.125 in
- ESD Ratings: Human Body Model, 3B > 8000 V Machine Model, C > 400 V

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V <sub>CEO</sub>	80	Vdc
Emitter-Base Voltage	V <sub>EB</sub>	5	Vdc
Collector Current – Continuous – Peak	Ι <sub>C</sub>	10 20	Adc
Total Power Dissipation @ T <sub>C</sub> = 25°C Derate above 25°C	P <sub>D</sub>	50 1.67	Watts W/°C
Total Power Dissipation @ T <sub>A</sub> = 25°C Derate above 25°C	P <sub>D</sub>	2.0 0.016	Watts W/°C
Operating and Storage Junction Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	–55 to 150	°C

#### THERMAL CHARACTERISTICS

Characteristic	Symbol	Мах	Unit	
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W	
Thermal Resistance, Junction to Ambient	$R_{\thetaJA}$	75	°C/W	

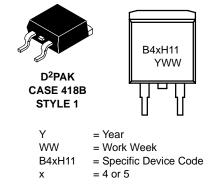


## ON Semiconductor®

http://onsemi.com

SILICON POWER TRANSISTORS 10 AMPERES 80 VOLTS 50 WATTS





## ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>	
MJB44H11	D <sup>2</sup> PAK	50 Units/Rail	
MJB44H11T4	D <sup>2</sup> PAK	800/Tape & Reel	
MJB45H11	D <sup>2</sup> PAK	50 Units/Rail	
MJB45H11T4	D <sup>2</sup> PAK	800/Tape & Reel	

+For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

**Preferred** devices are recommended choices for future use and best overall value.

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## **ELECTRICAL CHARACTERISTICS** ( $T_C = 25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Min	Тур	Max	Unit	
DFF CHARACTERISTICS				•		•
Collector–Emitter Sustaining Voltage $(I_C = 30 \text{ mA}, I_B = 0)$		V <sub>CEO(sus)</sub>	80	-	_	Vdc
Collector Cutoff Current ( $V_{CE}$ = Rated $V_{CEO}$ , $V_{BE}$ = 0)		I <sub>CES</sub>	-	-	10	μΑ
Emitter Cutoff Current (V <sub>EB</sub> = 5 Vdc)		I <sub>EBO</sub>	-	_	50	μΑ
ON CHARACTERISTICS						•
Collector–Emitter Saturation Voltage $(I_C = 8 \text{ Adc}, I_B = 0.4 \text{ Adc})$		V <sub>CE(sat)</sub>	-	_	1.0	Vdc
Base–Emitter Saturation Voltage $(I_C = 8 \text{ Adc}, I_B = 0.8 \text{ Adc})$		V <sub>BE(sat)</sub>	-	_	1.5	Vdc
DC Current Gain (V <sub>CE</sub> = 1 Vdc, I <sub>C</sub> = 2 Adc)		h <sub>FE</sub>	60	_	-	-
DC Current Gain (V <sub>CE</sub> = 1 Vdc, I <sub>C</sub> = 4 Adc)			40	_	_	
DYNAMIC CHARACTERISTICS						
Collector Capacitance (V <sub>CB</sub> = 10 Vdc, f <sub>test</sub> = 1 MHz)	MJB44H11 MJB45H11	C <sub>cb</sub>		130 230		pF
Gain Bandwidth Product ( $I_C = 0.5$ Adc, $V_{CE} = 10$ Vdc, f = 20 MHz)	MJB44H11 MJB45H11	f <sub>T</sub>		50 40		MHz
SWITCHING TIMES						
Delay and Rise Times ( $I_C = 5 \text{ Adc}, I_{B1} = 0.5 \text{ Adc}$ )	MJB44H11 MJB45H11	t <sub>d</sub> + t <sub>r</sub>	- -	300 135		ns
Storage Time ( $I_C = 5 \text{ Adc}, I_{B1} = I_{B2} = 0.5 \text{ Adc}$ )	MJB44H11 MJB45H11	t <sub>s</sub>	-	500 500	-	ns
Fall Time ( $I_C = 5 \text{ Adc}, I_{B1} = I_{B2} = 0.5 \text{ Adc}$ )	MJB44H11 MJB45H11	t <sub>f</sub>		140 100		ns

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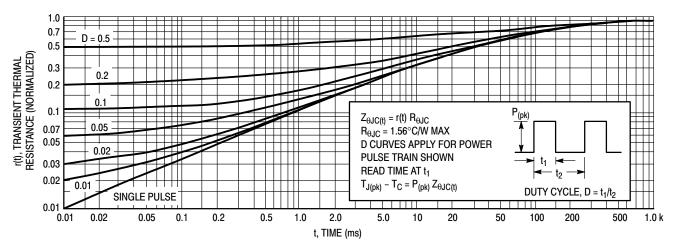


Figure 1. Thermal Response

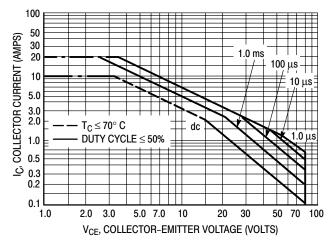
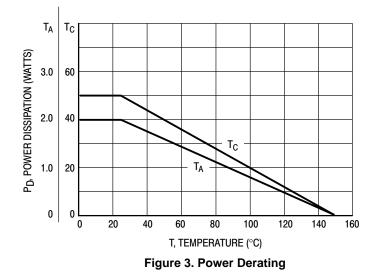


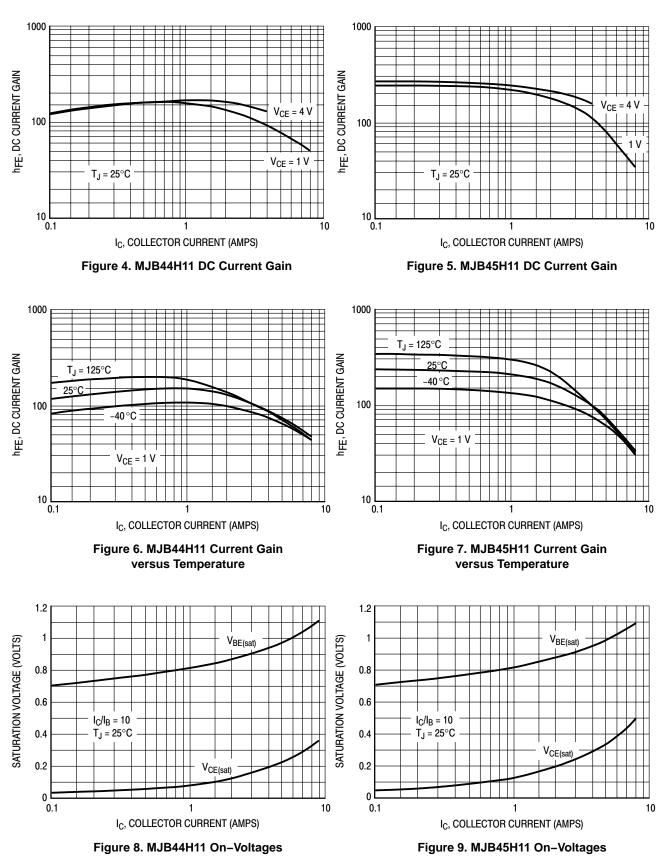
Figure 2. Maximum Rated Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on  $T_{J(pk)} = 150^{\circ}$ C;  $T_{C}$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \le 150^{\circ}$ C.  $T_{J(pk)}$  may be calculated from the data in Figure 1. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

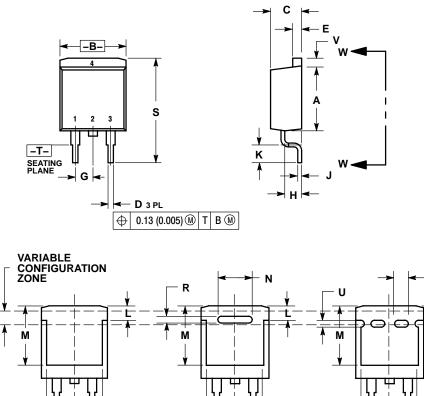


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## PACKAGE DIMENSIONS





F

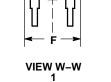
VIEW W-W

NOTES:

NOTES: 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: INCH. 3. 418B–01 THRU 418B–03 OBSOLETE, NEW STANDARD 418B–04.

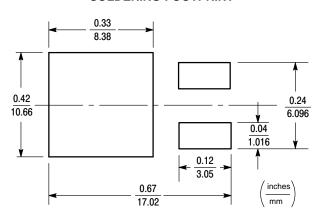
	INC	1150		ETERS	
	INCHES		MILLIMETERS		
DIM	MIN	MAX	MIN	MAX	
Α	0.340	0.380	8.64	9.65	
В	0.380	0.405	9.65	10.29	
С	0.160	0.190	4.06	4.83	
D	0.020	0.035	0.51	0.89	
Е	0.045	0.055	1.14	1.40	
F	0.310	0.350	7.87	8.89	
G	0.100 BSC		2.54 BSC		
Н	0.080	0.110	2.03	2.79	
J	0.018	0.025	0.46	0.64	
κ	0.090	0.110	2.29	2.79	
L	0.052	0.072	1.32	1.83	
М	0.280	0.320	7.11	8.13	
Ν	0.197 REF		5.00 REF		
Ρ	0.079 REF		2.00 REF		
R	0.039 REF		0.99 REF		
S	0.575	0.625	14.60	15.88	
٧	0.045	0.055	1.14	1.40	

STYLE 1: PIN 1. BASE 2. COLLECTOR 3. EMITTER 4. COLLECTOR





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\*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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