AND8090/D

AC Characteristics of ECL Devices

ON Semiconductor®

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APPLICATION NOTE

APPLICATION NOTE USAGE

This application note provides a general overview of the AC characteristics that are specified on the ON Semiconductor data sheets for MECL 10K™, 10H™, 100H, ECLinPS™, ECLinPS Lite™, and GigaComm™ SiGe devices. Data sheet information takes precedence over this application note if there are differences. This application note includes the following information:

- AC Test Bench Information
- AC Characteristic Definitions
- AC Characteristic Test Methods
- AC Characteristic Examples
- AC Characteristic Symbols
- AC Characteristic References

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LAB TESTING

Test Bench Overview

Specialized test benches are used to determine the AC characteristics of the Device−Under−Test (DUT). A typical test bench setup for a differential device is shown in Figure 1.

Test Initialization

- The test cables are connected from the pulse generator to the appropriate DUT test board input connectors.
- The test cables are connected from the DUT test board output connectors to the appropriate digital sampling oscilloscope input connectors.
- The power supply cables are connected to the DUT test board power supply connectors.
- The airflow regulator is set to 500 lfpm and the desired DUT ambient air temperature. The DUT is in this environment for a minimum of 3 minutes before testing begins. Data sheet specifications are typically given for −40°C, 25°C, and 85°C.

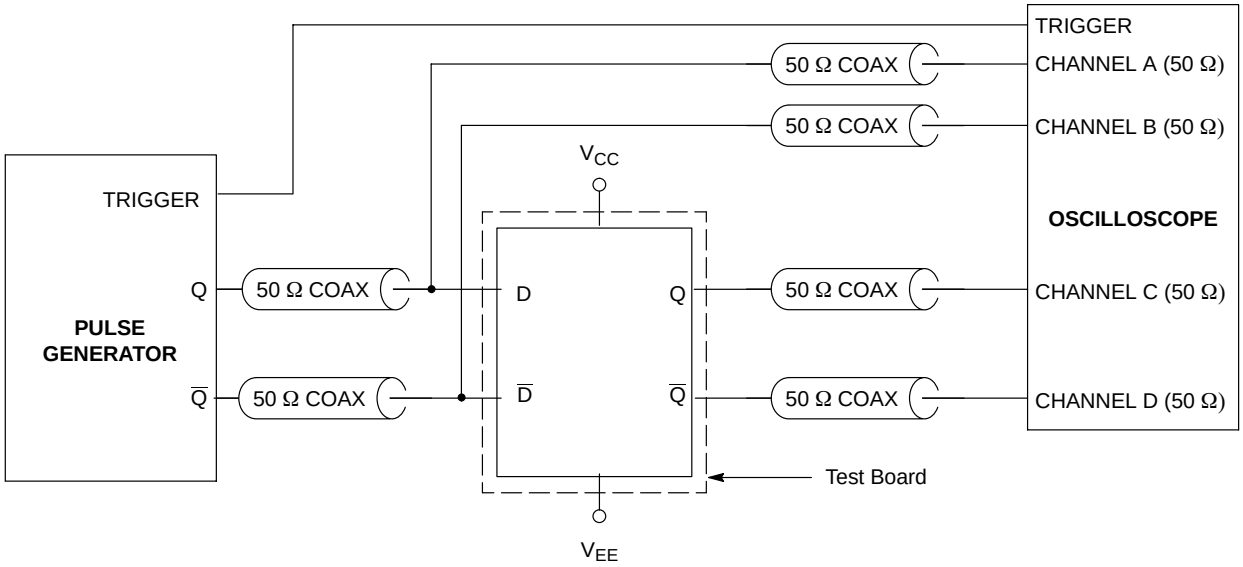


Figure 1. AC Characterization Test Bench Setup

Test Bench Equipment

AC characterization equipment is carefully selected to ensure that the test equipment is suitable for the devices to be tested, and that the measurements are accurate and repeatable. For example, sampling head bandwidth must be wide enough for accurate rise and fall time measurements. The test equipment that is currently used by ON Semiconductor is listed in Table 1. Further information on the test equipment can be found at the respective manufacturer's website.

Table 1. ON Semiconductor Test Bench Equipment

Test Equipment	Manufacturer/Model	Equipment Notes
Digital Sampling Oscilloscope	Tektronix 11801C SD24/26 20 GHz Module	Customers can use lower performance equipment for evaluation, but may not be able to duplicate all of ON Semiconductor measurements (e.g., rise/fall and propagation delay times).
Digital Sampling Oscilloscope	Tektronix TDS8000 80E03 20 GHz Module 80E01 50 GHz Module	Customers can use lower performance equipment for evaluation, but may not be able to duplicate all of ON Semiconductor measurements (e.g., rise/fall and propagation delay times). Note that the 50 GHz sampling module is required for GigaComm devices as they typically have rise and fall times between 20 ps and 50 ps.
Pulse/Pattern Generators	Tektronix HFS 9009	Maximum pulse frequency of 630 MHz.
	Agilent 8133A	Maximum pulse frequency of 3.0 GHz.
	Advantest D3186	Maximum pulse frequency of 12 GHz.
DC Power Supplies	Agilent HP6624A	Used to supply V_{CC}, V_{EE}, and specialized bias voltages. Low−resistance supply voltage connections and RF quality supply filter capacitors are designed into the AC test boards that are used to mount the DUT.
Test Cables	Various Manufacturers	High bandwidth, low−loss matched cables are used to ensure accurate measurements. Each cable of an input/output cable pair is the same length and has a characteristic impedance of 50 ohms.
Air Flow Regulator	Temptronics Thermostream	Establishes the DUT ambient temperature.

AC Test Boards

Each test device is mounted on a controlled impedance test board that is specifically designed to measure AC characteristics. Test boards typically have multiple layers. An example of an AC characteristic test board is shown in Figures 2 through 4. This particular test board is used to test ECLinPS Lite™ SOIC−8 devices.

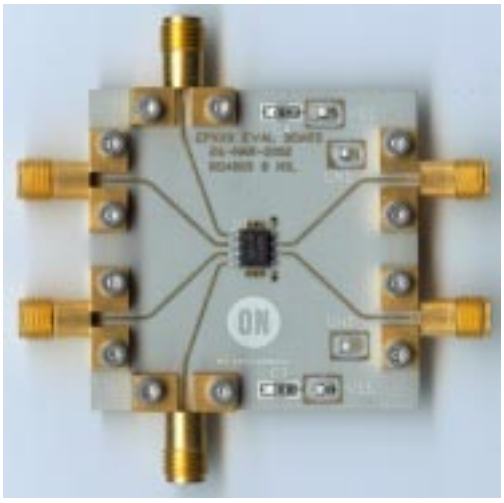


Figure 2. Top Photo of the AC Test Board

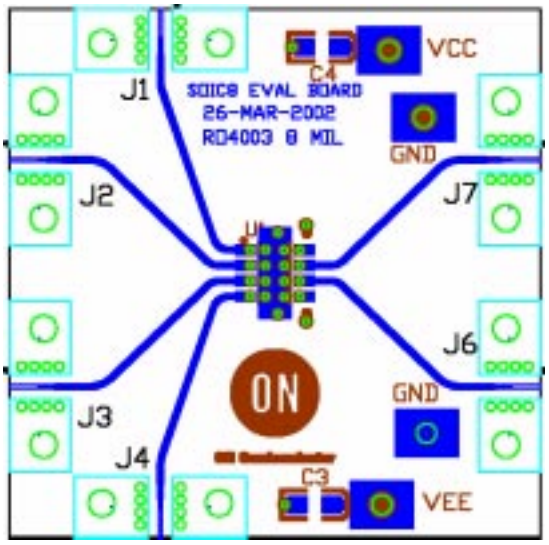


Figure 3. Top Schematic of the AC Test Board

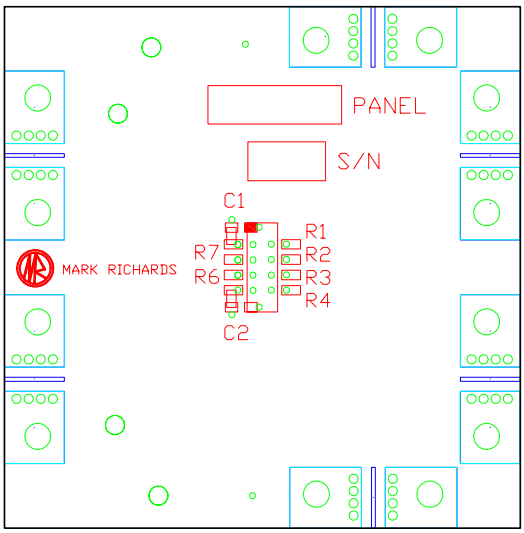


Figure 4. Bottom Schematic of the AC Test Board

SIGNAL LEVELS

AC HIGH and LOW Levels − The HIGH level referred to in this application note corresponds to the IEEE “topline,” and the LOW level corresponds to the IEEE “baseline” as shown in Figure 5. The 50% point lies halfway between the HIGH and LOW levels. Refer to IEEE Standard 194−1977 for further voltage level information.

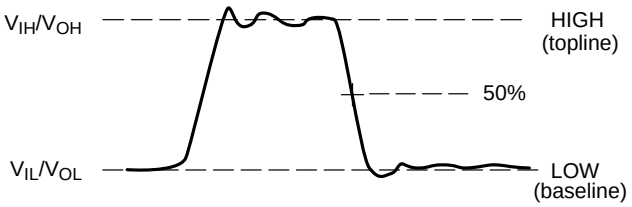


Figure 5. HIGH and LOW Waveform Definition

Input Levels − Operational differential input levels are specified by V_{PP} and the V_{IHCMR} range as described in the “Differential Characteristics” section. Operational single−ended input levels are specified by V_{IL} and V_{IH} as described in the “Single−Ended Characteristics” section.

Output Levels − Output signals may be differential or single−ended. AC characteristics for ON Semiconductor devices with ECL outputs are typically measured for an output termination of 50 Ω to V_{TT} (the termination voltage equal to V_{CC} − 2.0 V). HIGH and LOW output levels range between the boundary and threshold values for the respective HIGH and LOW input levels specified on data sheets. Output logic levels are shown in Figure 6.

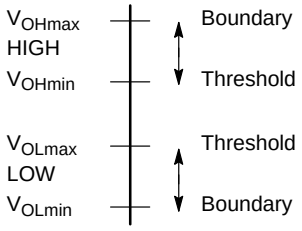


Figure 6. Output Logic Levels

Oscilloscope Averaging − Digital sampling oscilloscopes use an algorithm to determine the average level over a pulse width to establish the HIGH and LOW levels. An example is shown in Figure 7. The horizontal cursors at the HIGH and LOW levels indicate the determined average levels.

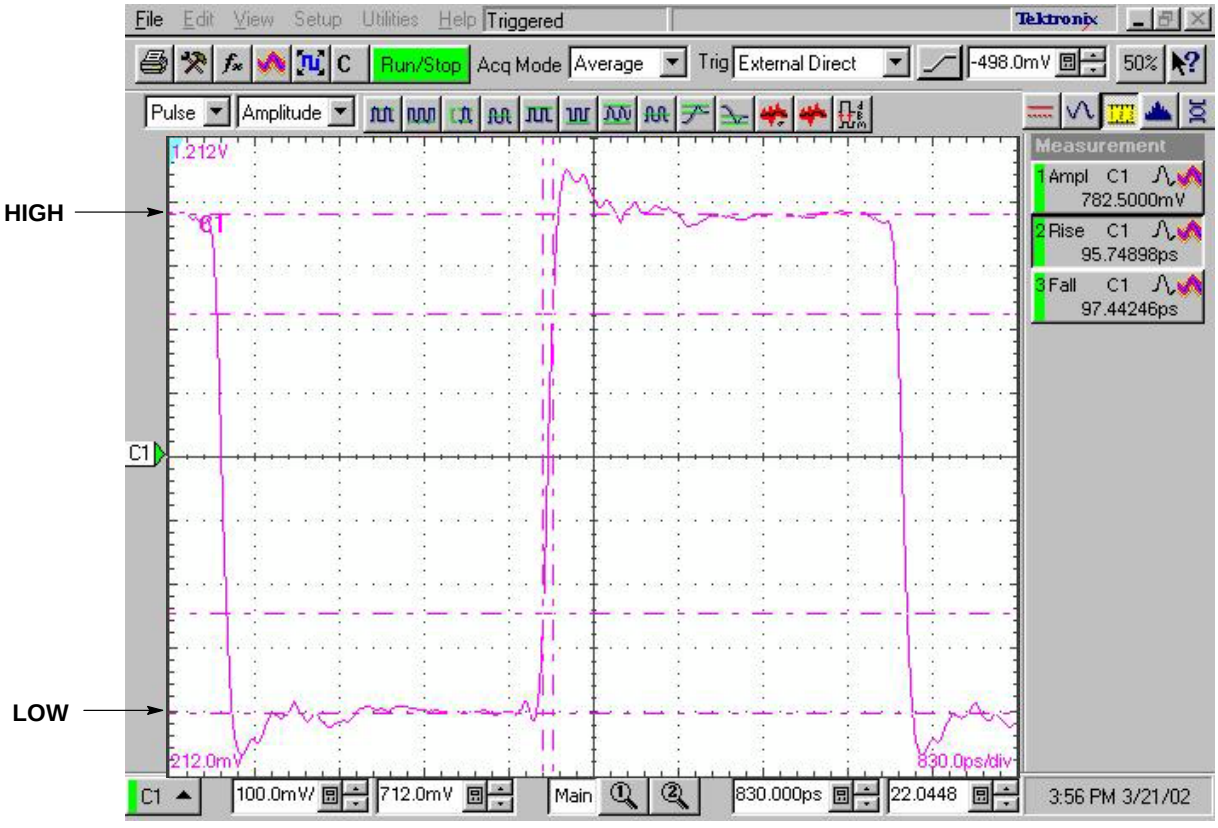


Figure 7. HIGH and LOW Waveform Levels

Output Swing − The output swing (V_{OUTpp}) is measured between the HIGH and LOW levels of each individual differential or single−ended output. The output voltage swing for each individual output is defined by the following equation and Figure 8.

$$V_{OUTPP} = V_{OH} - V_{OL}$$

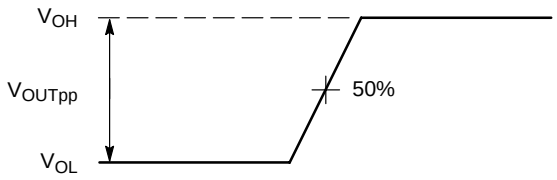


Figure 8. Output Voltage Swing

The V_{OUTpp} value is shown as the vertical axis in the data sheet maximum frequency plots (refer to the "Maximum Input Frequency" section).

SIGNAL TIMING

Duty Cycle − The duty cycle is the ratio of the HIGH pulse width (PW) to the signal period and is described by the following equations:

Signal Period = Time between adjacent rising edges

Duty Cycle = (HIGH Pulse Width/Signal Period) * 100%

The 50% points are used to measure the HIGH pulse width and the signal period. AC characteristics for ON Semiconductor devices are typically measured for a 50% duty cycle input. A 50% duty cycle input/output is shown in Figure 9. Note that the HIGH and LOW pulse widths (PW_H and PW_L respectively) are equal for a 50% duty cycle signal.

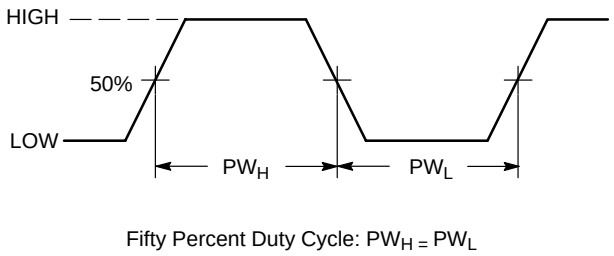


Figure 9. Input/Output Duty Cycle

Maximum Input Frequency − This is a typical device performance value. It is the highest allowable input frequency for proper device operation (f_{MAX}). For shift registers, it is referred to as the Maximum Shift Frequency (f_{SHIFT}). It is the frequency where the output voltage swing (V_{OUTpp}) is equal to a minimum value that is determined by the device type, or it is the frequency where the device no longer functions properly.

An output voltage swing versus input frequency plot is typically included with data sheets. For the MC100EP90 example shown in Figure 10, the maximum listed input frequency of 3.0 GHz occurs at an output voltage swing of approximately 400 mV. The jitter shown in Figure 10 is described in a later section.

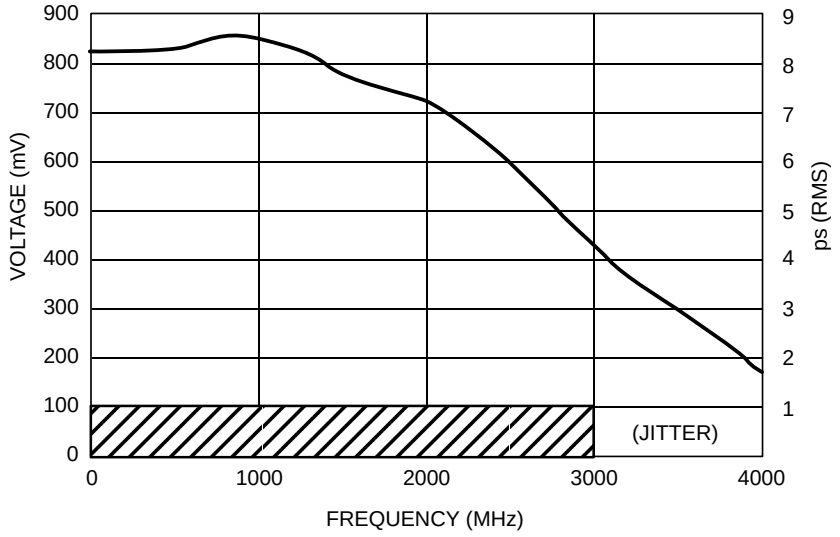


Figure 10. Output Voltage vs. Input Frequency Example

DIFFERENTIAL CHARACTERISTICS

Section Note − This section explains concepts that only apply for differential inputs and/or outputs. Differential inputs and outputs have true and inverted pins, and are often referred to as “complimentary” inputs and outputs. An example of a differential input is a true data input (D), and an inverted data input ($\overline{D}$).

Differential Input Application – True and inverted input signals must be applied in order to obtain accurate differential test measurements for differential input devices. The true output of the pulse generator is connected to the true input of the DUT, and the inverted output of the pulse generator is connected to the inverted input of the DUT.

Unused Output Termination – An unused output of a differential pair must be terminated in the same manner as the used output in order to obtain accurate measurements.

Differential Crosspoint – Differential crosspoints are used as a measurement point for differential input and differential output signals. A differential crosspoint (X_{pt}) is located where the true and inverted inputs or outputs intersect as shown in Figure 11.

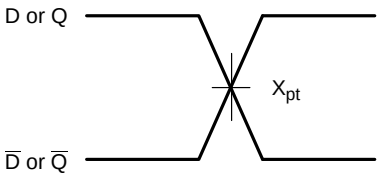


Figure 11. Differential Input/Output Crosspoint

Input Voltage Swing – The minimum input voltage swing (V_{PPmin}) is found by decreasing the swing between the true and inverted inputs until the device no longer performs its specified function. The maximum input voltage swing (V_{PPmax}) is determined by the internal circuitry of a specific device. The differential input voltage swing is defined by the following equations and Figure 12.

$$V_{PP} = | V_{IN(true)} - V_{IN(inverted)} |$$

$$V_{PP(min)} \le V_{PP} \le V_{PP(max)}$$

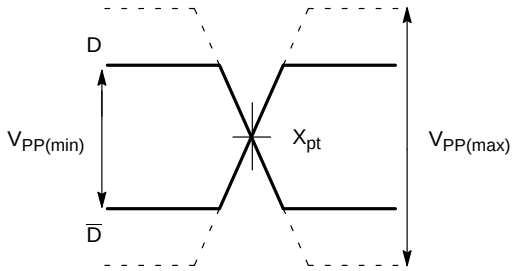


Figure 12. Differential Input Voltage Swing

Test Input Swing – The typical AC test input swing for differential inputs is shown below:

$$V_{PP\,(AC\ Test)} = |V_{IN\,(true)} - V_{IN\,(inverted)}| = 750\ mV$$

Common Mode Range – The most positive of the true and inverted input voltages (i.e., the HIGH level) must be within the differential HIGH input common mode range (V_{IHCMR}) for proper operation. To restate, the common mode range places an upper and lower boundary on the differential HIGH input level. The HIGH input common mode range is specified in relation to the input voltage swing (V_{PP}). The relationship is determined by the device type, so refer to the device data sheet for specific information. The differential HIGH input common mode range is defined by the following equations.

$$V_{IHCMR(min)} \le V_{IH} \le V_{IHCMR(max)}$$

$V_{IHCMR(max)}$ varies 1 : 1 with V_{CC}

$V_{IHCMR(min)}$ varies 1 : 1 with V_{EE}

The example shown in Figure 13 is typical, and specifies the common mode range with respect to the entire V_{PP} range.

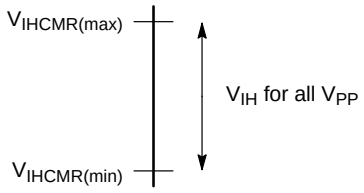


Figure 13. Common Mode Range

The MC100LVEL14 example shown in Figure 14 specifies the common mode range with respect to two V_{PP} ranges.

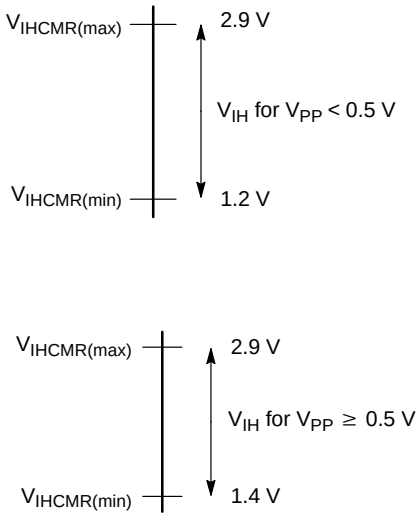


Figure 14. MC100LVEL14 Common Mode Range

Differential Input Example – The relationship between V_{PP} and V_{IHCMR} is used to completely define valid differential input signals. The following MC100EP116 example is for the 5.0 V PECL mode (V_{CC} = 5.0 V, V_{EE} = GND), and illustrates the valid input voltages for an application which uses the minimum and maximum input voltage swings for the device. Note that both the V_{PP} and the V_{IHCMR} conditions are satisfied for each of the two waveforms.

$$V_{IHCMR(min)} = 2.0\ V \le V_{IH} \le V_{IHCMR(max)} = 5.0\ V$$

$$V_{PP(min)} = 150\ mV \le V_{PP} \le V_{PP(max)} = 1200\ mV$$

The top waveform in Figure 15 represents the highest possible LOW input value where:

$$V_{IL(max)} = V_{IH(max)} - V_{PP(min)} = 5.0 - 0.15 = 4.85\ V$$

The bottom waveform in Figure 15 represents the lowest possible LOW input value where:

$$V_{IL(min)} = V_{IH(min)} - V_{PP(max)} = 2.0 - 1.2 = 0.80\ V$$

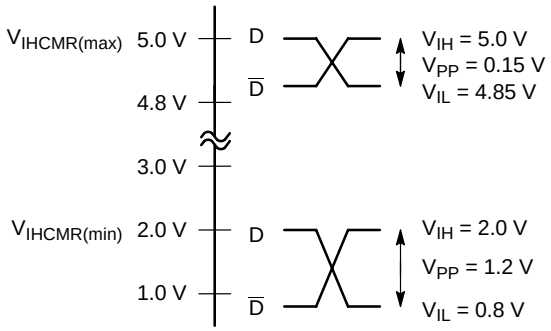


Figure 15. MC100EP116 Differential Input Voltage

SINGLE−ENDED CHARACTERISTICS

Section Note – This section explains concepts that only apply to single−ended inputs and/or outputs.

Single−Ended Inputs – Many inputs/outputs are single−ended instead of differential, i.e. they have a single input/output instead of a pair of true and inverted inputs/outputs.

Single−Ended 50% Points – Single−ended 50% points are used as a measurement point for single−ended input and output signals. A 50% point is the single−ended signal level which lies halfway between the HIGH and LOW input/output levels as shown in Figure 16.

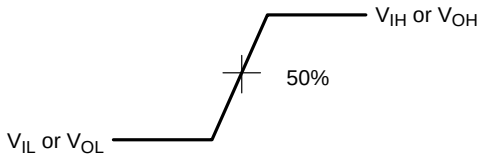


Figure 16. Single−Ended Input/Output 50% Point

Note from the following MC100EP116 calculations for the 5.0 V PECL mode that the 50% point voltage is not a fixed voltage. The 50% point varies with the input voltage range.

$$50\%\ Point_{(max)} = [V_{IH(max)} + V_{IL(max)}]/2 = (4120 + 3375)/2 = 3748\ mV$$

$$50\%\ Point_{(min)} = [V_{IH(min)} + V_{IL(min)}]/2 = (3775 + 3190)/2 = 3483\ mV$$

Single−Ended Input Voltage Range – Single−ended input HIGH and LOW levels have a boundary and a threshold as shown in Figure 17. Once an input crosses a logic threshold, the logic state is guaranteed to change to the new state.

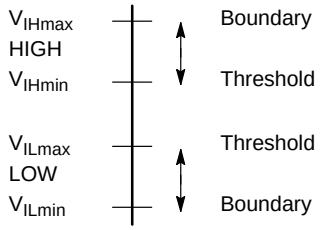


Figure 17. Single−Ended Input Logic Levels

The MC100EP116 example shown in Figure 18 is for the 5.0 V PECL mode.

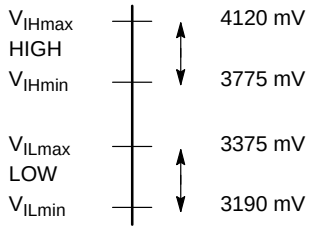


Figure 18. MC100EP116 Single−Ended Input Example

Single−Ended Input Test Level – The AC test single−ended input swing is typically given by the following equation:

$$V_{IN(swing)} = |V_{IH} - V_{IL}| = 750\ mV$$

Differential Inputs (Single−Ended Mode) – Either input of a differential pair may be used individually if the unused input of the differential pair is connected to V_{BB} (the switching reference voltage). The switching reference voltage is provided by many differential devices. Figure 19 illustrates the use of the true input as the single−ended input. Note that the unused inverted output is terminated in the same fashion as the true output.

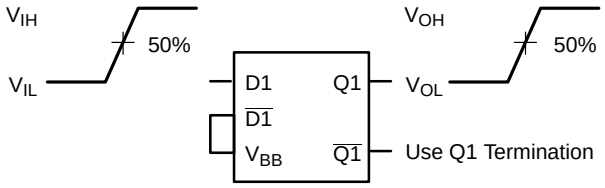


Figure 19. Differential Input in Single−Ended Mode

The switching reference voltage provides a switching point that is approximately halfway between the HIGH and LOW levels. As an example, the MC100EP116 data sheet specifies the following switching reference voltage range for the 5.0 V PECL mode. The MC100EP116 50% point range previously calculated is listed below the V_{BB} range.

$$3475\ mV \le V_{BB} \le 3675\ mV$$

$$3483\ mV \le 50\%\ Point \le 3748\ mV$$

Note that the V_{BB} range is very close to the 50% point range. This is true because the switching reference voltage provides a switching point for a differential input in single−ended mode that is analogous to the 50% point range for normal single−ended inputs.

TIMING CHARACTERISTICS

Output Rise and Fall Times

ECL Output Devices – The output rise time for ECL devices is the time required to rise from the 20% level to the 80% level of the output rising edge. The output fall time for ECL devices is the time required to fall from the 80% level to the 20% level of the output falling edge. The output rise and fall times for devices with ECL outputs is shown in Figure 20.

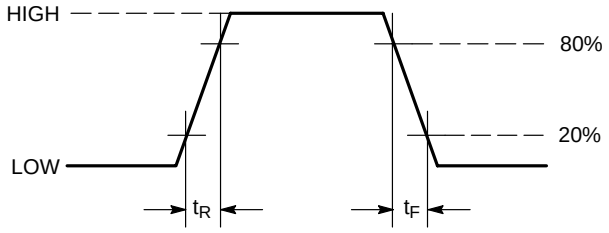


Figure 20. ECL Output Rise and Fall Times

Non−ECL Output Devices – Refer to the translator data sheets as different conditions are used to specify the output rise and fall times. One type of condition specifies output rise and fall times between the 10% and 90% output levels. For example, the rise and fall times for the MC100ELT21 PECL to TTL translator are specified between the 10% and 90% output levels as shown in Figure 21.

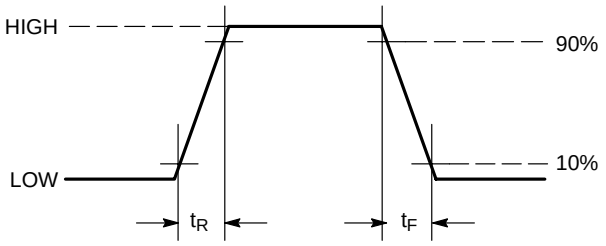


Figure 21. TTL Output Rise and Fall Time Percentages

Another type of test condition specifies non−ECL output rise and fall times between fixed output voltage levels. For example, the rise and fall times for the MC100EPT21 LVPECL to LVTTL translator are specified between fixed output voltages of 0.8 V and 2.0 V as shown in Figure 22.

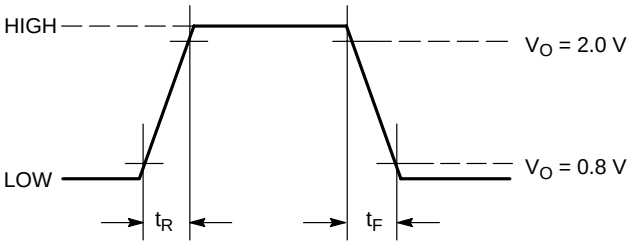


Figure 22. LVTTL Output Rise and Fall Time Levels

Propagation Delay

Rising Edge Propagation – The rising edge (LOW−to−HIGH transition) propagation delay (t_{PLH} or t_{P++}) is the time needed to propagate an input rising edge to the output.

Falling Edge Propagation – The falling edge (HIGH−to−LOW transition) propagation delay (t_{PHL} or t_{P--}) is the time needed to propagate an input falling edge to the output.

Single−Ended ECL Devices– Single−ended propagation delay is measured between the 50% point of the input rising or falling edge, and the 50% point of the identical output edge. There are many types of single−ended propagation delays such as a clock input to data output (CLK to Q) propagation delay. Single−ended output propagation delay is shown in Figure 23.

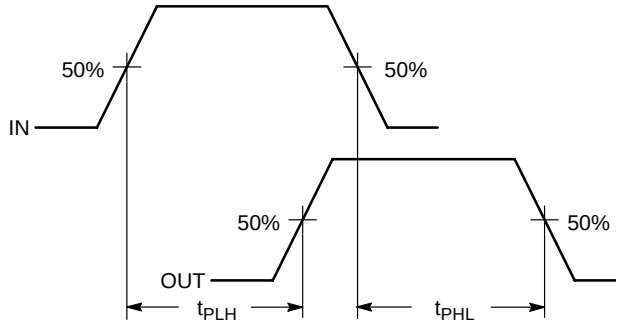


Figure 23. Single−Ended Propagation Delay

Differential ECL Devices – Differential propagation delay is measured between the crosspoint of the input rising or falling edge, and the crosspoint of the identical output edge. There are many types of differential input/output pairs such as inverted clock inputs to inverted data outputs ($\overline{CLK}$ to $\overline{Q}$). Differential output propagation delay is shown in Figure 24.

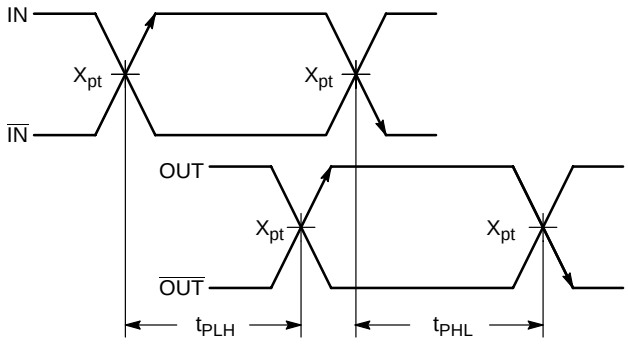


Figure 24. Differential Propagation Delay

ECL Inputs and Non−ECL Outputs – Refer to the device data sheet as several methods are used to measure the output propagation delays. One method specifies the output propagation delays from an ECL input crosspoint to a non−ECL fixed output voltage. For example, the output propagation delays for the MC100ELT21 PECL to TTL translator are specified between the ECL input crosspoint and a TTL output fixed voltage equal to 1.5 V as shown in Figure 25.

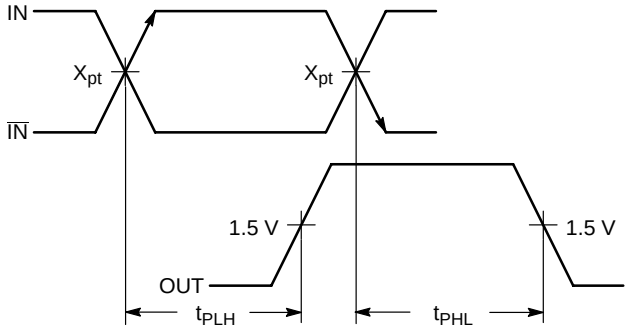


Figure 25. TTL Output Propagation Delay

Non−ECL Input and ECL Outputs – Refer to the device data sheet as several methods are used to measure the output propagation delays. One method specifies the output propagation delays from a non−ECL input fixed voltage to an ECL output 50% point. For example, the output propagation delays for the MC10H352 CMOS to PECL translator are specified between a CMOS input fixed voltage equal to $V_{CC}/2$ and the ECL output 50% point as shown in Figure 26.

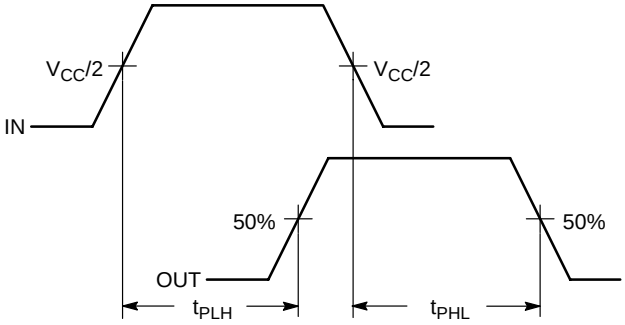


Figure 26. CMOS Input Propagation Delay

Skew (Duty Cycle)

Duty cycle skew is also referred to as pulse skew. Duty cycle skew is mathematically calculated by taking the difference between the rising and falling edge propagation delays. Unequal t_{PLH} and t_{PHL} values cause pulse width distortion which affects the duty cycle. Duty cycle skew is defined by the following equation and Figures 27 and 28 for an input and its associated output.

$$t_{SKEW}(\text{Duty Cycle}) = |t_{PLH} - t_{PHL}|$$

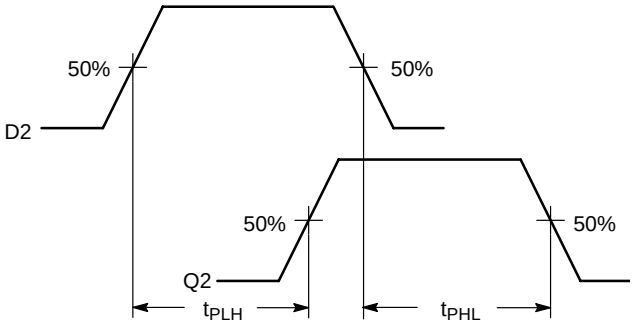


Figure 27. Single−Ended Duty Cycle Skew

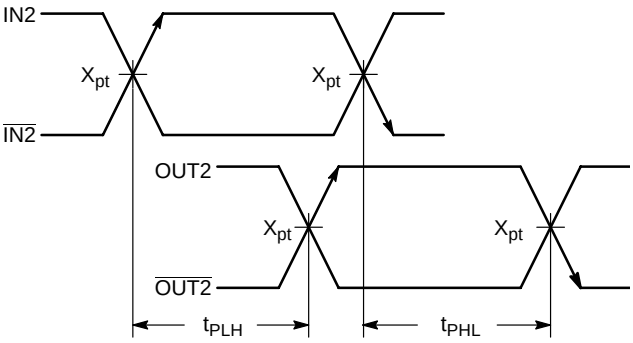


Figure 28. Differential Duty Cycle Skew

Skew (Within Device)

Within device skew is the difference between the identical transition propagation delays of a single multiple output device with a common input. It is mathematically calculated by obtaining the rising and falling output propagation delays for each individual output of the device. The minimum output propagation delay from the set of delays is then subtracted from the maximum output propagation delay from the set of delays as shown in the following equations. The higher of the two equation results is taken as the within device skew specification.

$$t_{SKEW}\ (\text{Within Device Rising Edge}) = t_{PLH}(\text{max from set}) - t_{PLH}(\text{min from set})$$

$$t_{SKEW}\ (\text{Within Device Falling Edge}) = t_{PHL}(\text{max from set}) - t_{PHL}(\text{min from set})$$

The example shown in Figure 29 defines the within device skew parameters for a device with two inputs (D1, D2) and their two associated outputs (Q1, Q2). The within device skew for this example would be the higher of the following two equation results:

$$t_{SKEW}(\text{Within Device}) = t_{PLH2} - t_{PLH1}$$

$$t_{SKEW}(\text{Within Device}) = t_{PHL2} - t_{PHL1}$$

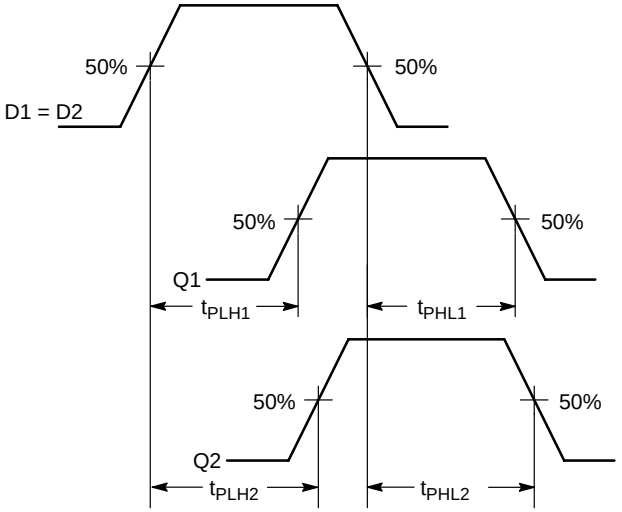


Figure 29. Within Device Skew

Skew (Device to Device)

Device to device skew is the difference between the identical transition propagation delays of two devices with a common input signal under identical operating conditions (identical ambient temperature, V_{CC}, V_{EE}, etc). It is mathematically calculated from data sheet propagation delay values as shown below.

$$t_{SKEW}\ (\text{Device to Device}) = t_{PLH(max)} - t_{PLH(min)} = t_{PHL(max)} - t_{PHL(min)}$$

Minimum Input Pulse Width

The minimum input pulse width (t_{PW}) is the shortest pulse width that will guarantee proper device operation. It is measured by decreasing the test signal generator pulse width (i.e., DUT input pulse width) until the DUT outputs no longer function properly. For single−ended inputs, it is measured between the 50% points of the rise and fall transitions as shown in Figure 30.

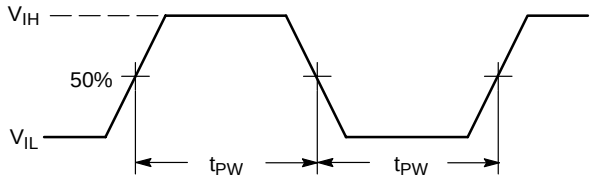


Figure 30. Single−Ended Input Pulse Width

For differential inputs, it is measured between the crosspoints of the rise and fall transitions as shown in Figure 31.

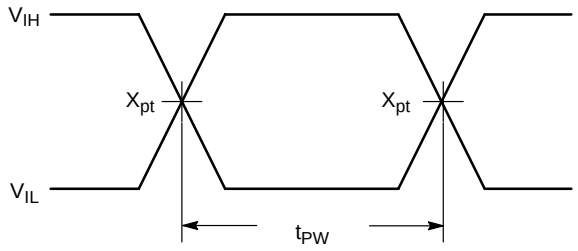


Figure 31. Differential Input Pulse Width

Setup and Hold Time

Applicability – Only synchronous clocked devices have setup (t_S or t_{SETUP}) and hold (t_H or t_{HOLD}) times.

Timing Window – The minimum setup requirement and the minimum hold requirement specify the timing window where the input must not change in order to successfully clock the input. The setup time specifies the left edge of the timing window, and the hold time specifies the right edge of the window. Both timing requirements must be met in order to successfully clock the input.

Measurement Points – Differential crosspoints (refer to the "Differential Characteristics" section) and single−end 50% points (refer to the "Single−Ended Characteristics" section) are used as time measurement points. Note from the following figures that the 50% point of the active clock edge is the time origin of all setup and hold time measurements.

Minimum Setup Time – The following is true of minimum setup times.

- Minimum setup times are usually positive, and they specify the minimum length of time that the input must remain unchanged before the active clock edge in order to successfully clock the input. Positive setup times therefore indicate that the left edge of the timing window is before the active clock edge.
- Negative minimum setup times specify the minimum length of time that the input must remain unchanged after the active clock edge in order to successfully clock the input. Negative setup times therefore indicate that the left edge of the timing window is after the active clock edge.

Minimum Hold Time – The following is true of minimum setup times.

- Minimum hold times are usually positive, and they specify the minimum length of time that the input must remain unchanged after the active clock edge in order to successfully clock the input. Positive hold times therefore indicate that the right edge of the timing window is after the active clock edge.
- Negative hold times specify the minimum length of time that the input must remain unchanged before the active clock edge in order to successfully clock the input. Negative hold times therefore indicate that the right edge of the timing window is before the active clock edge.

Typical Setup and Hold Times – The typical setup and hold times specified on data sheets are not guaranteed, and they are only included for failure analysis calculations. They are measured by independently moving the left and right edges of the timing window about the active clock edge until the outputs no longer function properly.

Positive Setup and Positive Hold Example – The MC100EP29 data sheet specifies the following:

- The minimum setup time of positive 100 ps indicates that the left edge of the timing window is 100 ps before the active rising clock edge.
- The minimum hold time of positive 100 ps specifies that the right edge of the timing window is 100 ps after the active rising clock edge.

The setup time requirement and the hold time requirement were both met in the example shown in Figure 32, therefore the LOW−to−HIGH output transition occurs after the CLK rising edge propagation delay of 420 ps. Note that the input cannot change within the timing window of 200 ps. Only one side of the differential clocks, inputs, and outputs are shown in Figure 32.

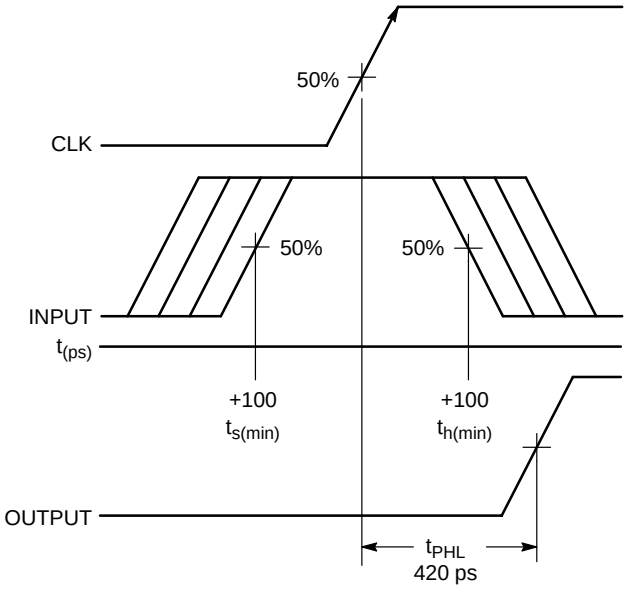


Figure 32. Positive Setup and Positive Hold Example

Negative Setup and Positive Hold Example – The MC100E445 4−Bit Serial/Parallel Converter data sheet specifies the following:

- The minimum setup time of negative 200 ps indicates that the left edge of the timing window is 200 ps after the active rising clock edge.
- The minimum hold time of positive 300 ps specifies that the right edge of the timing window is 300 ps after the active rising clock edge.

The setup time requirement and the hold time requirement were both met in the example shown in Figure 33, therefore the LOW−to−HIGH output transition occurs after the CLK rising edge propagation delay of 1800 ps. Note that the input cannot change within the timing window of 100 ps. Only one of the differential clocks and differential inputs is shown in Figure 33.

Positive Setup and Negative Hold Example – The MC100E136 6−Bit Universal Up/Down Counter data sheet specifies the following:

- The minimum setup time of positive 400 ps indicates that the left edge of the timing window is 400 ps before the active rising clock edge.
- The minimum hold time of negative 250 ps specifies that the right edge of the timing window is 250 ps before the active rising clock edge.

The setup time requirement and the hold time requirement were both met in the example shown in Figure 34, therefore the LOW−to−HIGH output transition occurs after the CLK rising edge propagation delay of 1150 ps. Note that the input cannot change within the timing window of 150 ps.

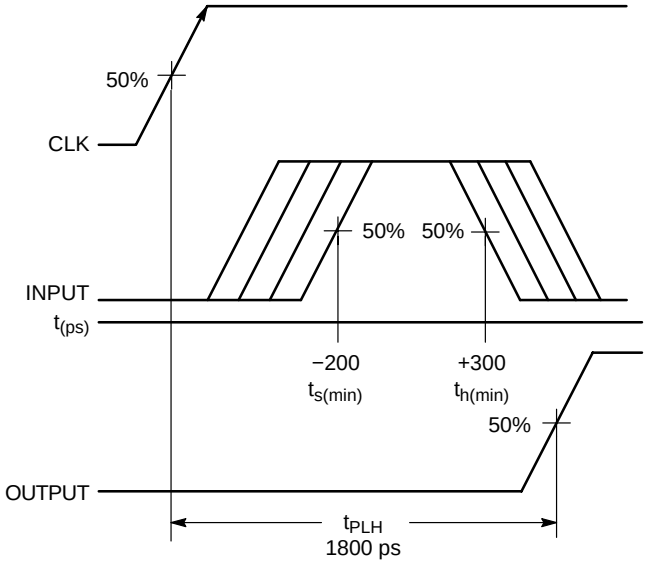


Figure 33. Negative Setup and Positive Hold Example

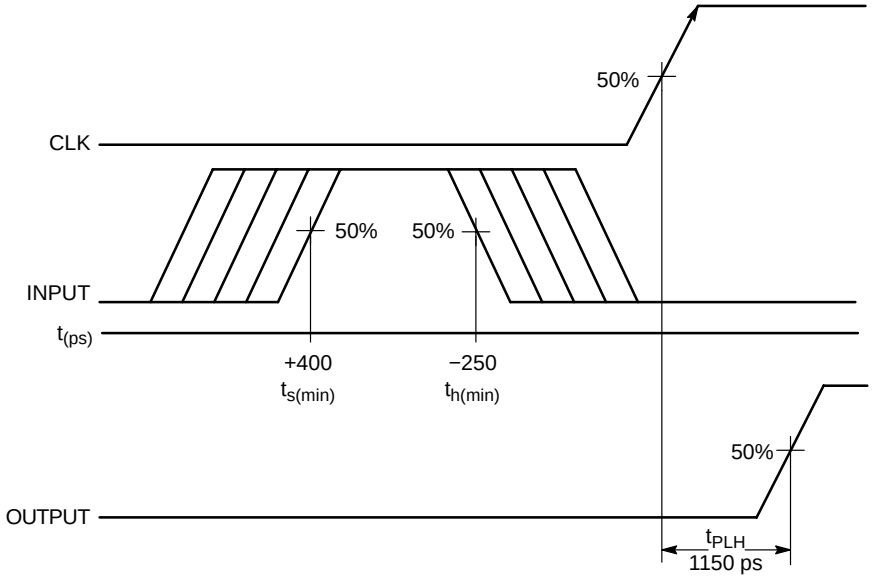


Figure 34. Positive Setup and Negative Hold Example

Negative Setup and Negative Hold Comment – The left edge of the timing window is the setup edge, and the right edge of the window is the hold edge. A negative setup time with a negative hold time cannot occur as this principle would be violated (i.e., the hold edge would occur before the set edge).

Set and Reset Recovery Time

Applicability – Only devices with a Set input have set recovery times (t_{SR}), and only devices with a Reset input have reset recovery times (t_{RR}).

Measurement Points – Differential crosspoints (refer to the "Differential Characteristics" section) and single−end 50% points (refer to the "Single−Ended Characteristics" section) are used as time measurement points. Note from the following figures that the 50% point of the active clock edge is the time origin of all set and reset recovery time measurements.

Minimum Set Recovery Time – This parameter defines the minimum length of time that Set has to be inactive before an active clock edge in order for the output to enter the non−Set state. In the non−Set state, the output is no longer dependent upon the Set state.

In the MC100EP29 example shown in Figure 35, the minimum set recovery time of 150 ps specifies that the system must be designed so that Set transitions from the active HIGH state to the inactive LOW state at least 150 ps before the active rising clock edge. The set recovery timing requirement (150 ps) and the input setup time requirement (100 ps) were both met in the example shown in Figure 35, therefore the output transitions from the Set state (HIGH) to the input state (LOW). The transition takes place after the specified 420 ps HIGH−to−LOW CLK propagation delay.

Minimum Reset Recovery Time – This parameter defines the minimum length of time that Reset has to be inactive before an active clock edge in order for the output to enter the non−Reset state. In the non−Reset state, the output is no longer dependent upon the Reset state.

In the MC100EP29 example shown in Figure 36, the minimum reset recovery time of 150 ps specifies that the system must be designed so that Reset transitions from the active HIGH state to the inactive LOW state at least 150 ps before the active rising clock edge. The reset recovery timing requirement (150 ps) and the input setup time requirement (100 ps) were both met in the example shown in Figure 36, therefore the output transitions from the Set state (HIGH) to the input state (LOW). The transition takes place after the specified 420 ps HIGH−to−LOW CLK propagation delay.

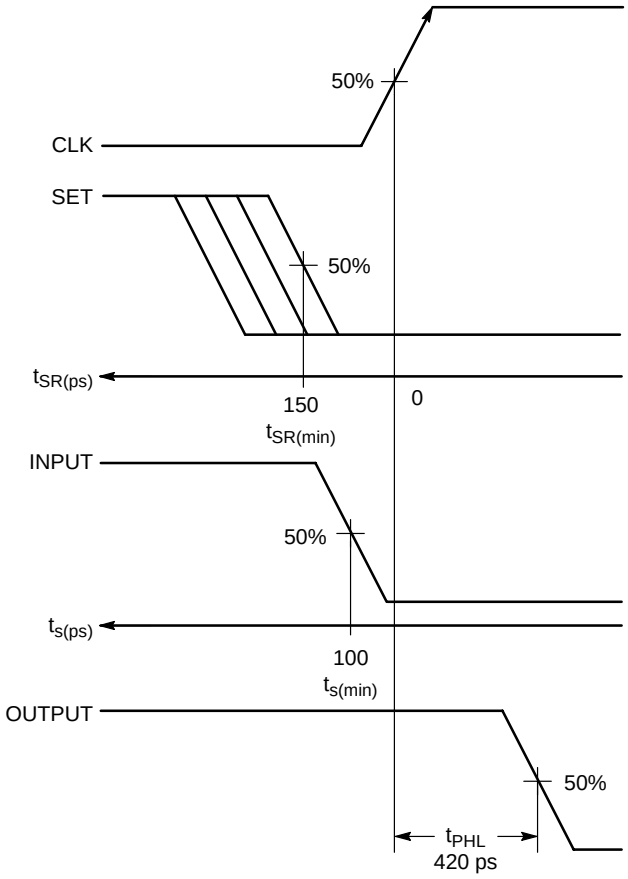


Figure 35. Set Recovery Time Example

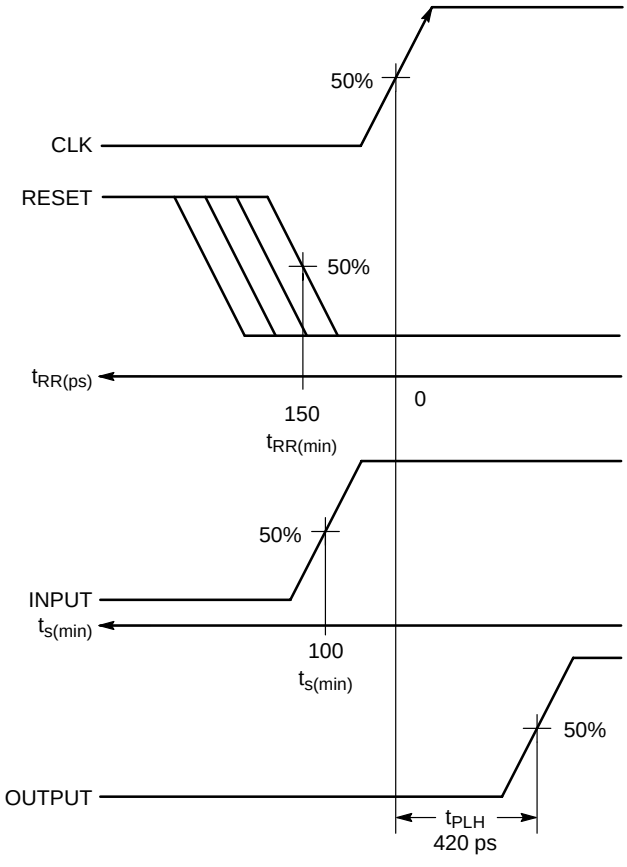


Figure 36. Reset Recovery Time Example

Typical Set and Reset Recovery Times – The typical set and reset recovery times specified on data sheets are not guaranteed, and they are only included for failure analysis calculations. They are measured by moving the active−to−inactive Set and Reset transitions towards the active clock edge until the outputs no longer enter the respective non−Set or non−Reset state.

JITTER

Jitter Definition

Jitter is defined as the deviation of an actual edge location from its ideal location. The possibility of a data transmission error increases as jitter increases. Total jitter consists of “Random Jitter” and “Deterministic Jitter” as described in the following sections.

Random Clock Jitter

Random jitter (RJ, also referred to as “non−systematic” jitter) is characterized by an unbounded Gaussian probability density function as shown in Figure 37. Random jitter is specified on data sheets as Cycle−to−Cycle Jitter, and is specified as an RMS value (the one sigma value). The function is described below, followed by a description of the Cycle−to−Cycle Jitter specification.

The center of the symmetrical probability distribution is the mean and represents an ideal edge location. The area under the distribution represents the probability that an actual edge location will lie within the range surrounding the ideal edge location. For instance, note from Figure 37 that a distribution range of plus/minus one sigma from the mean includes 68.27% of the total distribution area. This means that there is a 68.27% probability that the actual edge location will be within the plus/minus one sigma window.

RJ Confidence Levels

As sigma increases, the confidence that the actual edge location will lie within the distribution range surrounding the ideal edge location increases. This is why the sigma level is commonly referred to as the “Confidence Level.” Confidence levels per sigma are specified in Table 2 where “Sigma” represents the distribution range for one side of the mean, and “Total Sigma” represents the distribution range for both sides of the mean.

Table 2. Confidence Level per Sigma

Sigma	Total Sigma	Confidence Level
plus/minus 1	2	68.27%
plus/minus 2	4	95.45%
plus/minus 3	6	99.73%
plus/minus 4	8	99.99%

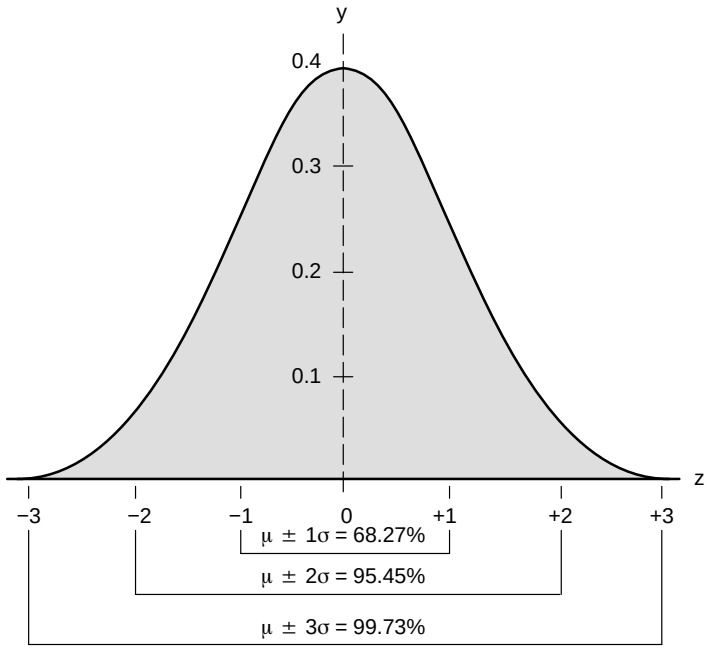
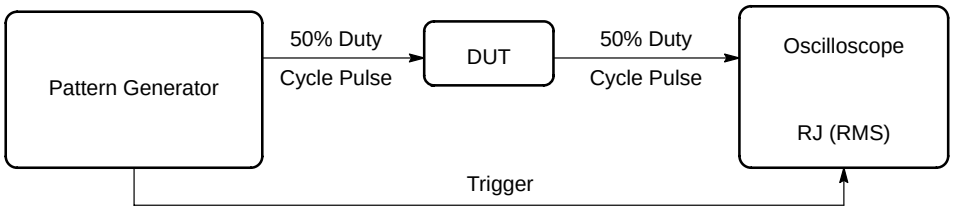


Figure 37. Gaussian Random Clock Jitter Distribution

As an example, the NBSG14 data sheet specifies the typical Cycle−to−Cycle Jitter as 0.5 ps RMS which is the one sigma value.

Total RJ Test Setup

The test setup shown in Figure 38 is used to sample edge locations over a large number of periods, and then measure the total RMS random jitter.

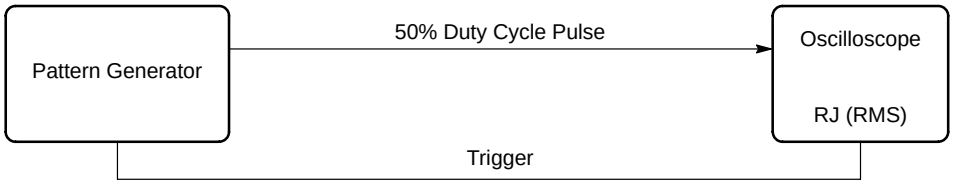


$$\text{Total Jitter (RJ)} = \sqrt{[\text{Pattern Generator (RJ)}]^2 + [\text{DUT (RJ)}]^2 + [\text{Oscilloscope (RJ)}]^2}$$

Figure 38. Total Random Jitter Test

Test Equipment RJ Test Setup

The test setup shown in Figure 39 is used to measure the test equipment RMS random jitter.



$$\text{Test Equipment Jitter (RJ)} = \sqrt{[\text{Pattern Generator (RJ)}]^2 + [\text{Oscilloscope (RJ)}]^2}$$

Figure 39. Test Equipment Random Jitter Test

DUT RJ Calculation

The DUT RMS random clock jitter determined with the following equation is specified as Cycle−to−Cycle Jitter.

$$\text{DUT (RJ)} = \sqrt{[\text{Total Jitter (RJ)}]^2 - [\text{Test Equipment Jitter (RJ)}]^2}$$

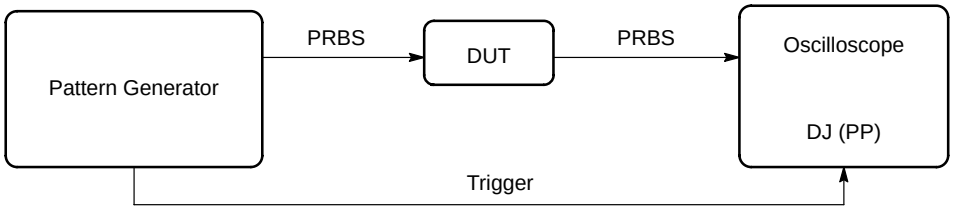
Deterministic Jitter

Deterministic jitter (DJ, also referred to as “data” or “systematic” jitter) is characterized by bounded non–Gaussian probability density functions. Deterministic jitter includes Duty Cycle Distortion (DCD) which is specified as Duty Cycle Skew or Pulse Skew on data sheets (refer to the “Duty Cycle Skew” section). Determistic jitter is defined for a specific test pattern, and is specified as a peak−to−peak value.

Total DJ Test Setup

The total DJ test setup shown in Figure 40 is used to produce an eye diagram. An eye diagram is useful as it provides a qualitative view of peak−to−peak deterministic jitter. To form an eye diagram, a PRBS (Pseudo−Random Bit Sequence) signal is sent to the DUT input, and the DUT output (the eye diagram) is observed on the oscilloscope.

The NBSG14 eye diagram in Figure 41 was created by an Advantest D3186 generating a $2^{31}-1$ PRBS data pattern at 10.8 Gbps. The Tektronix TDS8000 oscilloscope with an 80E01 50 GHz sampling module acquired 7000 samples. The total deterministic jitter represented by the histogram at the top left of the eye diagram is 18.00 ps peak−to−peak. As deterministic jitter increases, the eye closes (i.e., the eye width decreases) which increases the probability of a data transmission error.



Total Jitter(DJ) = Pattern Generator (DJ) + DUT (DJ) + Oscilloscope (DJ)

Figure 40. Total Deterministic Jitter Test

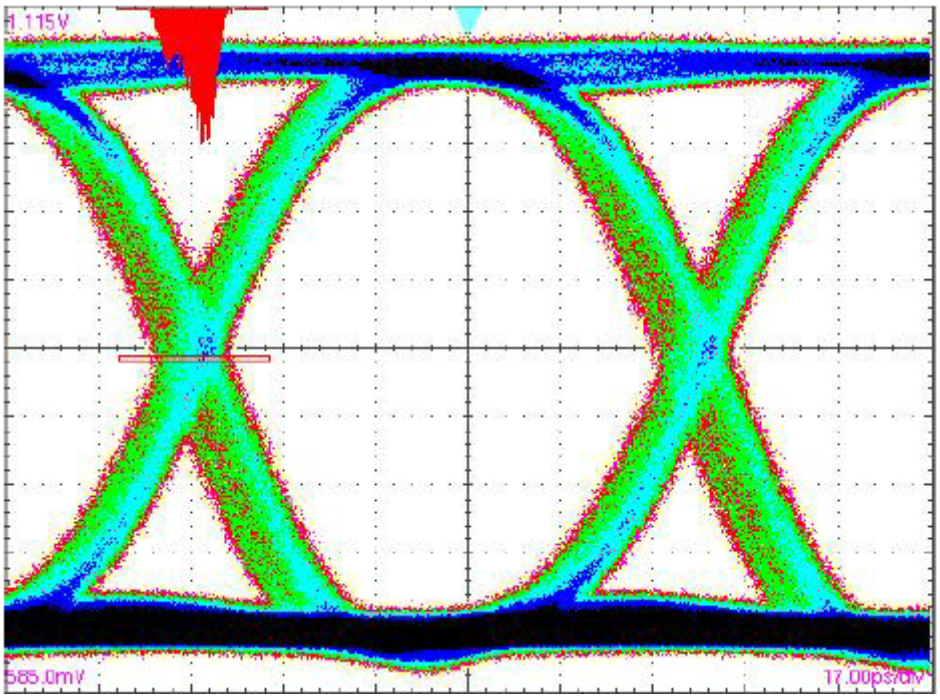
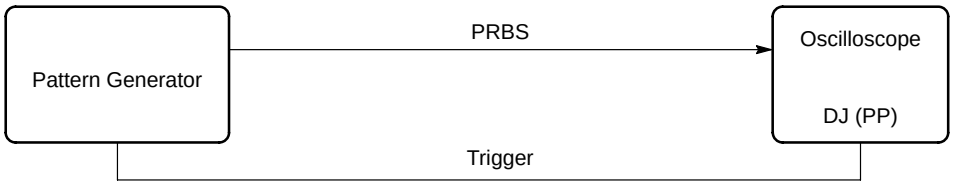


Figure 41. Total Deterministic Jitter Eye Diagram

Test Equipment DJ Test Setup

The general test setup shown in Figure 42 is used to measure the test equipment peak−to−peak deterministic jitter.

The NBSG14 test equipment deterministic jitter eye diagram in Figure 43 was created by the identical pattern generator and oscilloscope setup that was used to generate the total deterministic jitter eye diagram. The test equipment deterministic jitter represented by the histogram at the upper right of the eye diagram is 10.88 ps pp.



Test Equipment Jitter (DJ) = Pattern Generator (DJ) + Oscilloscope (DJ)

Figure 42. Test Equipment Deterministic Jitter Test

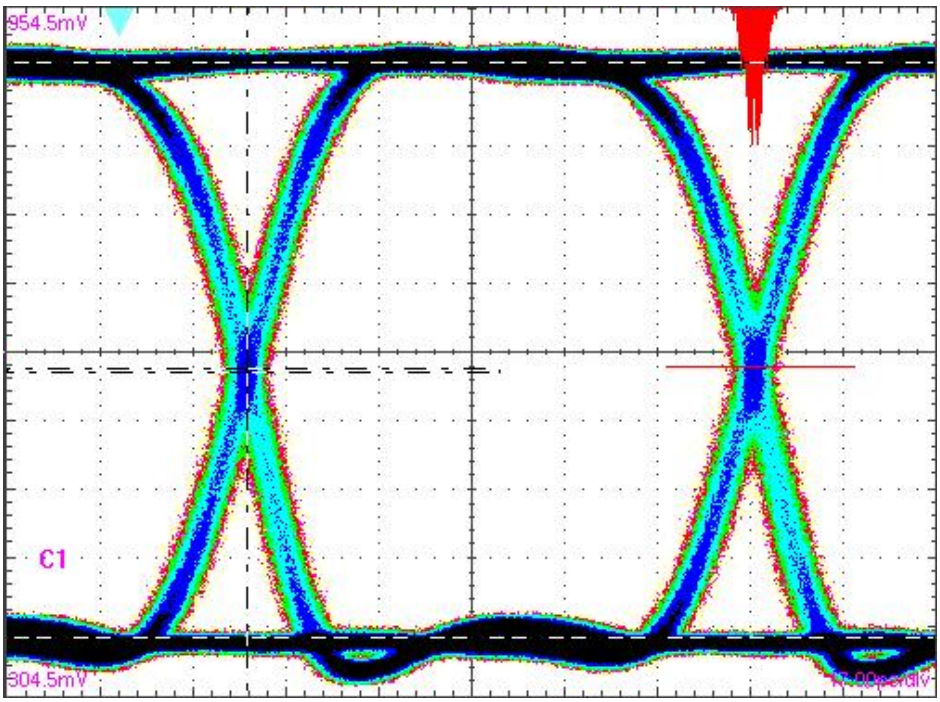


Figure 43. Test Equipment Deterministic Jitter Eye Diagram

DUT DJ Calculation

The DUT peak−to−peak deterministic jitter is determined with the following equation.

DUT (DJ) = Total Jitter (DJ) − Test Equipment Jitter (DJ)

The DUT peak−to−peak deterministic jitter for the above NBSG14 example is calculated below.

DUT (DJ) = 18.00 ps − 10.88 ps = 7.12 ps pp

Table 3. Symbols and Acronyms

A	Amperes
BER	Bit Error Rate
DUT	Device Under Test
ECL	Emitter Coupled Logic
ECLinPS	Emitter Coupled Logic in PicoSeconds
f_{MAX}	Maximum Toggle Frequency
f_{SHIFT}	Maximum Shift Frequency
Gbps	Gigabits (10^9 bits) per second
GHz	Gigahertz (10^9 Hz)
$Jitter_{PP}$	Peak−to−Peak Jitter
$Jitter_{RMS}$	RMS Jitter
lfpm	Linear Feet Per Minute
LVECLinPS	Low Voltage Emitter Coupled Logic in PicoSeconds
MHz	Megahertz (10^6 Hz)
NBSG	GigaComm Product Prefix
ns	Nanoseconds (10^{-9} sec)
pp	Peak−to−Peak
PRBS	Pseudo−Random Binary Sequence
ps	Picoseconds (10^{-12} sec)
RF	Radio Frequency
SOIC	Small Outline Integrated Circuit
t_f	Fall Time
t_h	Hold Time
t_{JITTER}	Jitter
t_{PHL}	Falling Edge Propagation Delay
t_{PLH}	Rising Edge Propagation Delay
t_{PWmin}	Minimum Input Pulse Width
t_r	Rise Time
t_{RR}	Set and Reset Recovery
t_S	Setup Time
t_{SK++}	Input Rising Edge to Output Rising Edge Skew
t_{SK--}	Input Falling Edge to Output Falling Edge Skew
t_{SKEW}	Skew
V_{BB}	Switching Reference Voltage
V_{CC}	The Most Positive Supply Voltage
V_{CMR}	Common Mode Range
V_{EE}	The Most Negative Supply Voltage
V_{IH}	Input High Voltage Level
V_{IL}	Input Low Voltage Level
V_{IN}	Input Voltage
V_{OH}	Output High Voltage Level
V_{OL}	Output Low Voltage Level
V_{OUT}	Output Voltage
V_{OUTpp}	Output Peak−to−Peak Voltage Swing
V_{PPmin}	(Or $V_{INPPmin}$) Minimum Input Peak−to−Peak Voltage Swing
V_{PPmax}	(Or $V_{INPPmax}$) Maximum Input Peak−to−Peak Voltage Swing
V_{TT}	Termination Voltage Typically Equal to V_{CC} – 2.0 V
X_{pt}	Crosspoint of the True and Inverted Waveforms

REFERENCES

Johnson, Howard and Graham, Martin. *High−Speed Digital Design: A Handbook of Black Magic.* PTR Prentice−Hall. New Jersey, 1993.

INCITS. *Methodologies for Jitter Specificatio*n. T11.2 Project 1230. http://www.t11.org.

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