4-Bit, 4-Port Bus Exchange Switch

The ON Semiconductor 74FST3400 is a 4–bit, 4–port bus exchange switch. The device is CMOS TTL compatible when operating between 4.0 and 5.5 Volts. The device exhibits extremely low R_{ON} and adds nearly zero propagation delay. The device adds no noise or ground bounce to the system.

Features

- $R_{ON} < 4 \Omega$ Typical
- Less Than 0.25 ns-Max Delay Through Switch
- Nearly Zero Standby Current
- No Circuit Bounce
- Control Inputs are TTL/CMOS Compatible
- Pin-For-Pin Compatible With QS3400, FST3400, CBT3400
- All Popular Packages: SOIC-24, TSSOP-24, QSOP-24
- All Devices in Package TSSOP are Inherently Pb-Free*

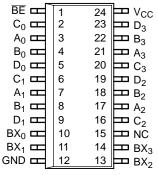
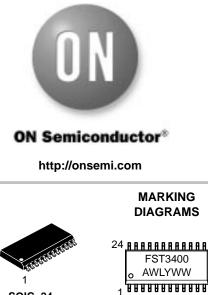


Figure 1. 24–Lead Pinout

TRUTH TABLE

BE	BX ₀	BX ₁	BX ₂	BX3	A0-3	B0–3	Function
н	Х	Х	Х	Х	Hi–Z	Hi–Z	Disconnect
L	BXi = L				C0-3	D0-3	Connect
L	BXi = H			D0-3	C0-3	Exchange	

NOTE: H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care, Hi–Z = High Impedance, i = 0, 1, 2 or 3



SOIC-24 DW SUFFIX CASE 751E



TSSOP-24 DT SUFFIX CASE 948H



Α

= Assembly Location

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24

ARARARARARA

FST 3400

ALYW

1 00000000000000

24 RRRRRRRRRRR

FST3400

AWLYYWW

L, WL = Wafer Lot

Y, YY = Year

W, WW = Work Week

PIN NAMES

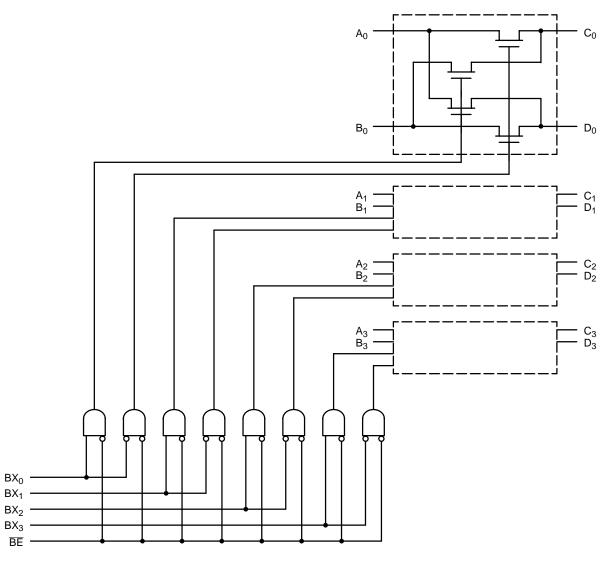
Pin	Description
BE	Bus Enable Input (Active LOW)
Ax, Bx, Cx, Dx	Bus A, Bus B, Bus C, Bus D
$\overline{OE}_1, \overline{OE}_2$	Bus Exchange (Bit 0)
$\overline{OE}_1, \overline{OE}_2$	Bus Exchange (Bit 1)
$\overline{OE}_1, \overline{OE}_2$	Bus Exchange (Bit 2)
$\overline{OE}_1, \overline{OE}_2$	Bus Exchange (Bit 3)
$\overline{OE}_1, \overline{OE}_2$	No Connect
$\overline{OE}_1, \overline{OE}_2$	Ground
$\overline{OE}_1, \overline{OE}_2$	Power

ORDERING INFORMATION See detailed ordering and shipping information in the package

dimensions section on page 2 of this data sheet.

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Semiconductor Components Industries, LLC, 2005





ORDERING INFORMATION

Device Order Number	Package	Shipping [†]
74FST3400DW	SOIC-24	48 Units / Rail
74FST3400DWR2	SOIC-24	2500 Units / Tape & Reel
74FST3400DT	TSSOP-24* (Pb-Free)	96 Units / Rail
74FST3400DTR2	TSSOP-24* (Pb-Free)	2500 Units / Tape & Reel
74FST3400QS	QSOP-24	96 Units / Rail
74FST3400QSR	QSOP-24	2500 Units / Tape & Reel

+For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
 *This package is inherently Pb–Free.

MAXIMUM RATINGS

Symbol	Paran	neter	Value	Unit
V _{CC}	DC Supply Voltage		-0.5 to $+7.0$	V
VI	DC Input Voltage		-0.5 to +7.0	V
Vo	DC Output Voltage		-0.5 to +7.0	V
I _{IK}	DC Input Diode Current	-50	mA	
I _{OK}	DC Output Diode Current	-50	mA	
Ι _Ο	DC Output Sink Current	128	mA	
I _{CC}	DC Supply Current per Supply Pin	±100	mA	
I _{GND}	DC Ground Current per Ground Pin	±100	mA	
T _{STG}	Storage Temperature Range	-65 to +150	°C	
ΤL	Lead Temperature, 1 mm from Case for 10) Seconds	260	°C
TJ	Junction Temperature Under Bias		+ 150	°C
θ_{JA}	Thermal Resistance	SOIC TSSOP QSOP	125 170 200	°C/W
MSL	Moisture Sensitivity		Level 1	
F _R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V–0 @ 0.125 in	
V _{ESD}	ESD Withstand Voltage	Human Body Model (Note 1) Machine Model (Note 2) Charged Device Model (Note 3)	>2000 >200 N/A	V
I _{Latchup}	Latchup Performance Abo	ove V_{CC} and Below GND at 85°C (Note 4)	±500	mA

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Tested to EIA/JESD22-A114-A.

2. Tested to EIA/JESD22-A115-A.

3. Tested to JESD22-C101-A.

4. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Р	Min	Max	Unit	
V _{CC}	Supply Voltage	Operating, Data Retention Only	4.0	5.5	V
VI	Input Voltage	(Note 5)	0	5.5	V
Vo	Output Voltage	(HIGH or LOW State)	0	5.5	V
T _A	Operating Free–Air Temperature		- 40	+ 85	°C
Δt/ΔV	Input Transition Rise or Fall Rate Switch I/O	Switch Control Input V _{CC} = 5.0 V \pm 0.5 V	0	DC 5	ns/V

5. Unused control inputs may not be left open. All control inputs must be tied to a high or low logic input voltage level.

DC ELECTRICAL CHARACTERISTICS

			V _{CC}	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$			
Symbol	Parameter	Conditions	(V)	Min	Тур*	Max	Unit
V _{IK}	Clamp Diode Resistance	$I_{IN} = -18mA$	4.5			- 1.2	V
VIH	High–Level Input Voltage		4.0 to 5.5	2.0			V
V _{IL}	Low-Level Input Voltage		4.0 to 5.5			0.8	V
I _I	Input Leakage Current	$0 \le V_{IN} \le 5.5 V$	5.5			±1.0	μΑ
I _{OZ}	OFF-STATE Leakage Current	$0 \le A, B \le V_{CC}$	5.5			±1.0	μΑ
R _{ON}	Switch On Resistance (Note 6)	$V_{IN} = 0 V$, $I_{IN} = 64 mA$	4.5		4	7	Ω
		V _{IN} = 0 V, I _{IN} = 30 mA	4.5		4	7	
		V _{IN} = 2.4 V, I _{IN} = 15 mA	4.5		8	15	
		V _{IN} = 2.4 V, I _{IN} = 15 mA	4.0		11	20	
I _{CC}	Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0$	5.5			3	μΑ
ΔI_{CC}	Increase In I _{CC} per Input	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5			2.5	mA

*Typical values are at V_{CC} = 5.0 V and T_A = 25°C.
6. Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC ELECTRICAL CHARACTERISTICS

				$\label{eq:T_A} \begin{array}{l} \textbf{T}_{\textbf{A}} = -40^{\circ}\text{C to} + 85^{\circ}\text{C} \\ \textbf{C}_{\textbf{L}} = 50 \text{ pF, RU} = \text{RD} = 500 \ \Omega \end{array}$			
			V _{CC} = 4.5–5.5 V V _{CC} = 4.0 V				
Symbol	Parameter	Conditions	Min	Max	Min	Max	Unit
t _{PHL} ,	Prop Delay Bus to Bus (Note 7)	V _I = OPEN		0.25		0.25	ns
t _{PLH}	Prop Delay, BXn to An, Bn, Cn or Dn		1.0	5.3		6.0	
t _{PZH} ,	Output Enable Time, BXn to An, Bn, Cn or Dn	$V_{I} = 7 V \text{ for } t_{PZL}$	1.0	5.8		6.5	ns
t _{PZL}	Output Enable Time, I _{OE} to An, Bn, Cn or Dn	$V_I = OPEN \text{ for } t_{PZH}$	1.0	5.8		6.5	
t _{PHZ} ,	Output Disable Time, BXn to An, Bn, Cn or Dn	$V_I = 7 V$ for t_{PLZ}	1.0	5.3		6.2	ns
t _{PLZ}	Output Disable Time, I _{OE} to An, Bn, Cn or Dn	$V_I = OPEN$ for t_{PHZ}	1.0	5.3		6.2	

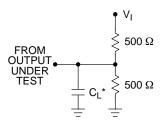
7. This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).

CAPACITANCE (Note 8)

Symbol	Parameter	Conditions	Тур	Max	Unit
C _{IN}	Control Pin Input Capacitance	V _{CC} = 5.0 V	6		pF
C _{I/O}	Port Input/Output Capacitance	$V_{CC}, \overline{OE} = 5.0 V$	13		pF

8. $T_A = +25^{\circ}C$, f = 1 MHz, Capacitance is characterized but not tested.

AC Loading and Waveforms

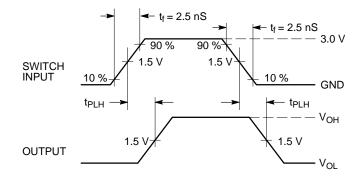


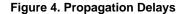
NOTES:

1. Input driven by 50 Ω source terminated in 50 $\Omega.$ 2. CL includes load and stray capacitance.

 $^{*}C_{L} = 50 \text{ pF}$

Figure 3. AC Test Circuit





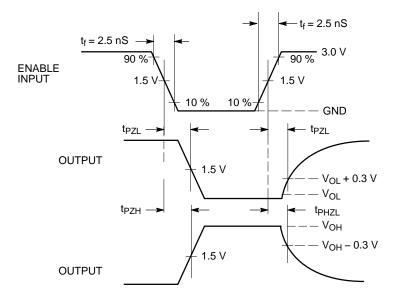
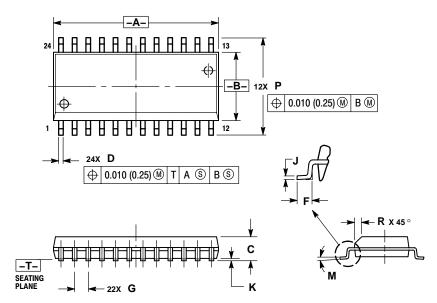


Figure 5. Enable/Disable Delays

PACKAGE DIMENSIONS

SOIC-24 **D SUFFIX** CASE 751E-04 ISSUE E

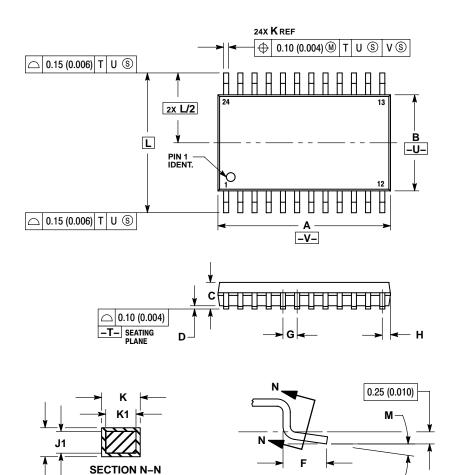


- NOTES: 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: MILLIMETER. 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE. 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	15.25	15.54	0.601	0.612
В	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050	BSC
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
Μ	0 °	8°	0°	8 °
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

PACKAGE DIMENSIONS

TSSOP-24 **DT SUFFIX** CASE 948H-01 **ISSUE A**

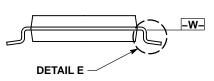


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NOTES:

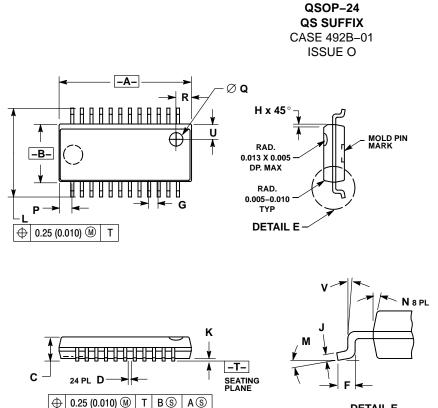
- NOTES:
 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 CONTROLLING DIMENSION: MILLIMETER.
 DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) DED GUE
- OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE. 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE. 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION. 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- REFERENCE ONLY.
 DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	7.70	7.90	0.303	0.311
В	4.30	4.50	0.169	0.177
С		1.20		0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65	BSC	0.026 BSC	
Н	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC			BSC
Μ	0°	8°	0°	8 °



DETAIL E

PACKAGE DIMENSIONS



DETAIL E

NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. CONTROLLING DIMENSION: INCH.
- 2
- THE BOTTOM PACKAGE SHALL BE BIGGER THAN THE TOP PACKAGE BY 4 MILS (NOTE: LEAD SIDE 3. ONLY). BOTTOM PACKAGE DIMENSION SHALL FOLLOW THE DIMENSION STATED IN THIS
- DRAWING. PLASTIC DIMENSIONS DOES NOT INCLUDE MOLD 4. FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 6 MILS PER SIDE.
- BOTTOM EJECTOR PIN WILL INCLUDE THE COUNTRY OF ORIGIN (COO) AND MOLD CAVITY I.D. 5.

			,	
	INC	HES	MILLIM	ETERS
DIM	MAX	MIN	MAX	MIN
Α	0.337	0.344	8.56	8.74
В	0.150	0.157	3.81	3.99
С	0.061	0.068	1.55	1.73
D	0.008	0.012	0.20	0.31
F	0.016	0.035	0.41	0.89
G	0.025	BSC	0.64 BSC	
Н	0.008	0.018	0.20	0.46
J	0.0098	0.0075	0.249	0.191
K	0.004	0.010	0.10	0.25
L	0.230	0.244	5.84	6.20
Μ	0 °	8 °	0 °	8 °
Ν	0 °	7 °	0°	7°
Р	0.027	0.037	0.69	0.94
Q	0.035	DIA	0.89	DIA
R	0.035	0.045	0.89	1.14
U	0.035	0.045	0.89	1.14
V	0 °	8 °	0 °	8 °

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