Ultra Low Noise 150 mA Low Dropout Voltage Regulator with ON/OFF Control

Housed in a Micro8™ or DFN6 package, the NCP623 delivers up to 150 mA where it exhibits a typical 180 mV dropout. With an incredible noise level of 25 μVRMS (over 100 Hz to 100 kHz, with a 10 nF bypass capacitor), the NCP623 represents the ideal choice for sensitive circuits, especially in portable applications where noise performance and space are premium. The NCP623 also excels in response time and reacts in less than 25 μs when receiving an OFF to ON signal (with no bypass capacitor).

Due to a novel concept, the NCP623 accepts output capacitors without any restrictions regarding their Equivalent Series Resistance (ESR) thus offering an obvious versatility for immediate implementation.

With a typical DC ripple rejection better than −90 dB (−70 dB @ 1.0 kHz), it naturally shields the downstream electronics against choppy power lines.

Additionally, thermal shutdown and short−circuit protection provide the final product with a high degree of ruggedness.

Features

- Very Low Quiescent Current 170 μA (ON, no load), 100 nA (OFF, no load)
- Very Low Dropout Voltage, Typical Value is 137 mV at an Output Current of 100 mA
- Very Low Noise with External Bypass Capacitor (10 nF), Typically 25 μVrms over 100 Hz to 100 kHz
- Internal Thermal Shutdown
- Extremely Tight Line Regulation Typically −90 dB
- Ripple Rejection −70 dB @ 1.0 kHz
- Line Transient Response: 1.0 mV for ΔV_{in} = 3.0 V
- Extremely Tight Load Regulation, Typically 20 mV at ΔI_{out} = 150 mA
- Multiple Output Voltages Available
- Logic Level ON/OFF Control (TTL−CMOS Compatible)
- ESR can vary from 0 to 3.0 Ω
- Pb−Free Packages are Available

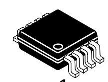
Applications

- All Portable Systems, Battery Powered Systems, Cellular Telephones, Radio Control Systems, Toys and Low Voltage Systems

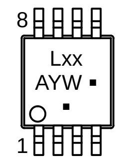
ON Semiconductor®

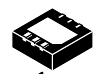
http://onsemi.com

MARKING DIAGRAMS

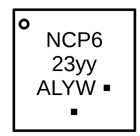


Micro8
DM SUFFIX
CASE 846A





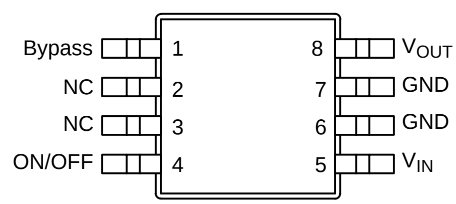
DFN6, 3X3
MN SUFFIX
CASE 488AE



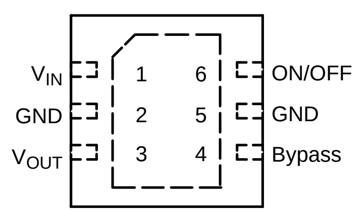
Lxx	= Device Code (Micro8)
	xx = FW, FX, or GN
NCP623yy	= Device Code (DFN6)
	yy = 33, 40, or 50
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



Micro8
(Top View)



DFN6
(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 12 of this data sheet.

May, 2006 − Rev. 4
Publication Order Number:
NCP623/D

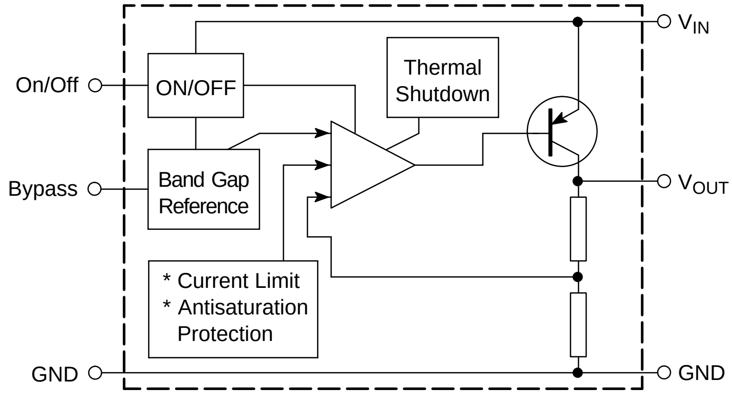


Figure 1. NCP623 Block Diagram

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{in}	12	V
Power Dissipation and Thermal Resistance Maximum Power Dissipation Case 488AE (DFN6, 3x3) MN Suffix Thermal Resistance, Junction−to−Air Thermal Resistance, Junction−to−Case Case 846A (Micro8) DM Suffix Thermal Resistance, Junction−to−Air Thermal Resistance, Junction−to−Case	P_D $R_{\theta JA}$ **psi−JC* or Ψ_{JC} $R_{\theta JA}$ $R_{\theta JC}$	Internally Limited 161 13 240 105	W °C/W
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Maximum Junction Temperature	T_{Jmax}	150	°C
Storage Temperature Range	T_{stg}	−60 to +150	°C
ESD Protection − Human Body Model − Machine Model	V_{ESD}	2000 200	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

*“C’’ (“case’’) is defined as the solder−attach interface between the center of the exposed pad on the bottom of the package, and the board to which it is attached.

** Refer to the JEDEC Specs (51−2, 51−6).

ELECTRICAL CHARACTERISTICS (For typical values T_A = 25°C, for min/max values T_A = −40°C to +85°C, Max T_J = 150°C)

Characteristics	Symbol	Min	Typ	Max	Unit
CONTROL ELECTRICAL CHARACTERISTICS					
Input Voltage Range	$V_{ON/OFF}$	0	−	V_{in}	V
ON/OFF Input Current (All versions) $V_{ON/OFF}$ = 2.4 V	$I_{ON/OFF}$	−	2.5	−	μA
ON/OFF Input Voltages (All versions) Logic “0”, i.e. OFF State Logic “1”, i.e. ON State	$V_{ON/OFF}$	− 2.2	− −	0.3 −	V
CURRENTS PARAMETERS					
Current Consumption in OFF State (All versions) OFF Mode Current: $V_{in} = V_{out}$ + 1.0 V, I_{out} = 0 mA	IQ_{OFF}	−	0.1	2.0	μA
Current Consumption in ON State (All versions) ON Mode Sat Current: $V_{in} = V_{out}$ + 1.0 V, I_{out} = 0 mA	IQ_{ON}	−	170	200	μA
Current Consumption in Saturation ON State (All versions) ON Mode Sat Current: $V_{in} = V_{out}$ − 0.5 V, I_{out} = 0 mA	IQ_{SAT}	−	900	1400	μA
Current Limit $V_{in} = V_{out}$ + 1.0 V, (All versions) Output Short−circuited (Note 1)	I_{MAX}	175	210	−	mA
$V_{in} = V_{out}$ + 1.0 V, T_A = 25°C, 1.0 mA < I_{out} < 150 mA 3.3 Suffix 4.0 Suffix 5.0 Suffix	V_{out}	3.23 3.92 4.90	3.3 4.0 5.0	3.37 4.08 5.1	V
$V_{in} = V_{out}$ + 1.0 V, −40°C < T_A < 85°C 3.3 Suffix 4.0 Suffix 5.0 Suffix	V_{out}	3.18 3.86 4.83	3.3 4.0 5.0	3.42 4.14 5.17	V
LINE AND LOAD REGULATION, DROPOUT VOLTAGES					
Line Regulation (All versions) V_{out} + 1.0 V < V_{in} < 12 V, I_{out} = 60 mA	Reg_{line}	−	2.0	10	mV
Load Regulation (All versions) $V_{in} = V_{out}$ + 1.0 V I_{out} = 1.0 to 60 mA I_{out} = 1.0 to 100 mA I_{out} = 1.0 to 150 mA	Reg_{load}	− − −	8.0 15 20	25 35 45	mV
Dropout Voltage (All versions) I_{out} = 10 mA I_{out} = 100 mA I_{out} = 150 mA	$V_{in} - V_{out}$	− − −	30 137 180	90 230 260	mV
DYNAMIC PARAMETERS					
Ripple Rejection (All versions) $V_{in} = V_{out}$ + 1.0 V, V_{pp} = 1.0 V, f = 1.0 kHz, I_{out} = 60 mA		60	70	−	dB
Line Transient Response $V_{in} = V_{out}$ + 1.0 V to V_{out} + 4.0 V, I_{out} = 60 mA, $d(V_{in})/dt$ = 15 mV/μs		−	1.0	−	mV
Output Noise Voltage (All versions) C_{out} = 1.0 μF, I_{out} = 60 mA, f = 100 Hz to 100 kHz C_{bypass} = 10 nF C_{bypass} = 1.0 nF C_{bypass} = 0 nF	V_{RMS}	− − −	25 40 65	− − −	μVrms
Output Noise Density C_{out} = 1.0 μF, I_{out} = 60 mA, f = 1.0 kHz	V_N	−	230	−	nV/ $\sqrt{Hz}$
Output Rise Time (All versions) C_{out} = 1.0 μF, I_{out} = 30 mA, $V_{ON/OFF}$ = 0 to 2.4 V 1% of ON/OFF Signal to 99% of Nominal Output Voltage Without Bypass Capacitor With C_{bypass} = 10 nF	t_r	− −	40 1.1	− −	μs ms
THERMAL SHUTDOWN					
Thermal Shutdown (All versions)		−	150	−	°C

1. I_{out} (Output Current) is the measured current when the output voltage drops below 0.3 V with respect to V_{out} at I_{out} = 30 mA.

DEFINITIONS

Load Regulation − The change in output voltage for a change in load current at constant chip temperature.

Dropout Voltage − The input/output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops 100 mV below its nominal value (which is measured at 1.0 V differential), dropout voltage is affected by junction temperature, load current and minimum input supply requirements.

Output Noise Voltage − The RMS AC voltage at the output with a constant load and no input ripple, measured over a specified frequency range.

Maximum Power Dissipation − The maximum total dissipation for which the regulator will operate within specifications.

Quiescent Current − Current which is used to operate the regulator chip and is not delivered to the load.

Line Regulation − The change in input voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Line Transient Response − Typical over− and undershoot response when input voltage is excited with a given slope.

Thermal Protection − Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically 150°C, the regulator turns off. This feature is provided to prevent catastrophic failures from accidental overheating.

Maximum Package Power Dissipation − The maximum package power dissipation is the power dissipation level at which the junction temperature reaches its maximum value i.e. 125°C. The junction temperature is rising while the difference between the input power (V_{CC} X I_{CC}) and the output power (V_{out} X I_{out}) is increasing.

Depending on ambient temperature, it is possible to calculate the maximum power dissipation, maximum load current or maximum input voltage (see Application Hints: Protection).

The maximum power dissipation supported by the device is a lot increased when using appropriate application design. Mounting pad configuration on the PCB, the board material and also the ambient temperature are affected the rate of temperature rise. It means that when the I_C has good thermal conductivity through PCB, the junction temperature will be “low” even if the power dissipation is great.

The thermal resistance of the whole circuit can be evaluated by deliberately activating the thermal shutdown of the circuit (by increasing the output current or raising the input voltage for example).

Then you can calculate the power dissipation by subtracting the output power from the input power. All variables are then well known: power dissipation, thermal shutdown temperature (150°C for NCP623) and ambient temperature.

APPLICATION HINTS

Input Decoupling − As with any regulator, it is necessary to reduce the dynamic impedance of the supply rail that feeds the component. A 1.0 μF capacitor either ceramic or tantalum is recommended and should be connected close to the NCP623 package. Higher values will correspondingly improve the overall line transient response.

Output Decoupling − Due to a novel concept, the NCP623 is a stable component and does not require any Equivalent Series Resistance (ESR) neither a minimum output current. Capacitors exhibiting ESRs ranging from a few mΩ up to 3.0 Ω can thus safely be used. The minimum decoupling value is 1.0 μF and can be augmented to fulfill stringent load transient requirements. The regulator accepts ceramic chip capacitors as well as tantalum devices.

Noise Performances − Unlike other LDOs, the NCP623 is a true low−noise regulator. With a 10 nF bypass capacitor, it typically reaches the incredible level of 25 μVRMS overall noise between 100 Hz and 100 kHz. To give maximum insight on noise specifications, ON Semiconductor includes spectral density graphics as well as noise dependency versus bypass capacitor.

The bypass capacitor impacts the startup phase of the NCP623 as depicted by the data−sheet curves. A typical 1.0 ms settling time is achieved with a 10 nF bypass capacitor. However, due to its low−noise architecture, the NCP623 can operate without bypass and thus offers a typical 20 μs startup phase. In that case, the typical output noise stays lower than 65 μVRMS between 100 Hz − 100 kHz.

Protections − The NCP623 hosts several protections, conferring natural ruggedness and reliability to the products implementing the component. The output current is internally limited to a minimum of 175 mA while temperature shutdown occurs if the die heats up beyond 150°C. These value lets you assess the maximum differential voltage the device can sustain at a given output current before its protections come into play.

The maximum dissipation the package can handle is given by:

$$P_{max} = \frac{T_{Jmax} - T_A}{R_{\theta JA}}$$

If T_{Jmax} is internally limited to 150°C, then the NCP623 can dissipate up to 595 mW @ 25°C.

The power dissipated by the NCP623 can be calculated from the following formula:

$$Ptot = \langle V_{in} \cdot I_{gnd}(I_{out}) \rangle + \langle V_{in} - V_{out} \rangle \cdot I_{out}$$

or

$$Vin_{max} = \frac{Ptot + V_{out} \cdot I_{out}}{I_{gnd} + I_{out}}$$

If a 150 mA output current is needed, the ground current is extracted from the data−sheet curves: 6.5 mA @ 150 mA. For a NCP623NW28R2 (2.8 V), the maximum input voltage will then be 6.48 V, a rather comfortable margin.

Typical Application − The following figure portraits the typical application for the NCP623 where both input/output decoupling capacitors appear.

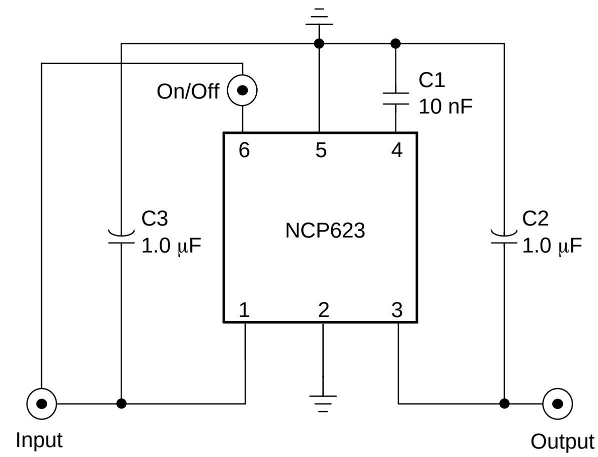


Figure 2. A Typical NCP623 Application with Recommended Capacitor Values (DFN6)

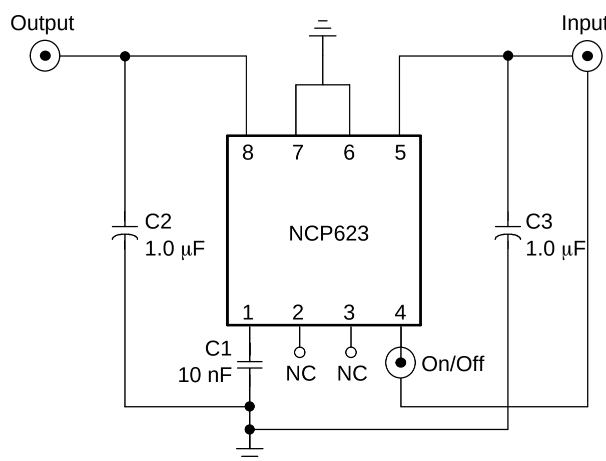


Figure 3. A Typical NCP623 Application with Recommended Capacitor Values (Micro8)

NCP623 Wake−up Improvement − In portable applications, an immediate response to an enable signal is vital. If noise is not of concern, the NCP623 without a bypass capacitor settles in nearly 20 μs and typically delivers 65 μVRMS between 100 Hz and 100 kHz.

In ultra low−noise systems, the designer needs a 10 nF bypass capacitor to decrease the noise down to 25 μVRMS between 100 Hz and 100 kHz. With the addition of the 10 nF capacitor, the wake−up time expands up to 1.0 ms as shown on the data−sheet curves. If an immediate response is wanted, following figure's circuit gives a solution to charge the bypass capacitor with the enable signal without degrading the noise response of the NCP623.

At power−on, C4 is discharged. When the control logic sends its wake−up signal by going to a high level, the PNP base is momentarily tied to ground. The PNP switch closes and immediately charges the bypass capacitor C1 toward its operating value. After a few μs, the PNP opens and becomes totally transparent to the regulator.

This circuit improves the response time of the regulator which drops from 1.0 ms down to 30 μs. The value of C4 needs to be tweaked in order to avoid any bypass capacitor overload during the wake−up transient.

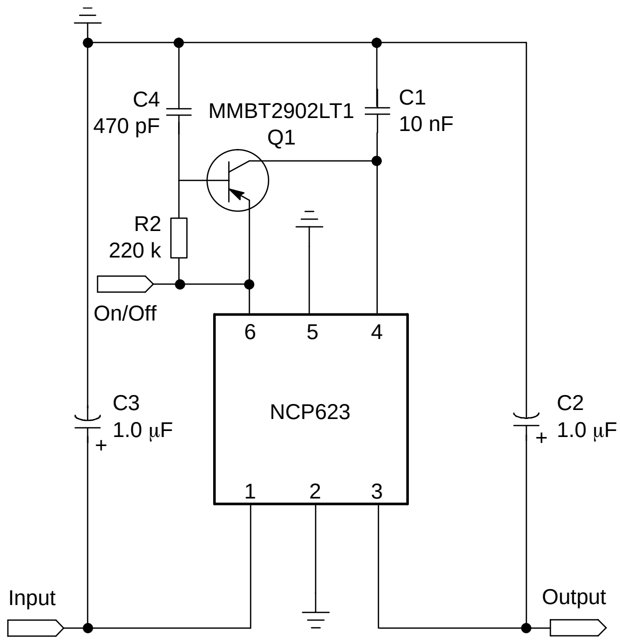


Figure 4. A PNP Transistor Drives the Bypass Pin when Enable Goes High (DFN6)

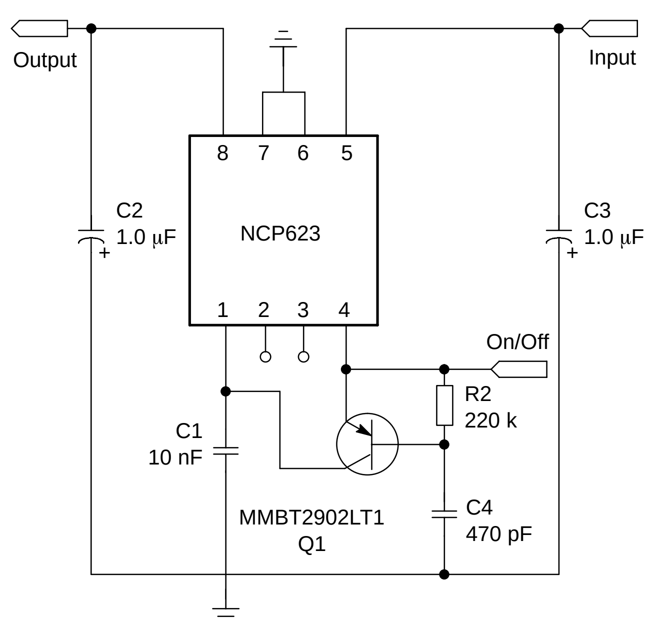


Figure 5. A PNP Transistor Drives the Bypass Pin when Enable Goes High (Micro8)

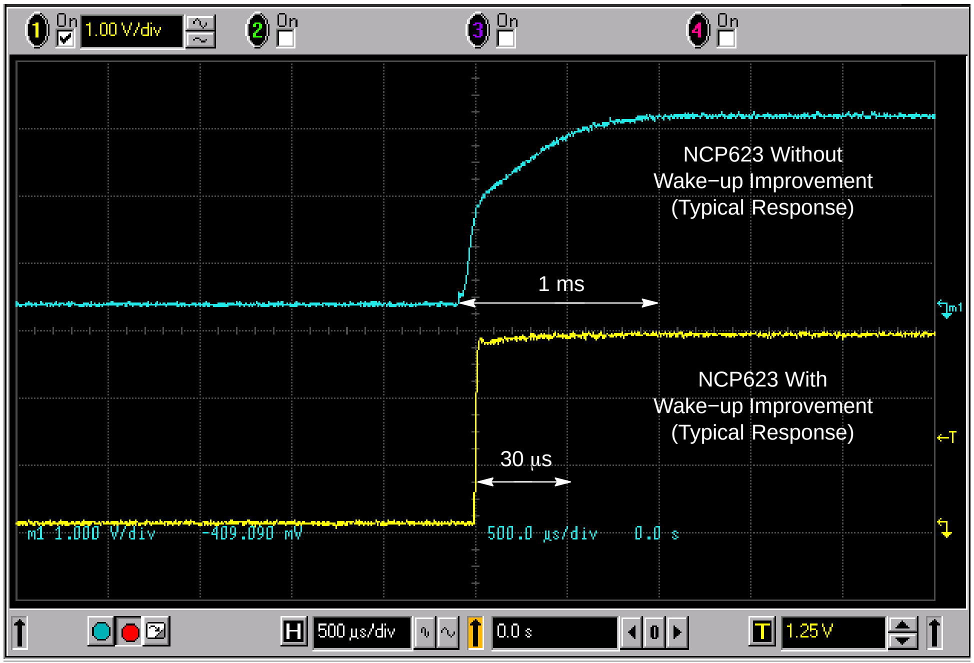


Figure 6. NCP623 Wake−up Improvement with Small PNP Transistor

The PNP being wired upon the bypass pin, it shall not degrade the noise response of the NCP623. Figure 7 confirms the good behavior of the integrated circuit in this area which reaches a typical noise level of 26 μVRMS (100 Hz to 100 kHz) at I_{out} = 60 mA.

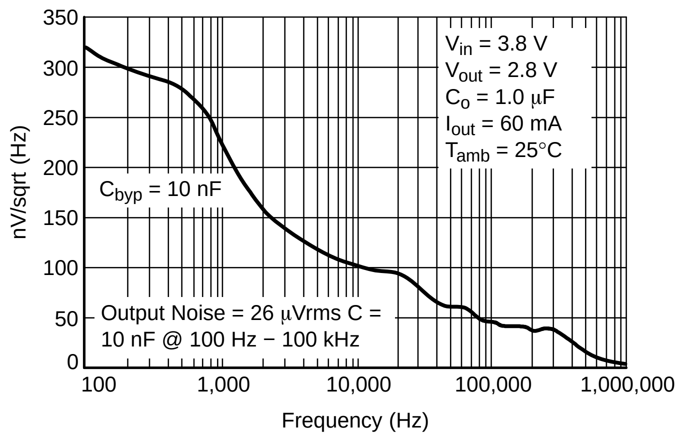


Figure 7. Noise Density of the NCP623 with a 10 nF Bypass Capacitor and a Wake−up Improvement Network

TYPICAL PERFORMANCE CHARACTERISTICS

Ground Current Performances

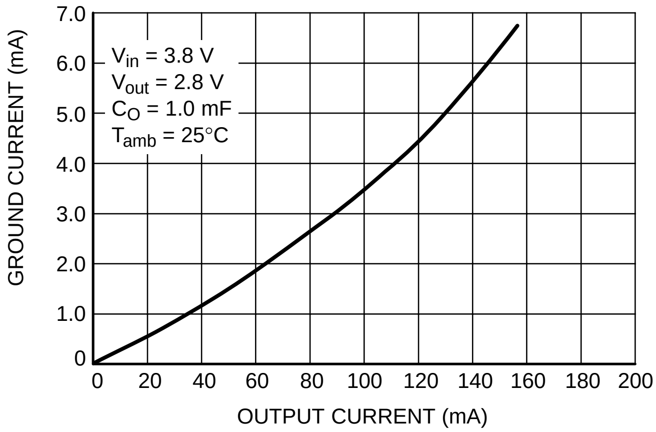


Figure 8. Ground Current versus Output Current

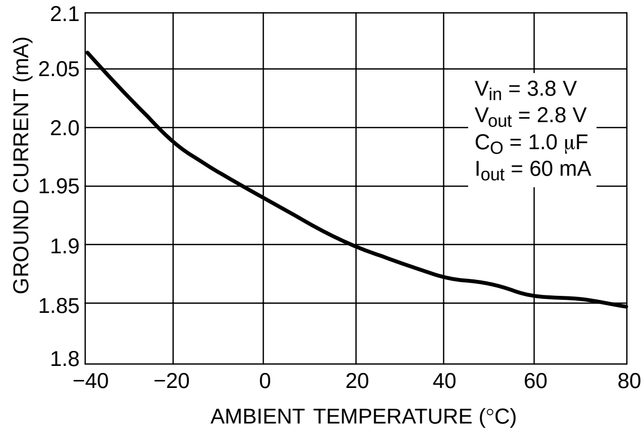


Figure 9. Ground Current versus Ambient Temperature

Line Transient Response and Output Voltage

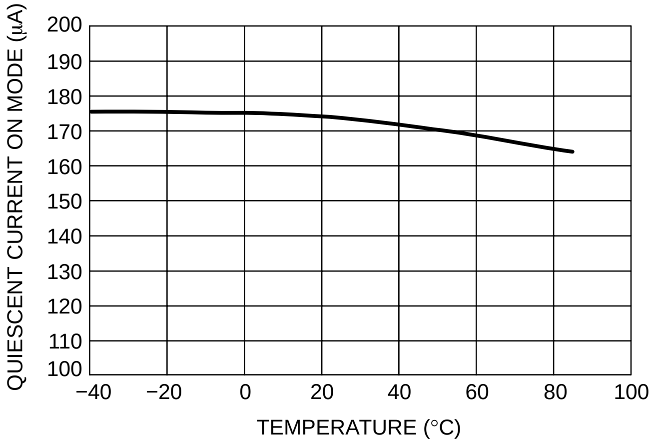


Figure 10. Quiescent Current versus Temperature

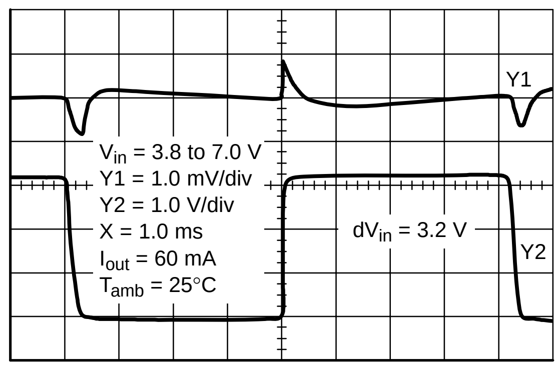
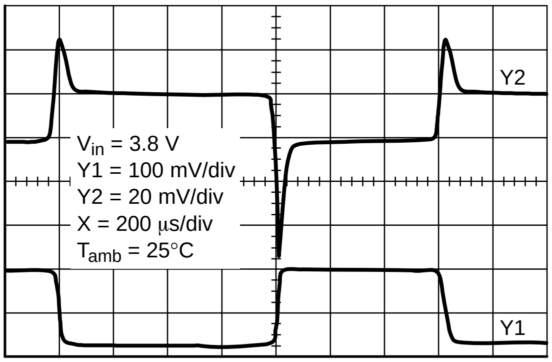


Figure 11. Line Transient Response

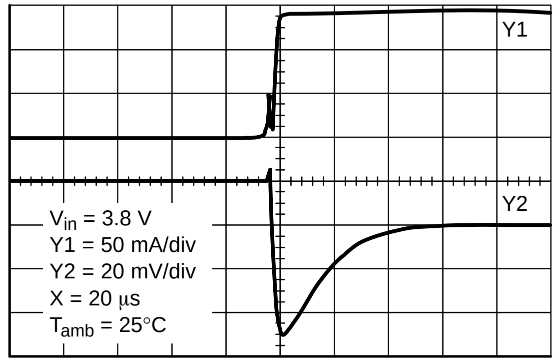
TYPICAL PERFORMANCE CHARACTERISTICS

Load Transient Response versus Load Current Slope



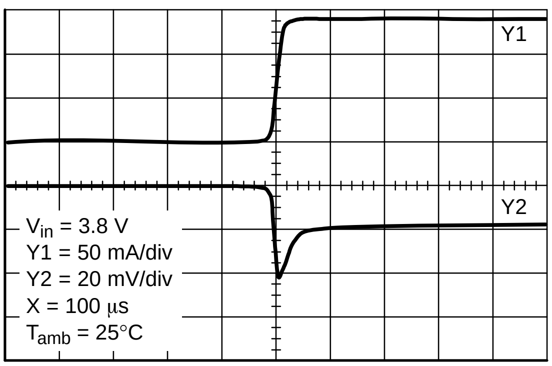
Y1: OUTPUT CURRENT, Y2: OUTPUT VOLTAGE

Figure 12. I_{out} = 3.0 mA to 150 mA



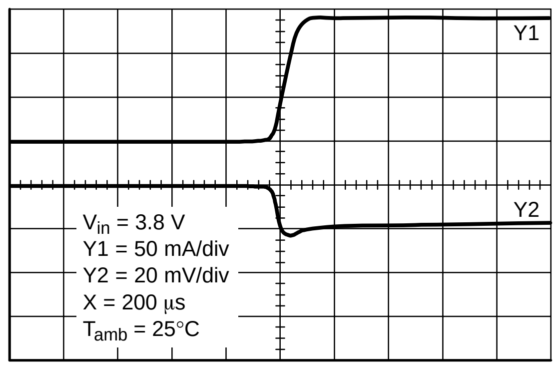
Y1: OUTPUT CURRENT, Y2: OUTPUT VOLTAGE

Figure 13. I_{Slope} = 100 mA/μs (Large Scale)
I_{out} = 3.0 mA to 150 mA



Y1: OUTPUT CURRENT, Y2: OUTPUT VOLTAGE

Figure 14. I_{Slope} = 6.0 mA/μs (Large Scale)
I_{out} = 3.0 mA to 150 mA



Y1: OUTPUT CURRENT, Y2: OUTPUT VOLTAGE

Figure 15. I_{Slope} = 2.0 mA/μs (Large Scale)
I_{out} = 3.0 mA to 150 mA

TYPICAL PERFORMANCE CHARACTERISTICS

Noise Performances

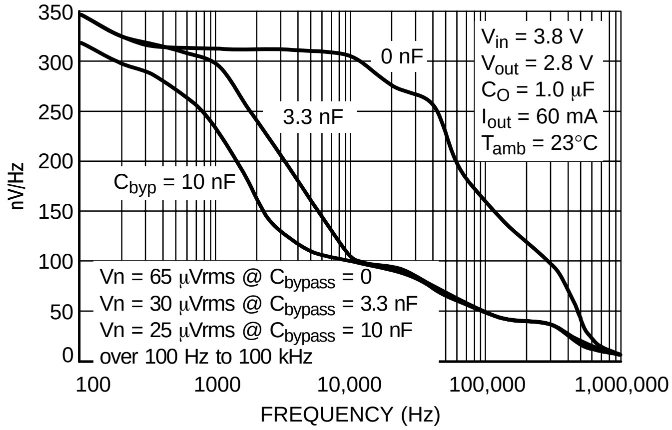


Figure 16. Noise Density versus Bypass Capacitor

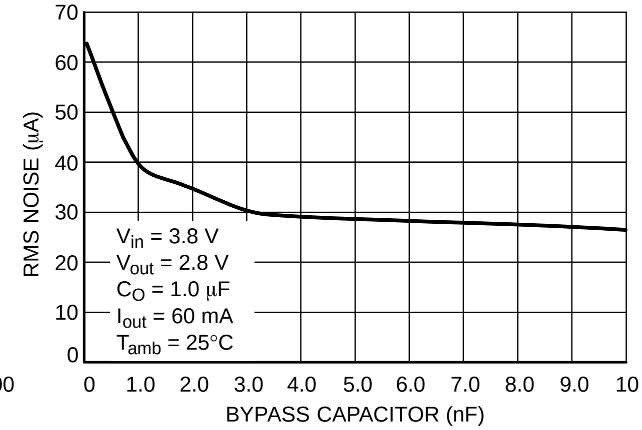


Figure 17. RMS Noise versus Bypass Capacitor (100 Hz − 100 kHz)

Settling Time Performances

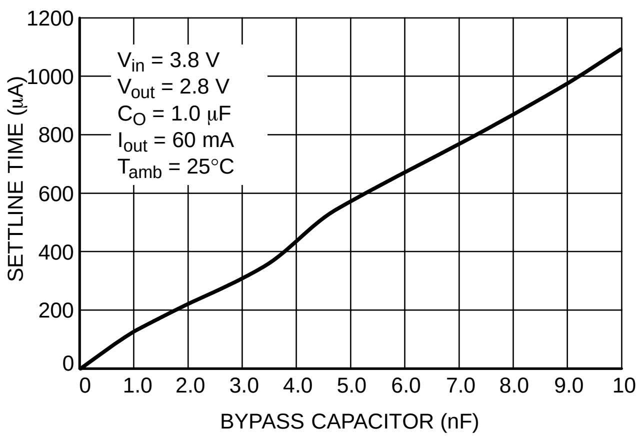


Figure 18. Output Voltage Settling Time versus Bypass Capacitor

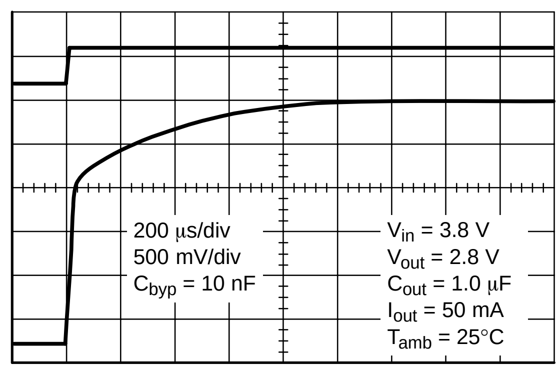


Figure 19. Output Voltage Settling Shape C_{bypass} = 10 nF

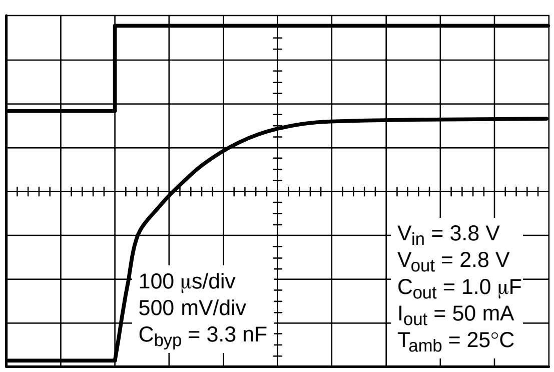


Figure 20. Output Voltage Settling Shape C_{bypass} = 3.3 nF

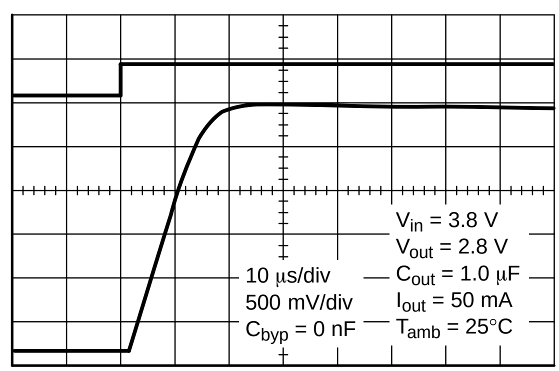


Figure 21. Output Voltage Settling Shape without Bypass Capacitor

TYPICAL PERFORMANCE CHARACTERISTICS

Dropout Voltage

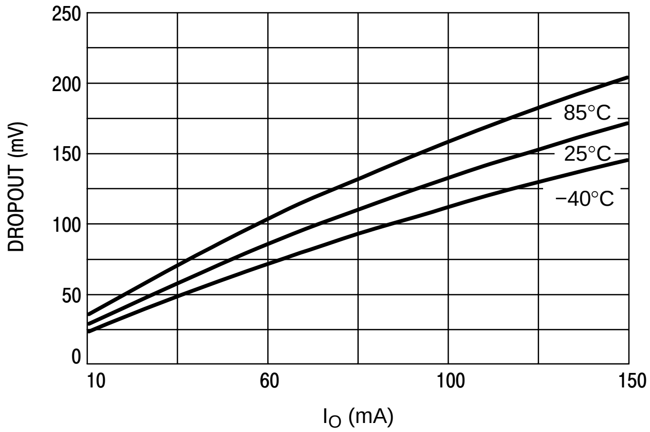


Figure 22. Dropout Voltage versus I_{out}

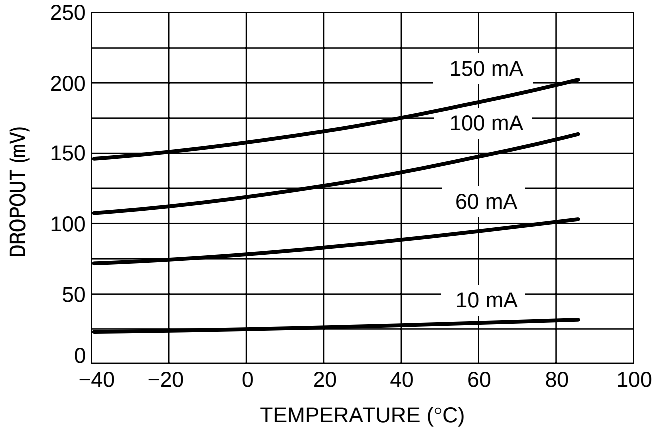


Figure 23. Dropout Voltage versus Temperature

Output Voltage

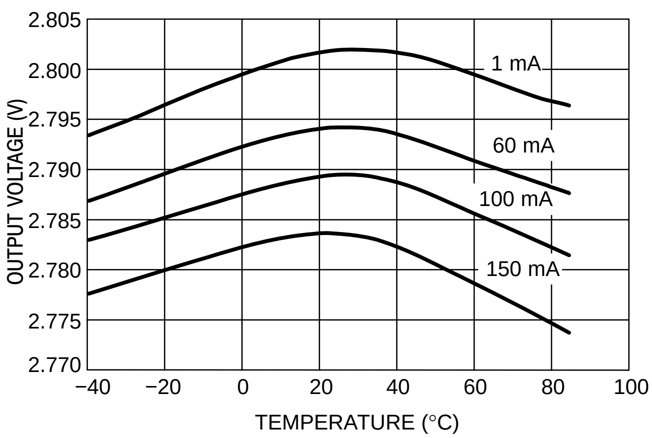


Figure 24. Output Voltage versus Temperature

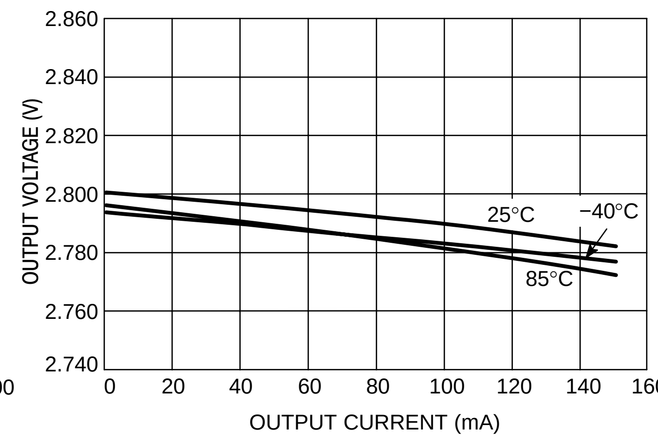


Figure 25. Output Voltage versus I_{out}

Ripple Rejection Performances

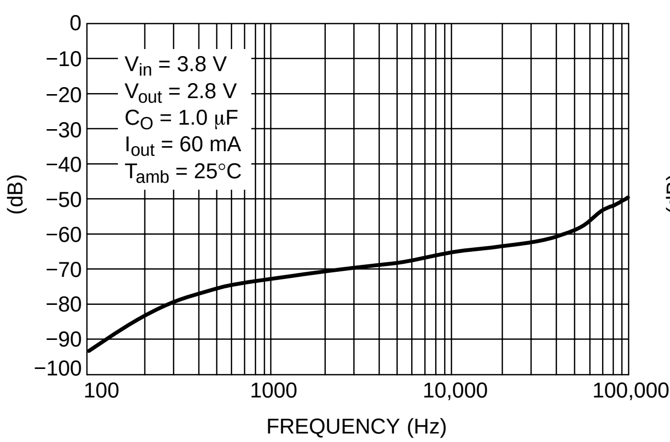


Figure 26. Ripple Rejection versus Frequency with 10 nF Bypass Capacitor

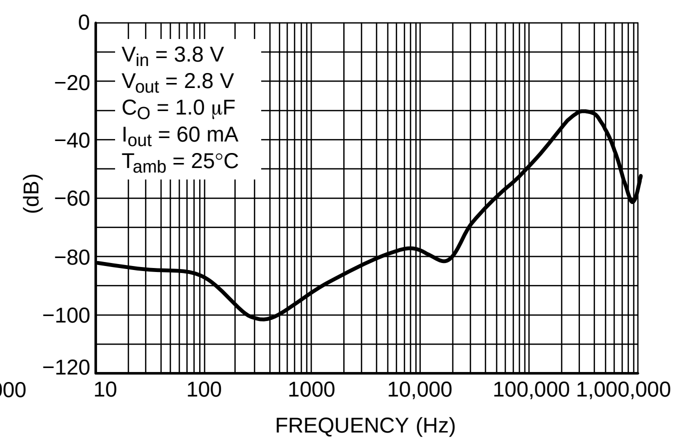


Figure 27. Ripple Rejection versus Frequency without Bypass Capacitor

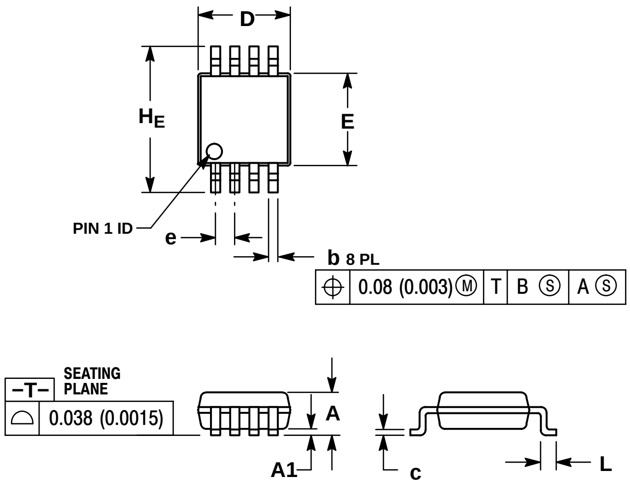
ORDERING INFORMATION

Device	Version	Package	Shipping†
NCP623DM−3.3R2	3.3 V	Micro8	4000 Tape & Reel
NCP623DM−3.3R2G		Micro8 (Pb−Free)	
NCP623DM−4.0R2	4.0 V	Micro8	
NCP623DM−4.0R2G		Micro8 (Pb−Free)	
NCP623DM−5.0R2	5.0 V	Micro8	
NCP623DM−5.0R2G		Micro8 (Pb−Free)	
NCP623MN−3.3R2	3.3 V	DFN6, 3x3	3000 Tape & Reel
NCP623MN−4.0R2	4.0 V		
NCP623MN−4.0R2G		DFN6, 3x3 (Pb−Free)	
NCP623MN−5.0R2	5.0 V	DFN6, 3x3	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

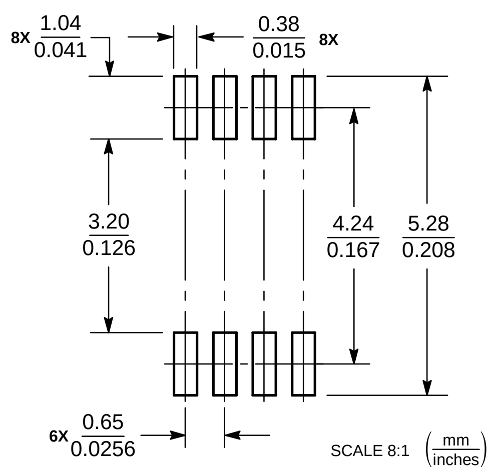
Micro8™
CASE 846A−02
ISSUE G



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846A−01 OBSOLETE, NEW STANDARD 846A−02.

	MILLIMETERS			INCHES		
DIM	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**
A	−−	−−	1.10	−−	−−	0.043
A1	0.05	0.08	0.15	0.002	0.003	0.006
b	0.25	0.33	0.40	0.010	0.013	0.016
c	0.13	0.18	0.23	0.005	0.007	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	2.90	3.00	3.10	0.114	0.118	0.122
e	0.65 BSC			0.026 BSC		
L	0.40	0.55	0.70	0.016	0.021	0.028
H_E	4.75	4.90	5.05	0.187	0.193	0.199

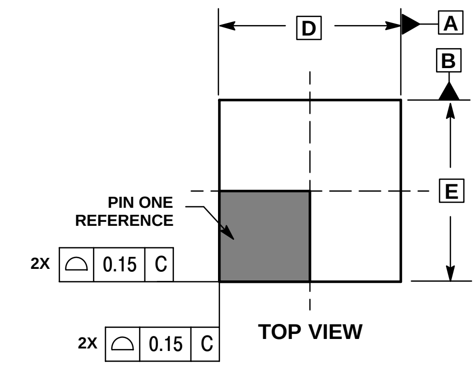
SOLDERING FOOTPRINT*

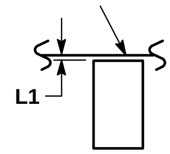


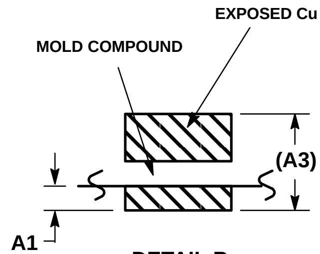
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

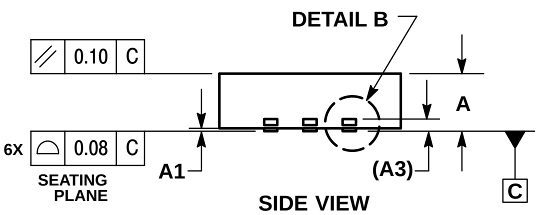
PACKAGE DIMENSIONS

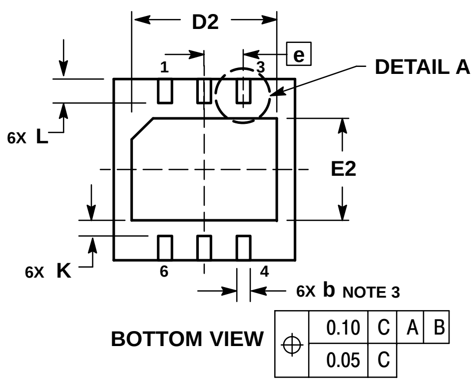
6 PIN DFN, 3x3x0.9
CASE 488AE−01
ISSUE B







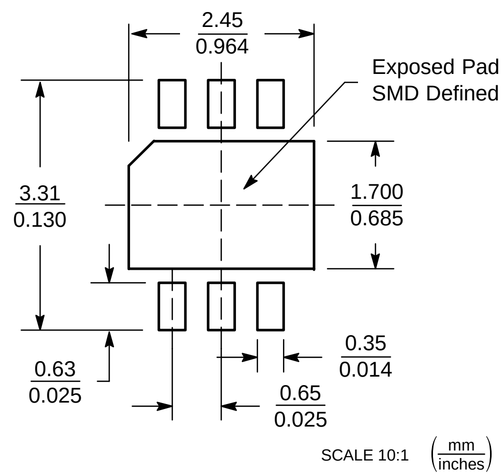




NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. TERMINAL b MAY HAVE MOLD COMPOUND MATERIAL ALONG SIDE EDGE. MOLD FLASHING MAY NOT EXCEED 30 MICRONS ONTO BOTTOM SURFACE OF TERMINAL b.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20	0.25
b	0.18	0.30
D	3.00 BSC	
D2	2.25	2.55
E	3.00 BSC	
E2	1.55	1.85
e	0.65 BSC	
K	0.20	−−−
L	0.30	0.50
L1	0.00	0.021

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PUBLICATION ORDERING INFORMATION

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