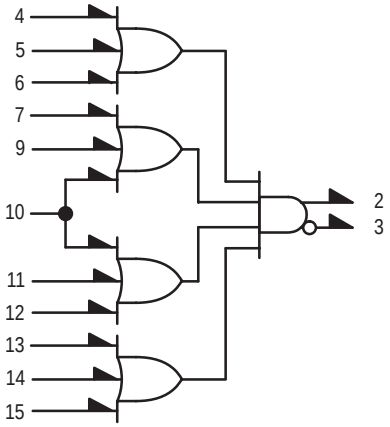
MC10H121

4-Wide OR-AND/$\overline{\text{OR-AND}}$ Gate

The MC10H121 is a basic logic building block providing the simultaneous OR–AND/OR–AND–Invert function, useful in data control and digital multiplexing applications. This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power– supply current.

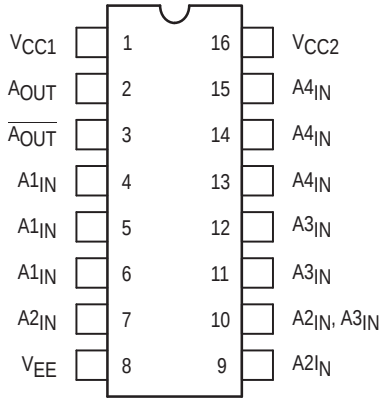
- Propagation Delay, 1.0 ns Typical
- Power Dissipation 100 mW/Gate Typical (same as MECL 10K)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K–Compatible

LOGIC DIAGRAM



V_{CC1} = PIN 1
V_{CC2} = PIN 16
V_{EE} = PIN 8

DIP PIN ASSIGNMENT

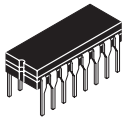


Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18 of the ON Semiconductor MECL Data Book (DL122/D).

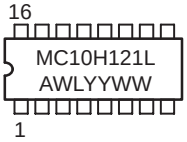
ON Semiconductor

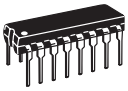
http://onsemi.com

MARKING DIAGRAMS

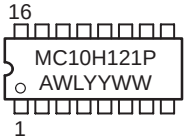


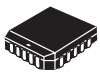
CDIP–16
L SUFFIX
CASE 620A





PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H121L	CDIP–16	25 Units/Rail
MC10H121P	PDIP–16	25 Units/Rail
MC10H121FN	PLCC–20	46 Units/Rail

MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0)	–8.0 to 0	Vdc
V_I	Input Voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_{out}	Output Current — Continuous — Surge	50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range — Plastic — Ceramic	–55 to +150 –55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%) (See Note 1.)

		0°		25°		75°		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
I_E	Power Supply Current	—	29	—	26	—	29	mA
I_{inH}	Input Current High Pins 3, 4, 5, 6, 7, 9 11, 12, 13, 14, 15 Pin 10	 — —	 500 610	 — —	 295 360	 — —	 295 360	µA
I_{inL}	Input Current Low	0.5	—	0.5	—	0.3	—	µA
V_{OH}	High Output Voltage	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
V_{OL}	Low Output Voltage	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
V_{IH}	High Input Voltage	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
V_{IL}	Low Input Voltage	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

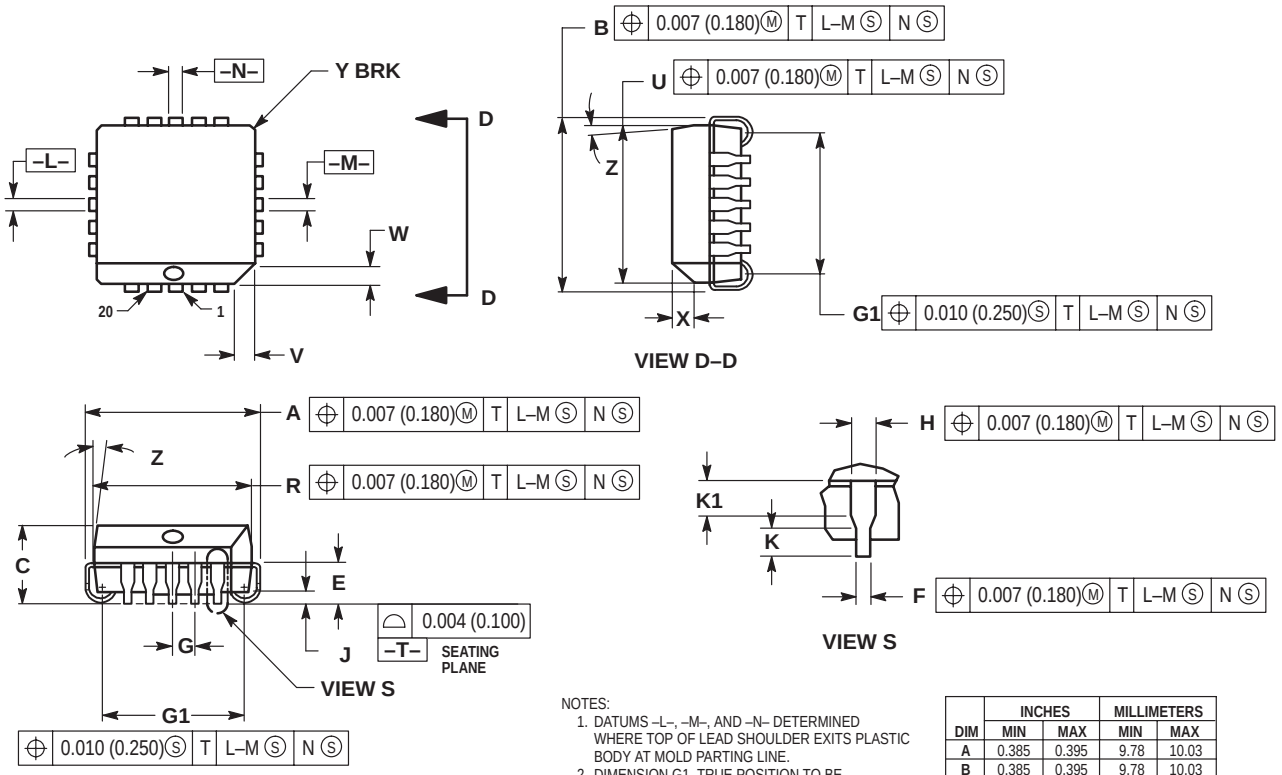
AC PARAMETERS

t_{pd}	Propagation Delay Pin 10 Only Exclude Pin 10	 0.45 0.55	 1.8 1.95	 0.45 0.6	 1.8 2.0	 0.55 0.7	 2.2 2.4	ns
t_r	Rise Time	0.5	1.7	0.5	1.8	0.5	1.9	ns
t_f	Fall Time	0.5	1.7	0.5	1.8	0.5	1.9	ns

1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts.

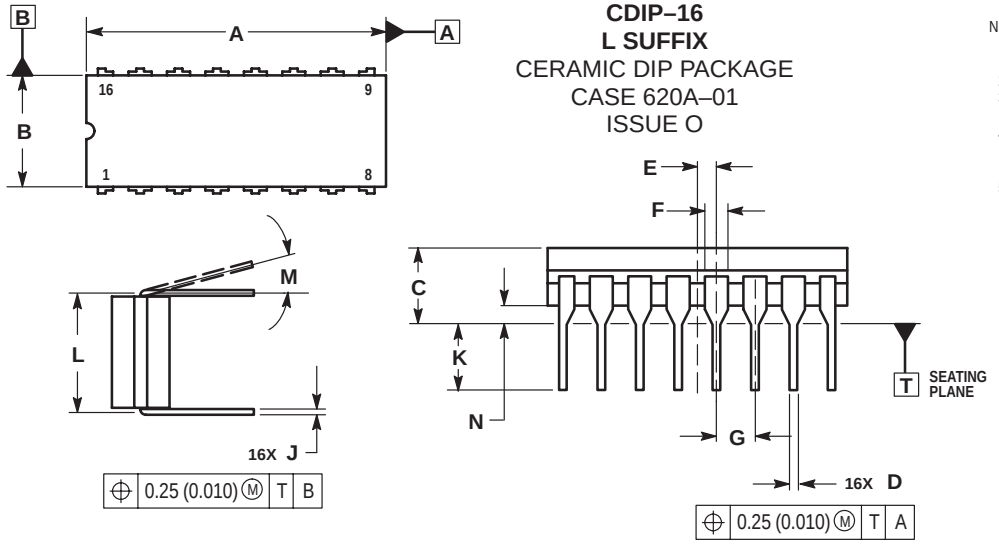
PACKAGE DIMENSIONS

PLCC–20
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 775–02
ISSUE C



NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

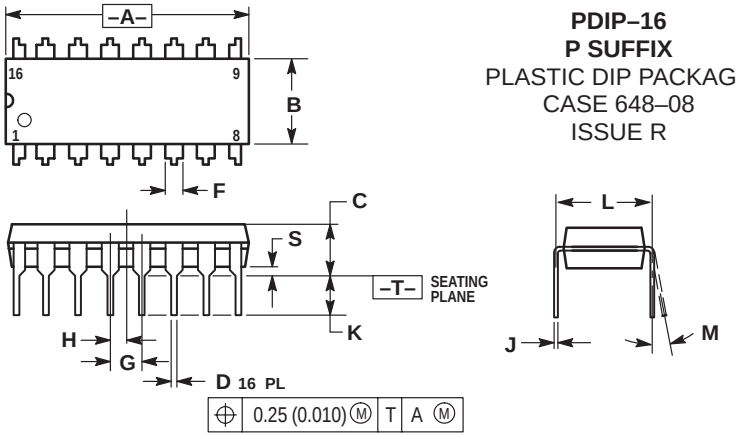
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2 °	10 °	2 °	10 °
G1	0.310	0.330	7.88	8.38
K1	0.040	—	1.02	—



CDIP–16
L SUFFIX
CERAMIC DIP PACKAGE
CASE 620A–01
ISSUE O

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.
5 THIS DRAWING REPLACES OBSOLETE CASE OUTLINE 620–10.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0 °	15 °	0 °	15 °
N	0.020	0.040	0.51	1.01



PDIP–16
P SUFFIX
PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

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