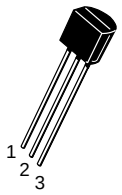
FET Transistor
N–Channel — Enhancement

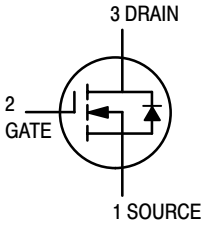
VN0610LL

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	60	Vdc
Drain–Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	60	Vdc
Gate–Source Voltage – Continuous – Non–repetitive ($t_p \leq 50$ μs)	 V_{GS} V_{GSM}	 ± 20 ± 40	 Vdc Vpk
Drain Current Continuous Pulsed	 I_D I_{DM}	 190 1000	mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	400 3.2	mW mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to +150	°C



CASE 29–11, STYLE 22
TO–92 (TO–226AA)



THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	312.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/16” from case for 10 seconds	T_L	300	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 100 μA)	$V_{(BR)DSS}$	60	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 48 Vdc, V_{GS} = 0) (V_{DS} = 48 Vdc, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 10 500	μAdc
Gate–Body Leakage Current, Forward (V_{GSF} = 30 V, V_{DS} = 0)	I_{GSSF}	—	–100	nAdc
ON CHARACTERISTICS[1]				
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1.0 mA)	$V_{GS(th)}$	0.8	2.5	Vdc
Static Drain–Source On–Resistance (V_{GS} = 10 V, I_D = 500 mA) (V_{GS} = 10 V, I_D = 500 mA, T_C = 125°C)	$r_{DS(on)}$	 — —	 5.0 9.0	Ω
Drain–Source On–Voltage (V_{GS} = 5.0 V, I_D = 200 mA) (V_{GS} = 10 V, I_D = 500 mA)	$V_{DS(on)}$	 — —	 1.5 2.5	Vdc
On–State Drain Current (V_{GS} = 10 V, $V_{DS} \geq 2.0\ V_{DS(on)}$)	$I_{D(on)}$	750	—	mAdc
Forward Transconductance ($V_{DS} \geq 2.0\ V_{DS(on)}$, I_D = 500 mA)	g_{fs}	100	—	μmhos

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (Continued)

Characteristic		Symbol	Min	Max	Unit
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	60	pF
Output Capacitance		C_{oss}	—	25	
Reverse Transfer Capacitance		C_{rss}	—	5.0	
SWITCHING CHARACTERISTICS(1)					
Turn–On Delay Time	(V_{DD} = 15 Vdc, I_D = 600 mA, R_{gen} = 25 Ω, R_L = 23 Ω)	t_{on}	—	10	ns
Turn–Off Delay Time		t_{off}	—	10	

1. Pulse Test: Pulse Width ≤ 300 ms, Duty Cycle ≤ 10%.

RESISTIVE SWITCHING

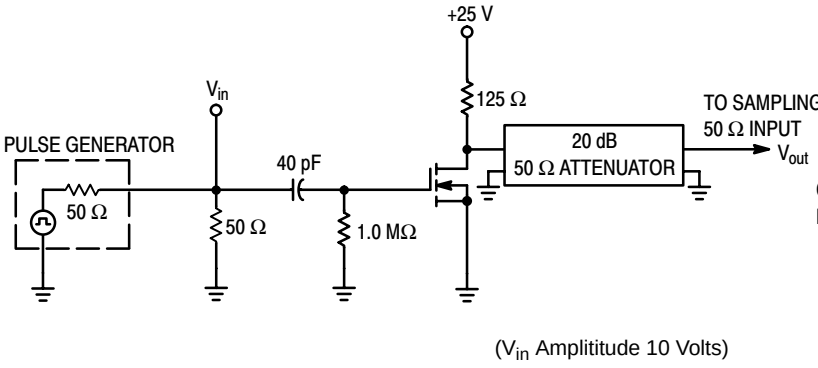


Figure 1. Switching Test Circuit

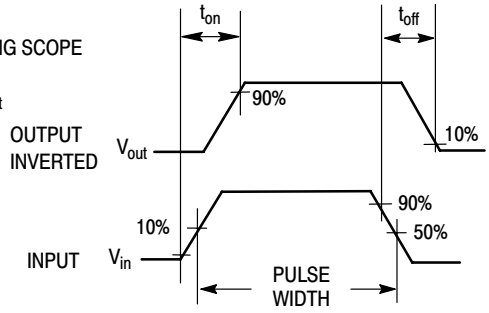


Figure 2. Switching Waveforms

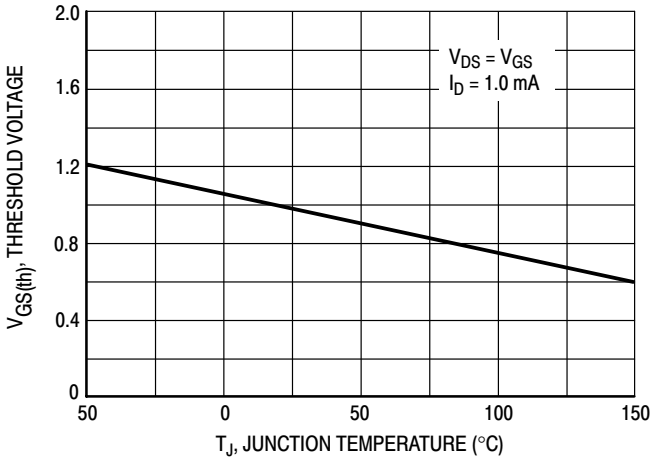


Figure 3. $V_{GS(th)}$ Normalized versus Temperature

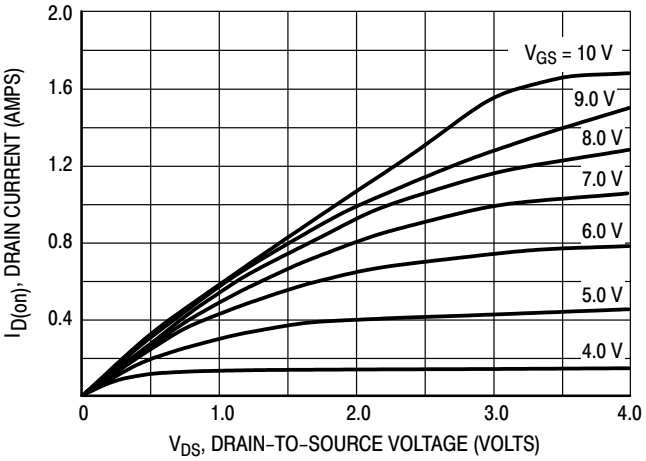


Figure 4. On−Region Characteristics

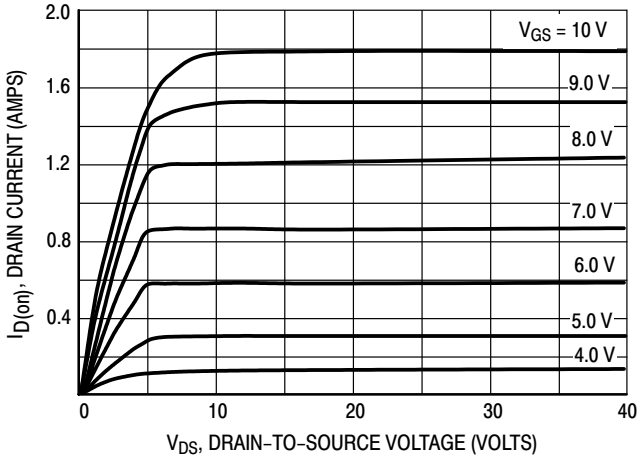


Figure 5. Output Characteristics

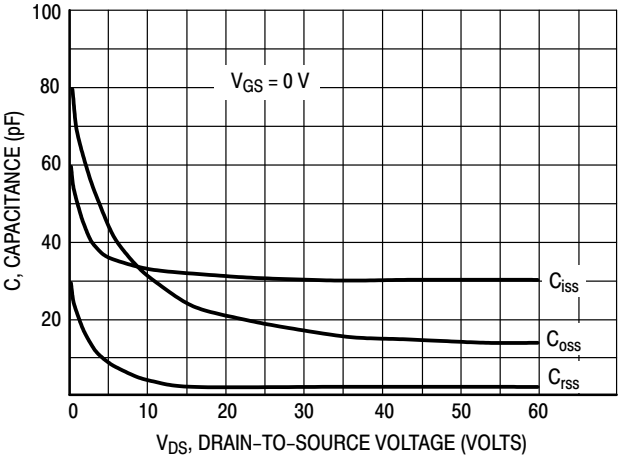


Figure 6. Capacitance versus Drain−To−Source Voltage

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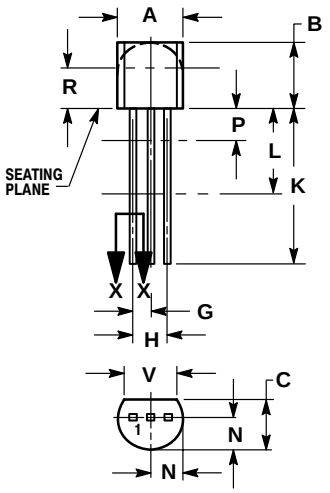
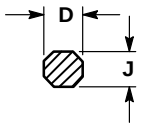
PACKAGE DIMENSIONS

TO–92 (TO–226AA)
CASE 29–11
ISSUE AL





SECTION X–X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.021	0.407	0.533
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.115	---	2.93	---
V	0.135	---	3.43	---

STYLE 22:
PIN 1. SOURCE
2. GATE
3. DRAIN

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