

MC100EPT23

Dual Differential LVPECL to LVTTTL Translator

The MC100EPT23 is a dual differential LVPECL to LVTTTL translator. Because LVPECL (Positive ECL) levels are used only +3.3V and ground are required. The small outline 8-lead SOIC package and the dual gate design of the EPT23 makes it ideal for applications which require the translation of a clock and a data signal.

The EPT23 is available in only the ECL 100K standard. Since there are no LVPECL outputs or an external V_{BB} reference, the EPT23 does not require both ECL standard versions. The LVPECL inputs are differential. Therefore, the MC100EPT23 can accept any standard differential LVPECL input referenced from a V_{CC} of +3.3V.

- 1.5ns Typical Propagation Delay
- Minimum Operating Frequency > 275MHz
- Differential LVPECL Inputs
- Small Outline SOIC Package
- 24mA LVTTTL Outputs
- Flow Through Pinouts
- Internal Input Resistors: Pulldown on D, Pulldown and Pullup on \overline{D}
- Q Output will default LOW with inputs open or at GND
- ESD Protection: >1.2KV HBM, >150V MM
- Moisture Sensitivity Level 1, Indefinite Time Out of Drypack.
For Additional Information, See Application Note AND8003/D
- Flammability Rating: UL-94 code V-0 @ 1/8",
Oxygen Index 28 to 34
- Transistor Count = 91 devices

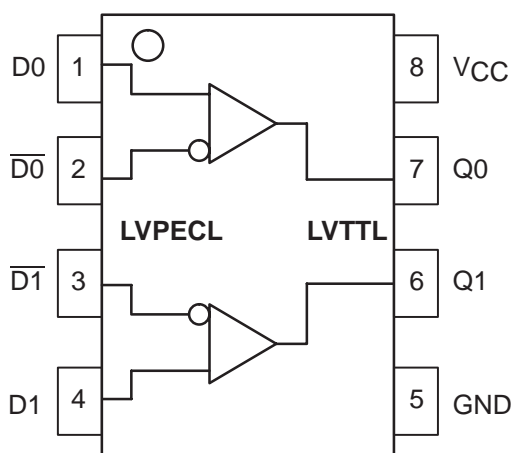


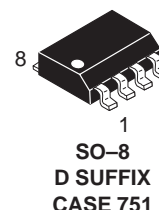
Figure 1. 8-Lead Pinout and Logic Diagram



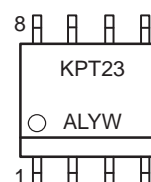
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MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

PIN DESCRIPTION

PIN	FUNCTION
Q0, Q1	LVTTTL Outputs
D0, D1, $\overline{D0}$, $\overline{D1}$	Differential LVPECL Inputs
V_{CC}	Positive Supply
GND	Ground

ORDERING INFORMATION

Device	Package	Shipping
MC100EPT23D	SOIC	98 Units/Rail
MC100EPT23DR2	SOIC	2500 Tape & Reel

MC100EPT23

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply (GND = 0V)	0 to 3.8	VDC
V_I	Input Voltage (GND = 0V, V_I not more positive than V_{CC})	0 to 3.8	VDC
I_{out}	Output Current Continuous Surge	50 100	mA
T_A	Operating Temperature Range	−40 to +85	°C
T_{stg}	Storage Temperature	−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient) Still Air 500lfpm	190 130	°C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	41 to 44 ± 5%	°C/W
T_{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

DC CHARACTERISTICS ($V_{CC} = 3.3V \pm 0.3V$; GND = 0V; $T_A = -40^\circ\text{C}$ to 85°C)

Symbol	Characteristic	Min	Typ	Max	Unit
I_{CCH}	Power Supply Current (Outputs set to HIGH)	10	18	25	mA
I_{CCL}	Power Supply Current (Outputs set to LOW)	15	26	33	mA
V_{IH}	Input HIGH Voltage ($V_{CC} = 3.3$) (Note 1.)	2135		2420	mV
V_{IL}	Input LOW Voltage ($V_{CC} = 3.3$) (Note 1.)	1490		1825	mV
I_{IH}	Input HIGH Current			150	μA
I_{IL}	Input LOW Current D D	−150		0.5	μA
V_{OH}	Output HIGH Voltage ($I_{OH} = -3.0\text{mA}$) (Note 2.)	2.4			V
V_{OL}	Output LOW Voltage ($I_{OL} = 24\text{mA}$) (Note 2.)			0.5	V
I_{OS}	Output Short Circuit Current	−180		−50	mA
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 3.)	2.0		3.3	V


NOTE: 100EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

1. All values vary 1:1 with V_{CC} .
2. All loading with 500 ohms to GND, $C_L = 20\text{pF}$.
3. V_{IHCMR} min varies 1:1 with GND, max varies 1:1 with V_{CC} .

AC CHARACTERISTICS ($V_{CC} = 3.3V \pm 0.3V$; GND = 0V)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency (Note 4.)	275	350		275	350		275	350		MHz
t_{PLH} , t_{PHL}	Propagation Delay to Output Differential (Note 5.)	1.2 1.2	1.5 1.5	1.8 1.8	1.2 1.2	1.5 1.5	1.8 1.8	1.3 1.2	1.7 1.5	2.2 1.8	ns
$t_{SK+ +}$ $t_{SK- -}$ t_{SKPP}	Output-to-Output Skew++ Output-to-Output Skew-- Part-to-Part Skew (Note 6.)		60 25 500			60 25 500			60 25 500		ps
t_{JITTER}	Cycle-to-Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Voltage Swing (Differential) (Note 7.)	100	800	1200	100	800	1200	100	800	1200	mV
t_r t_f	Output Rise/Fall Times (20% – 80%) Q, \overline{Q}	330	600	900	330	600	900	330	650	900	ps

4. F_{max} guaranteed for functionality only. V_{OL} and V_{OH} levels are guaranteed at DC only.
5. Reference ($V_{CC} = 3.3V \pm 5\%$; GND = 0V)
6. Skews are measured between outputs under identical conditions.
7. 200mV input guarantees full logic swing at the output.

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