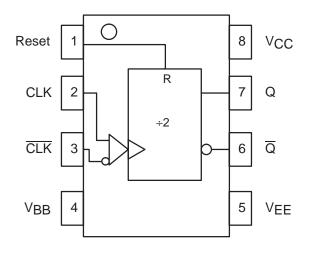
+2 Divider

The MC100LVEL32 is an integrated $\div 2$ divider. The differential clock inputs and the V_{BB} allow a differential, single-ended or AC coupled interface to the device. If used, the V_{BB} output should be bypassed to ground with a $0.01\mu F$ capacitor. Also note that the V_{BB} is designed to be used as an input bias on the LVEL32 only, the V_{BB} output has limited current sink and source capability. The LVEL32 is functionally identical to the EL32, but operates from a low voltage supply.

The reset pin is asynchronous and is asserted on the rising edge. Upon power-up, the internal flip-flop will attain a random state; the reset allows for the synchronization of multiple EL32's in a system.

- 510ps Propagation Delay
- 3.0GHz Toggle Frequency
- High Bandwidth Output Transitions
- 75kΩ Internal Input Pulldown Resistors
- >1000V ESD Protection

LOGIC DIAGRAM AND PINOUT ASSIGNMENT





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SO-8 D SUFFIX CASE 751

MARKING DIAGRAM

8 A A A A KVL32 ALYW

= Assembly Location

L = Wafer Lot Y = Year

W = Work Week

*For additional information, see Application Note AND8002/D

PIN DESCRIPTION

PIN	FUNCTION
CLK	Clock Inputs
Reset	Asynch Reset
V _{BB}	Ref Voltage Output
Q	Data Ouputs

ORDERING INFORMATION

Device	Package	Shipping				
MC100LVEL32D	SO-8	98 Units/Rail				
MC100LVEL32DR2	SO–8	2500 Tape & Reel				

DC CHARACTERISTICS ($V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = GND$)

		-40°C			0°C			25°C			85°C			
Symbol	Characteristic	Min	Тур	Max	Unit									
IEE	Power Supply Current		25			25			25			25		mA
VEE	Power Supply Voltage		-3.0		-3.0	-3.3	-3.8	-3.0	-3.3	-3.8	-3.0	-3.3	-3.8	V
V _{BB}	Output Reference Voltage	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	V
lіН	Input HIGH Current			150			150			150			150	μΑ

AC CHARACTERISTICS ($V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = GND$)

		-40°C			0°C			25°C			85°C			
Symbol	Characteristic	Min	Тур	Max	Unit									
f _{MAX}	Maximum Toggle Frequency		3.0			3.0			3.0			3.0		GHz
[†] PLH [†] PHL	Propagation Delay CLK to Q (Diff) CLK to Q (S.E.) Reset to Q	350 300 340	500 500 540	530 580 540	360 310 350	500 500 540	540 590 550	370 320 350	510 510 540	550 600 550	410 360 380	540 540 550	590 640 580	ps
VPP	Minimum Input Swing ¹	150			150			150			150			mV
t _r	Output Rise/Fall Times Q (20% – 80%)		225			225			225			225		ps

^{1.} Minimum input swing for which AC parameters are guaranteed.

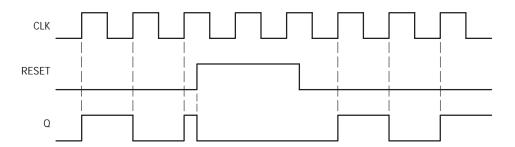
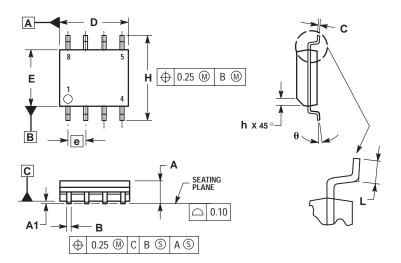


Figure 1. Timing Diagram

PACKAGE DIMENSIONS

SO-8 **D SUFFIX** PLASTIC SOIC PACKAGE CASE 751-06 ISSUE T



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. DIMENSIONS ARE IN MILLIMETER.
 3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
 5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS							
DIM	MIN	MAX						
Α	1.35	1.75						
A1	0.10	0.25						
В	0.35	0.49						
С	0.19	0.25						
D	4.80	5.00						
Ε	3.80	4.00						
е	1.27	BSC						
Н	5.80	6.20						
h	0.25	0.50						
L	0.40	1.25						
θ	0 °	7 °						

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