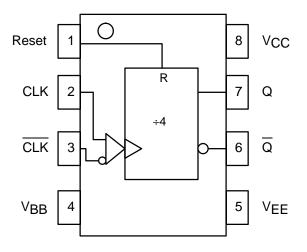
# +4 Divider

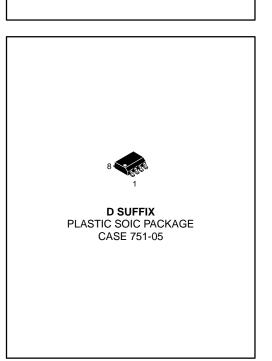
The MC100LVEL33 is an integrated +4 divider. The differential clock inputs and the V<sub>BB</sub> allow a differential, single-ended or AC coupled interface to the device. If used, the V<sub>BB</sub> output should be bypassed to ground with a 0.01µF capacitor. Also note that the V<sub>BB</sub> is designed to be used as an input bias on the EL33 only, the V<sub>BB</sub> output has limited current sink and source capability. The LVEL is functionally equivalent to the EL33 and works from a low voltage supply.

The reset pin is asynchronous and is asserted on the rising edge. Upon power-up, the internal flip-flops will attain a random state; the reset allows for the synchronization of multiple LVEL33's in a system.

- 630ps Propagation Delay
- 4.0GHz Toggle Frequency
- High Bandwidth Output Transitions
- Operates from -3.3V (or 3.3V) Supply
- 75kΩ Internal Input Pulldown Resistors
- >2000V ESD Protection

#### LOGIC DIAGRAM AND PINOUT ASSIGNMENT





MC100LVEL33

PIN	FUNCTION
CLK	Clock Inputs
Reset	Asynch Reset
VBB	Ref Voltage Output
Q	Data Ouputs



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### DC CHARACTERISTICS (VEE = VEE(min) to VEE(max); VCC = GND)

		-40°C			0°C			25°C			85°C			
Symbol	Characteristic	Min	Тур	Max	Unit									
IEE	Power Supply Current		33	37		33	37		33	37		35	39	mA
VEE	Power Supply Voltage	-3.0		-3.8	-3.0		-3.8	-3.0		-3.8	-3.0		-3.8	V
V <sub>BB</sub>	Output Reference Voltage	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	V
Iн	Input HIGH Current			150			150			150			150	μΑ
١L	Input LOW Current CLK Other	-600 0.5			-600 0.5			-600 0.5			-600 0.5			μA

## AC CHARACTERISTICS (VEE = VEE(min) to VEE(max); VCC = GND)

		–40°C			0°C			25°C			85°C			
Symbol	Characteristic	Min	Тур	Max	Unit									
fMAX	Maximum Toggle Frequency	3.4	4.2		3.8	4.2		3.8	4.2		3.8	4.2		GHz
<sup>t</sup> PLH <sup>t</sup> PHL	Propagation Delay CLK to Q (Diff) CLK to Q (SE) Reset to Q	510 460 500		690 740 700	530 480 510		710 760 710	540 490 520		720 770 720	600 550 580		780 830 780	ps
t <sub>rr</sub>	Reset Recovery	300			300			300			300			ps
<sup>t</sup> skew	Duty Cycle Skew <sup>2</sup>			20			20			20			20	ps
VPP	Minimum Input Swing <sup>1</sup>	150			150			150			150			mV
VCMR	Common Mode Range <sup>3</sup> Vpp < 500mV Vpp ≥ 500mV	-2.0 -1.8		-0.4 -0.4	-2.1 -1.9		-0.4 -0.4	-2.1 -1.9		-0.4 -0.4	-2.1 -1.9		-0.4 -0.4	V
t <sub>r</sub> t <sub>f</sub>	Output Rise/Fall Times Q (20% – 80%)	120		320	120		320	120		320	120		320	ps

Minimum input swing for which AC parameters are guaranteed.
Duty cycle skew is the difference between TPLH and TPLL.
The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between Vppmin and 1V. The lower end of the CMR range varies 1:1 with VEE. The numbers in the spec table assume a nominal VEE = -3.3V. Note for PECL operation, the V<sub>CMR</sub>(min) will be fixed at 3.3V - |V<sub>CMR</sub>(min)|.

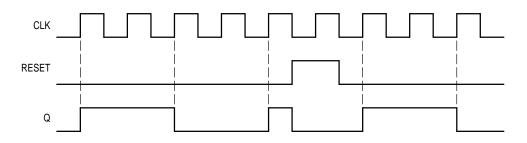
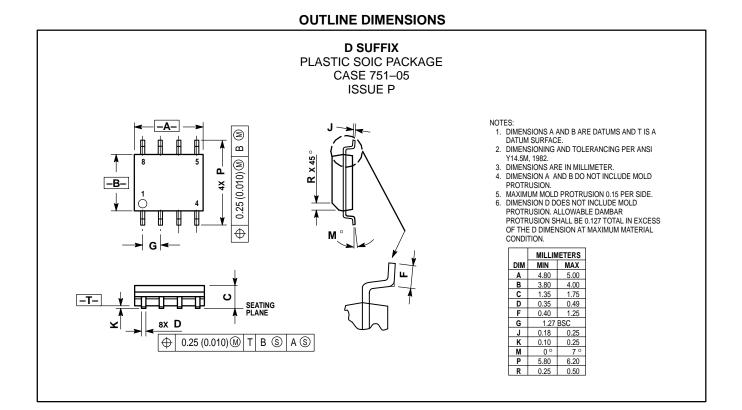


Figure 1. Timing Diagram



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