Differential Clock D Flip-Flop

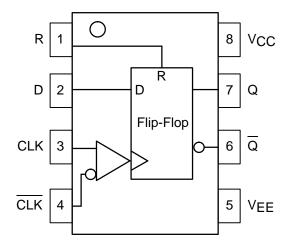
The MC10EL/100EL51 is a differential clock D flip-flop with reset. The device is functionally similar to the E151 device with higher performance capabilities. With propagation delays and output transition times significantly faster than the E151 the EL51 is ideally suited for those applications which require the ultimate in AC performance.

The reset input is an asynchronous, level triggered signal. Data enters the master portion of the flip-flop when the clock is LOW and is transferred to the slave, and thus the outputs, upon a positive transition of the clock. The differential clock inputs of the EL51 allow the device to be used as a negative edge triggered flip-flop.

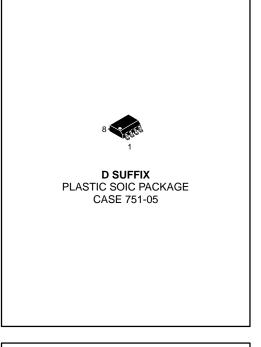
The differential input employs clamp circuitry to maintain stability under open input (pulled down to V_{EE}) conditions.

- 475ps Propagation Delay
- 2.8GHz Toggle Frequency
- 75kΩ Internal Input Pulldown Resistors
- >1000V ESD Protection

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



MC10EL51 MC100EL51



TRUTH TABLE								
	D	R	CLK	ď				
	L	L	Z	L				
	Н	L	Z	Н				
	х	Н	Х	L				
Z = LOW to HIGH Transition								

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DC CHARACTERISTICS (VEE = VEE(min) to VEE(max); VCC = GND)

			–40°C		0°C			25°C			85°C				
Symbol	nbol Characteristic		Min	Тур	Max	Unit									
IEE	Power Supply Current	10EL 100EL		24 24	29 29		24 24	29 29		24 24	29 29		24 30	29 36	mA
VEE	Power Supply Voltage	10EL 100EL	-4.75 -4.20	-5.2 -4.5	-5.5 -5.5	V									
lН	Input HIGH Current				150			150			150			150	μΑ

AC CHARACTERISTICS ($V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$; $V_{CC} = GND$)

		-40°C		0°C		25°C			85°C					
Symbol	Characteristic	Min	Тур	Max	Unit									
fMAX	Maximum Toggle Frequency	1.8	2.8		2.2	2.8		2.2	2.8		2.2	2.8		GHz
^t PLH ^t PHL	Propagation Delay to Output CLK	325 305	465 455	605 605	375 355	465 455	555 555	385 355	475 465	565 565	440 410	530 510	620 620	ps
ts	Setup Time	150	0		150	0		150	0		150	0		ps
tH	Hold Time	250	100		250	100		250	100		250	100		ps
^t RR	Reset Recovery	400	200		400	200		400	200		400	200		ps
tpW	Minimum Pulse Width CLK, Reset	400			400			400			400			ps
V _{PP}	Minimum Input Swing ¹	150			150			150			150			mV
VCMR	Common Mode Range ²	-0.4		See2	V									
t _r t _f	Output Rise/Fall Times Q (20% – 80%)	100	225	350	100	225	350	100	225	350	100	225	350	ps

 $^{1. \ \} Minimum \ input \ swing \ for \ which \ AC \ parameters \ are \ guaranteed.$

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The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within
the specified range and the peak-to-peak voltage lies between V_{PP}min and 1V. The lower end of the CMR range is dependent on V_{EE} and is
equal to V_{EE} + 2.5V.

OUTLINE DIMENSIONS

NOTES:

- DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14 5M 1982
- 3. DIMENSIONS ARE IN MILLIMETER.
- DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
- 5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
 6. DIMENSION D DOES NOT INCLUDE MOLD
- DIMENSION D DOES NOT INCLUDE MOLD
 PROTRUSION. ALLOWABLE DAMBAR
 PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS
 OF THE D DIMENSION AT MAXIMUM MATERIAL
 CONDITION.

	MILLIMETERS								
DIM	MIN	MAX							
Α	4.80	5.00							
В	3.80	4.00							
С	1.35	1.75							
D	0.35	0.49							
F	0.40	1.25							
G	1.27	1.27 BSC							
J	0.18	0.25							
K	0.10	0.25							
М	0 °	7 °							
Р	5.80	6.20							
R	0.25	0.50							

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