## Dual D Type Master-Slave Flip-Flop

The MC10H131 is a MECL 10H part which is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in clock speed and propagation delay and no increase in power–supply current.

- Propagation Delay, 1.0 ns Typical
- Power Dissipation, 235 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K–Compatible

#### MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply ( $V_{CC} = 0$ )	VEE	-8.0 to 0	Vdc
Input Voltage (V <sub>CC</sub> = 0)	VI	0 to V <sub>EE</sub>	Vdc
Output Current — Continuous — Surge	l <sub>out</sub>	50 100	mA
Operating Temperature Range	Т <sub>А</sub>	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T <sub>stg</sub>	–55 to +150 –55 to +165	°C ℃

### ELECTRICAL CHARACTERISTICS (V<sub>EE</sub> = -5.2 V ±5%) (See Note)

		<b>0</b> °		<b>25</b> °		<b>75</b> °		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	١ <sub>E</sub>	—	62	-	56		62	mA
Input Current High Pins 6, 11 Pin 9 Pins 7, 10 Pins 4, 5, 12, 13	linH		530 660 485 790		310 390 285 465		310 390 285 465	μΑ
Input Current Low	I <sub>inL</sub>	0.5		0.5	—	0.3		μΑ
High Output Voltage	VOH	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	VOL	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	VIH	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	VIL	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

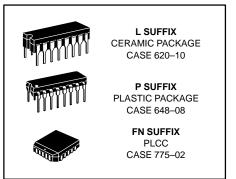
### AC PARAMETERS

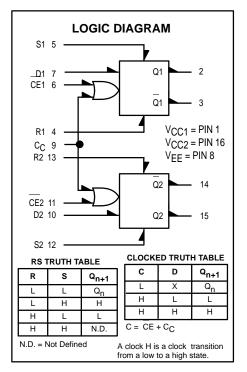
Propaga <u>tion</u> Delay Clock, CE Set, Reset	<sup>t</sup> pd	0.8 0.6	1.6 1.6	0.8 0.7	1.7 1.7	0.8 0.7	1.8 1.8	ns
Rise Time	t <sub>r</sub>	0.6	2.0	0.6	2.0	0.6	2.2	ns
Fall Time	t <sub>f</sub>	0.6	2.0	0.6	2.0	0.6	2.2	ns
Set–up Time	<sup>t</sup> set	0.7	-	0.7		0.7	-	ns
Hold Time	<sup>t</sup> hold	0.8		0.8	Ι	0.8		ns
Toggle Frequency	ftog	250	_	250	_	250	—	MHz

#### NOTE:

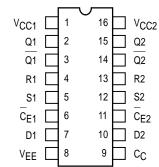
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts.

# MC10H131





#### DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package. For PLCC pin assignment, see the Pin Conversion Tables on page 6–11 of the Motorola MECL Data Book (DL122/D).



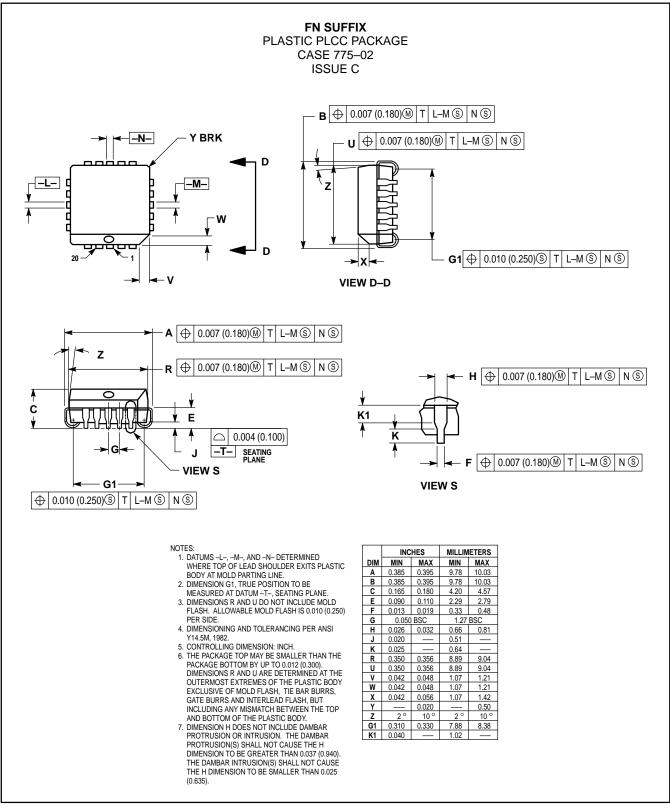
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### **APPLICATION INFORMATION**

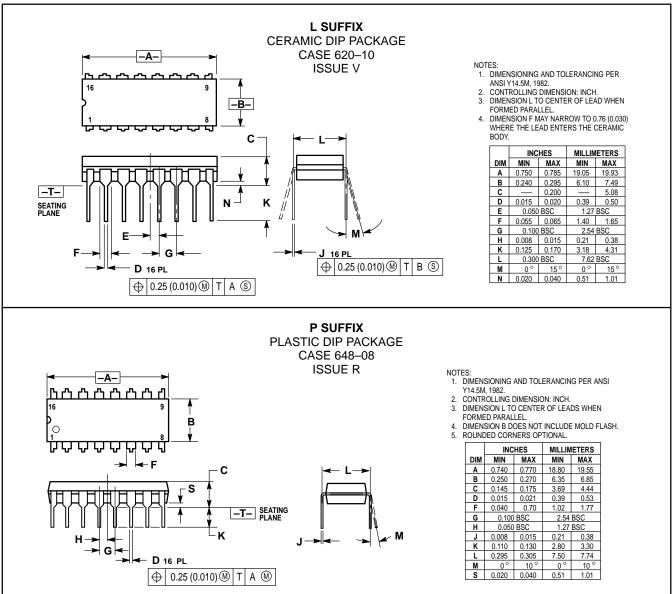
The MC10H131 is a dual master–slave type D flip–flop. Asynchronous Set (S) and Reset (R) override Clock (C<sub>C</sub>) and Clock Enable (CE) inputs. Each flip–flop may be clocked separately by holding the common clock in the new low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip–flop, the Clock Enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip-flop change on the positive transition of the clock. A change in the information present at the data (D) input will not affect the output information at any other time due to master slave construction.

### **OUTLINE DIMENSIONS**



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