# **Dual 4-5-Input OR/NOR Gate**

The MC10H109 is a dual 4–5–input OR/NOR gate. This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power–supply current.

- Propagation Delay, 1.0 ns Typical
- Power Dissipation 35 mW/Gate Typical (same as MECL 10K)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

#### **MAXIMUM RATINGS**

Characteristic	Symbol	Rating	Unit
Power Supply (V <sub>CC</sub> = 0)	VEE	-8.0 to 0	Vdc
Input Voltage (V <sub>CC</sub> = 0)	VI	0 to V <sub>EE</sub>	Vdc
Output Current — Continuous — Surge	l <sub>out</sub>	50 100	mA
Operating Temperature Range	T <sub>A</sub>	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T <sub>stg</sub>	-55 to +150 -55 to +165	ပို့

# ELECTRICAL CHARACTERISTICS (VEE = -5.2 V ±5%) (See Note)

		<b>0</b> °		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	ΙΕ	_	15		14	1	15	mA
Input Current High	l <sub>inH</sub>	_	425	_	265	-	265	μΑ
Input Current Low	l <sub>inL</sub>	0.5	1	0.5	_	0.3	_	μΑ
High Output Voltage	Vон	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	VOL	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	VIH	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	V <sub>IL</sub>	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

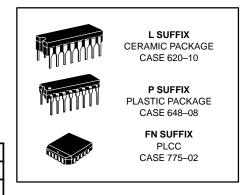
## **AC PARAMETERS**

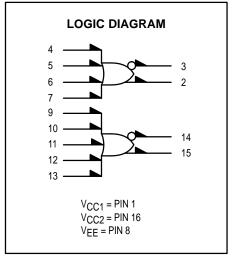
Propagation Delay	<sup>t</sup> pd	0.4	1.3	0.4	1.3	0.45	1.45	ns
Rise Time	t <sub>r</sub>	0.5	2.0	0.5	2.1	0.5	2.2	ns
Fall Time	t <sub>f</sub>	0.5	2.0	0.5	2.1	0.5	2.2	ns

## NOTE:

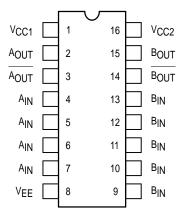
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts.

# MC10H109



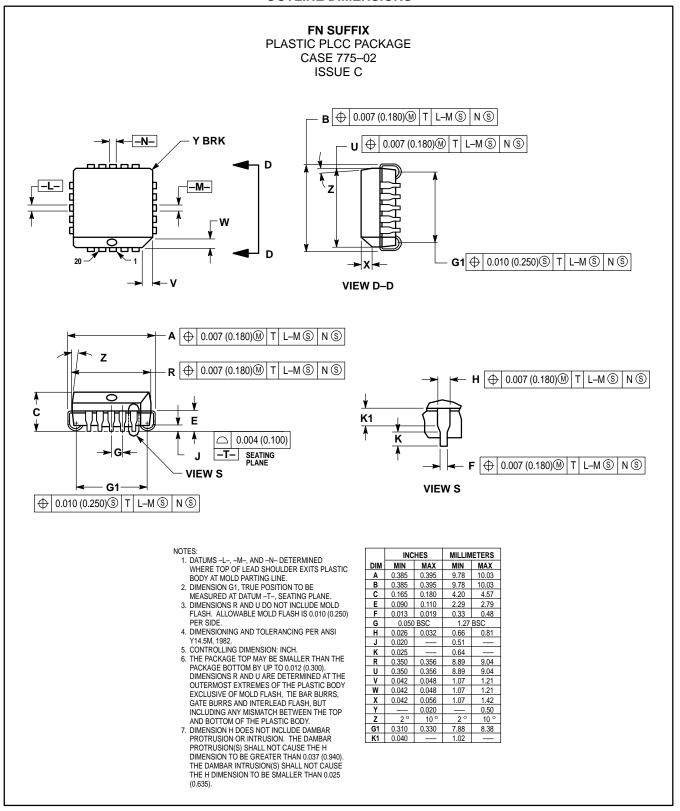


# DIP PIN ASSIGNMENT

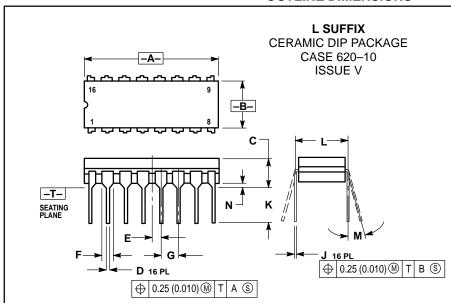


Pin assignment is for Dual-in-Line Package.
For PLCC pin assignment, see the Pin Conversion
Tables on page 6–11 of the Motorola MECL Data
Book (DL122/D).

## **OUTLINE DIMENSIONS**



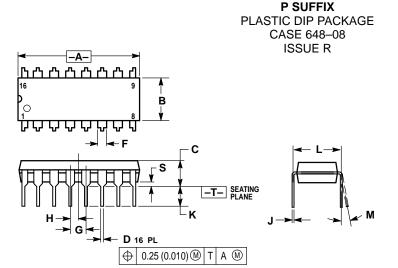
#### **OUTLINE DIMENSIONS**



#### NOTES:

- DIMENSIONING AND TOLERANCING PER
- ANSI Y14.5M, 1982. CONTROLLING DIMENSION: INCH.
- DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
- DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC

	INC	HES	MILLIMETERS		
DIM	MIN	MAX	MIN	MAX	
Α	0.750	0.785	19.05	19.93	
В	0.240	0.295	6.10	7.49	
С		0.200		5.08	
D	0.015	0.020	0.39	0.50	
Е	0.050	BSC	1.27 BSC		
F	0.055	0.065	1.40	1.65	
G	0.100 BSC		2.54 BSC		
Н	0.008	0.015	0.21	0.38	
K	0.125	0.170	3.18	4.31	
L	0.300	BSC	7.62 BSC		
M	0°	15°	0 °	15°	
N	0.020	0.040	0.51	1.01	



- NOTES:
  1. DIMENSIONING AND TOLERANCING PER ANSI
- Y14.5M, 1982. CONTROLLING DIMENSION: INCH.
- DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
- DIMENSION B DOES NOT INCLUDE MOLD FLASH.
- ROUNDED CORNERS OPTIONAL

	INC	HES	MILLIMETERS			
DIM	MIN	MAX	MIN	MAX		
Α	0.740	0.770	18.80	19.55		
В	0.250	0.270	6.35	6.85		
С	0.145	0.175	3.69	4.44		
D	0.015	0.021	0.39	0.53		
F	0.040	0.70	1.02	1.77		
G	0.100 BSC		2.54 BSC			
Н	0.050	0.050 BSC		1.27 BSC		
J	0.008	0.015	0.21	0.38		
K	0.110	0.130	2.80	3.30		
L	0.295	0.305	7.50	7.74		
M	0°	10 °	0°	10 °		
S	0.020	0.040	0.51	1.01		

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#### How to reach us:

USA/EUROPE/Locations Not Listed: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036. 1-800-441-2447 or 602-303-5454

MFAX: RMFAX0@email.sps.mot.com - TOUCHTONE 602-244-6609 INTERNET: http://Design-NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, 6F Seibu-Butsuryu-Center, 3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 03-81-3521-8315

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298



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