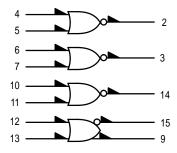
Quad 2-Input NOR Gate

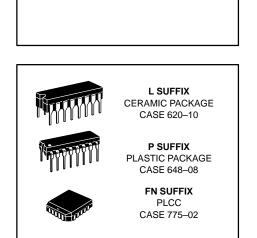
The MC10102 is a quad 2–input NOR gate. The MC10102 provides one gate with OR/NOR outputs.

 $\label{eq:pd} \begin{array}{l} \mathsf{P}_D = 25 \text{ mW typ/gate (No Load)} \\ \mathsf{t}_{pd} = 2.0 \text{ ns typ} \\ \mathsf{t}_{f}, \, \mathsf{t}_{f} = 2.0 \text{ ns typ } (20\%\text{--}80\%) \end{array}$

LOGIC DIAGRAM







MC10102

DIP PIN ASSIGNMENT

VCC1	1	16	VCC2
AOUT	2	15	DOUT
BOUT	3	14	COUT
A _{IN}	4	13	D _{IN}
A _{IN}	5	12	D _{IN}
B _{IN}	6	11	C _{IN}
B _{IN}	7	10	C _{IN}
V_{EE}	8	9	D _{OUT}

Pin assignment is for Dual–in–Line Package. For PLCC pin assignment, see the Pin Conversion Tables on page 6–11 of the Motorola MECL Data Book (DL122/D).



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ELECTRICAL CHARACTERISTICS

				Test Limits							
Characteristic		Symbol	Pin Under Test	–30°C		+25°C			+85°C		1
				Min	Max	Min	Тур	Max	Min	Max	Unit
Power Supply Drain Current		١E	8		29		20	26		29	mAdc
Input Current		l _{inH}	12		425			265		265	μAdc
		l _{inL}	12	0.5		0.5			0.3		μAdc
Output Voltage	Logic 1	VOH	9 9 15 15	-1.060 -1.060 -1.060 -1.060	-0.890 -0.890 -0.890 -0.890	-0.960 -0.960 -0.960 -0.960		-0.810 -0.810 -0.810 -0.810	-0.890 -0.890 -0.890 -0.890	-0.700 -0.700 -0.700 -0.700	Vdc
Output Voltage	Logic 0	VOL	9 9 15 15	-1.890 -1.890 -1.890 -1.890	-1.675 -1.675 -1.675 -1.675	-1.850 -1.850 -1.850 -1.850		-1.650 -1.650 -1.650 -1.650	-1.825 -1.825 -1.825 -1.825	-1.615 -1.615 -1.615 -1.615	Vdc
Threshold Volta	age Logic 1	Voha	9 9 15 15	-1.080 -1.080 -1.080 -1.080		-0.980 -0.980 -0.980 -0.980			-0.910 -0.910 -0.910 -0.910		Vdc
Threshold Volta	age Logic 0	V _{OLA}	9 9 15 15		-1.655 -1.655 -1.655 -1.655			-1.630 -1.630 -1.630 -1.630		-1.595 -1.595 -1.595 -1.595	Vdc
Switching Time	es (50Ω Load)										ns
Propagation De	elay	^t 12+15– ^t 12–15+ ^t 12+9+ ^t 12–9–	15 15 9 9	1.0 1.0 1.0 1.0	3.1 3.1 3.1 3.1	1.0 1.0 1.0 1.0	2.0 2.0 2.0 2.0	2.9 2.9 2.9 2.9	1.0 1.0 1.0 1.0	3.3 3.3 3.3 3.3	
Rise Time	(20 to 80%)	^t 15+ t9+	15 9	1.1 1.1	3.6 3.6	1.1 1.1	2.0 2.0	3.3 3.3	1.1 1.1	3.7 3.7	
Fall Time	(20 to 80%)	t ₁₅₋ t ₉₋	15 9	1.1 1.1	3.6 3.6	1.1 1.1	2.0 2.0	3.3 3.3	1.1 1.1	3.7 3.7	

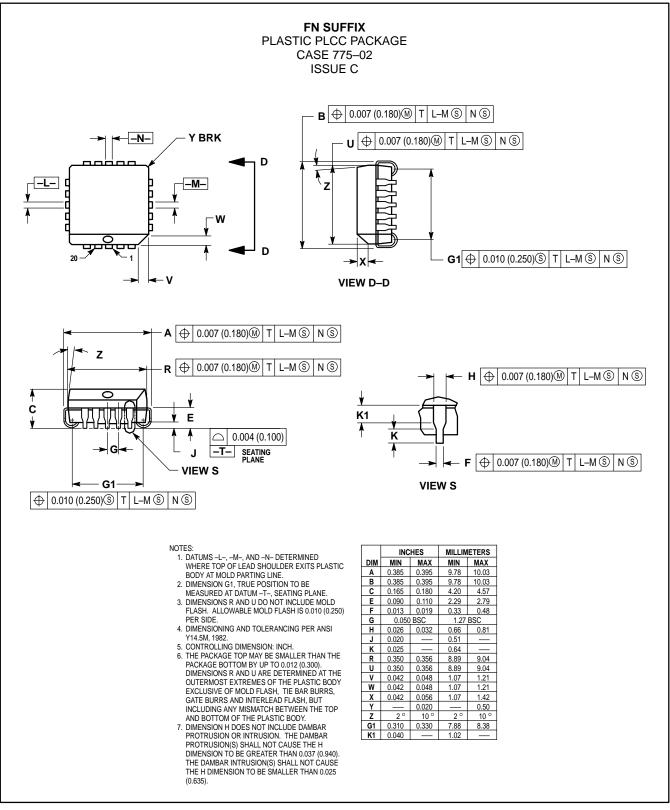
ELECTRICAL CHARACTERISTICS (continued)

				TEST VOLTAGE VALUES (Volts)					
		@ Test Temperature		VIHmax	VILmin	VIHAmin	VILAmax	VEE	
			–30°C	-0.890	-1.890	-1.205	-1.500	-5.2	
			+25°C	-0.810	-1.850	-1.105	-1.475	-5.2	1
			+85°C	-0.700	-1.825	-1.035	-1.440	-5.2	
			Pin	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					
Characteristic		Symbol	Under Test	V _{IHmax}	V _{ILmin}	V _{IHAmin}	V _{ILAmax}	VEE	(V _{CC}) Gnd
Power Supply Drain Cu	urrent	١E	8					8	1, 16
Input Current		l _{inH}	12	12				8	1, 16
		l _{inL}	12		12			8	1, 16
Output Voltage	Logic 1	VOH	9 9 15 15	12 13				8 8 8 8	1, 16 1, 16 1, 16 1, 16 1, 16
Output Voltage	Logic 0	V _{OL}	9 9 15 15	12 13				8 8 8 8	1, 16 1, 16 1, 16 1, 16 1, 16
Threshold Voltage	Logic 1	Voha	9 9 15 15			12 13	12 13	8 8 8 8	1, 16 1, 16 1, 16 1, 16 1, 16
Threshold Voltage	Logic 0	VOLA	9 9 15 15			12 13	12 13	8 8 8 8	1, 16 1, 16 1, 16 1, 16 1, 16
Switching Times	(50 Ω Load)					Pulse In	Pulse Out	–3.2 V	+2.0 V
Propagation Delay		^t 12+15– ^t 12–15+ ^t 12+9+ ^t 12–9–	15 15 9 9			12 12 12 12 12	15 15 9 9	8 8 8 8	1, 16 1, 16 1, 16 1, 16 1, 16
Rise Time	(20 to 80%)	^t 15+ ^t 9+	15 9			12 12	15 9	8 8	1, 16 1, 16
Fall Time	(20 to 80%)	t _{15–} t9–	15 9			12 12	15 9	8 8	1, 16 1, 16

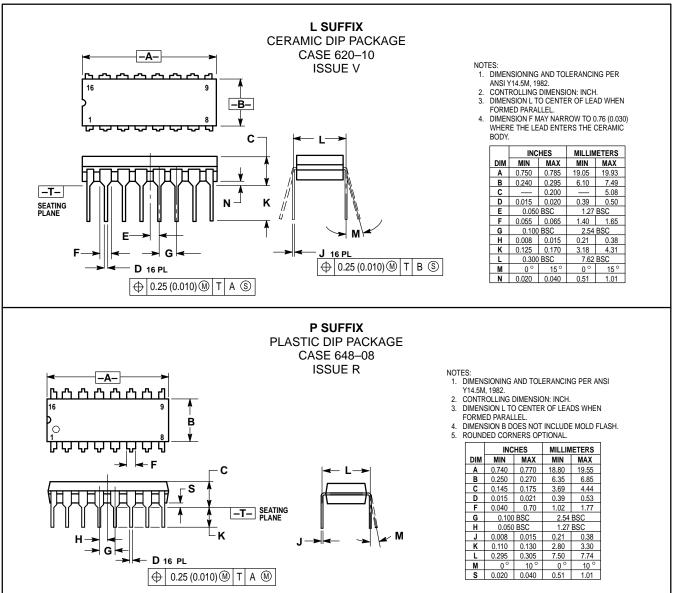
Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

MC10102

OUTLINE DIMENSIONS



OUTLINE DIMENSIONS



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