

# Binary to 1-8 Decoder (Low)

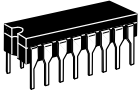
The MC10161 is designed to decode a three bit input word to a one of eight line output. The selected output will be low while all other outputs will be high. The enable inputs, when either or both are high, force all outputs high.

The MC10161 is a true parallel decoder. No series gating is used internally, eliminating unequal delay times found in other decoders. This design provides the identical 4 ns delay from any address or enable input to any output.

A complete mux/demux operation on 16 bits for data distribution is illustrated in Figure 1. This system, using the MC10136 control counters, has the capability of incrementing, decrementing or holding data channels. When both S0 and S1 are low, the index counters reset, thus initializing both the mux and demux units. The four binary outputs of the counter are buffered by the MC10101s to send twisted-pair select data to the multiplexer/demultiplexer to units.

$P_D = 315 \text{ mW typ/pkg (No Load)}$   
 $t_{pd} = 4.0 \text{ ns typ}$   
 $t_r, t_f = 2.0 \text{ ns typ (20\%--80\%)}$

## MC10161



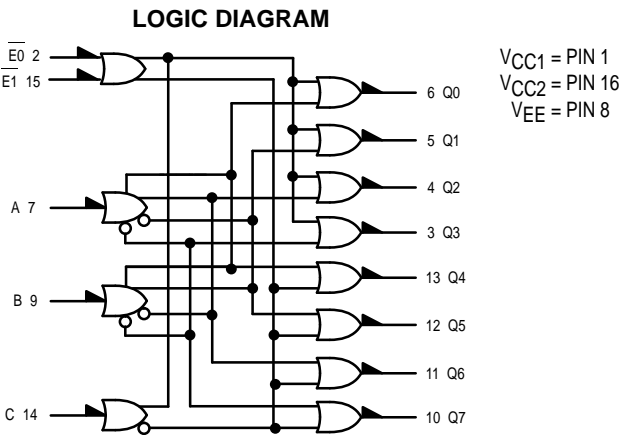
**L SUFFIX**  
CERAMIC PACKAGE  
CASE 620-10



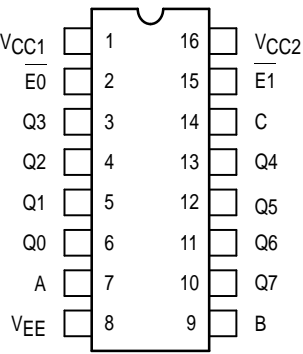
**P SUFFIX**  
PLASTIC PACKAGE  
CASE 648-08



**FN SUFFIX**  
PLCC  
CASE 775-02



### DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-Line Package.  
For PLCC pin assignment, see the Pin Conversion  
Tables on page 6-11 of the Motorola MECL Data  
Book (DL122/D).

### TRUTH TABLE

ENABLE INPUTS		INPUTS			OUTPUTS							
E1	E0	C	B	A	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
L	L	L	L	L	L	H	H	H	H	H	H	H
L	L	L	L	H	H	L	H	H	H	H	H	H
L	L	L	L	H	H	H	L	H	H	H	H	H
L	L	L	H	H	H	H	H	L	H	H	H	H
L	L	L	H	L	H	H	H	H	L	H	H	H
L	L	L	H	L	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	L	H
L	L	L	H	H	H	H	H	H	H	H	H	L
H	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	H	H	H	H	H	H	H	H



## ELECTRICAL CHARACTERISTICS

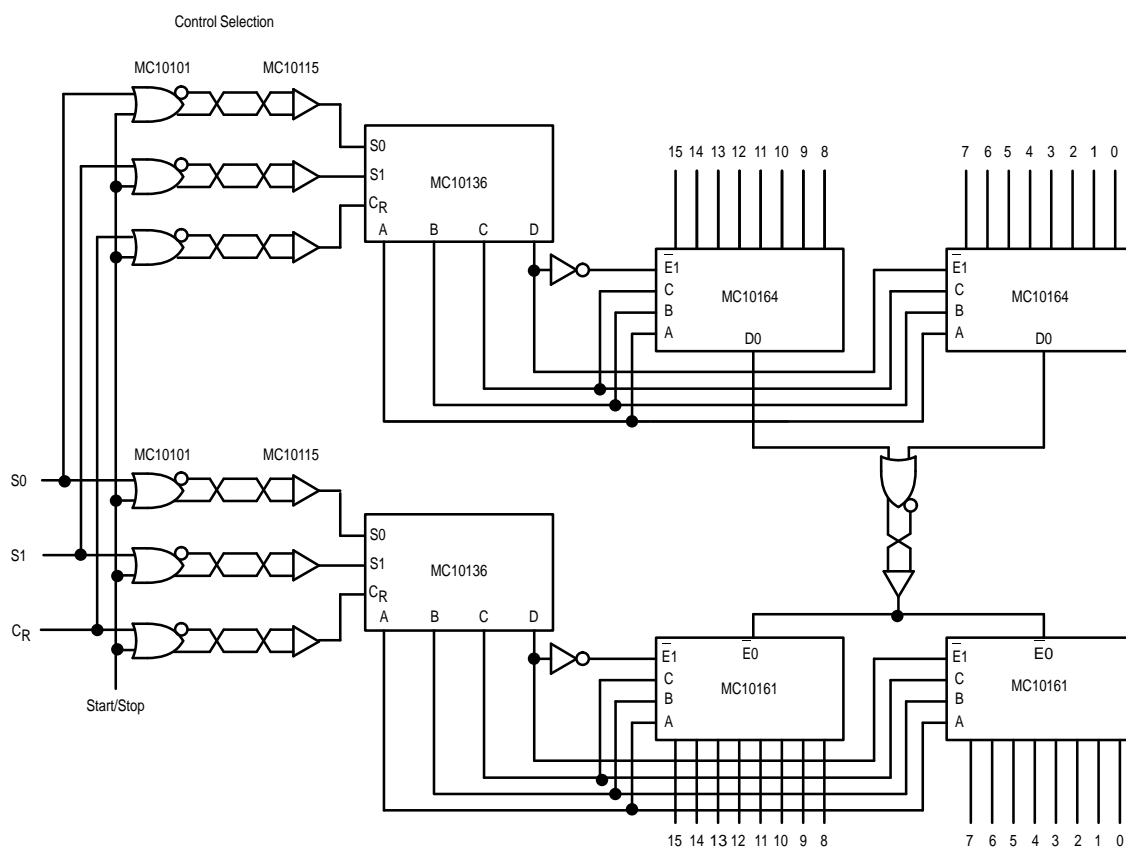
Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			−30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I <sub>E</sub>	8		84		61	76		84	mAdc
Input Current	I <sub>inH</sub>	14		350			220		220	μAdc
	I <sub>inL</sub>	14	0.5		0.5			0.3		μAdc
Output Voltage      Logic 1	V <sub>OH</sub>	13	−1.060	−0.890	−0.960		−0.810	−0.890	−0.700	Vdc
		13	−1.060	−0.890	−0.960		−0.810	−0.890	−0.700	
Output Voltage      Logic 0	V <sub>OL</sub>	13	−1.890	−1.675	−1.850		−1.650	−1.825	−1.615	Vdc
Threshold Voltage      Logic 1	V <sub>OHA</sub>	13	−1.080		−0.980			−0.910		Vdc
		13	−1.080		−0.980			−0.910		
Threshold Voltage      Logic 0	V <sub>OLA</sub>	13		−1.655			−1.630		−1.595	Vdc
Switching Times    (50Ω Load)										ns
Propagation Delay	t <sub>14+13−</sub>	13	1.5	6.2	1.5	4.0	6.0	1.5	6.4	
	t <sub>14−13+</sub>	13	1.5	6.2	1.5	4.0	6.0	1.5	6.4	
Rise Time            (20 to 80%)	t <sub>13+</sub>	13	1.0	3.3	1.1	2.0	3.3	1.1	3.5	
Fall Time            (20 to 80%)	t <sub>13−</sub>	13	1.0	3.3	1.1	2.0	3.3	1.1	3.5	

## ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature			TEST VOLTAGE VALUES (Volts)					(V <sub>CC</sub> ) Gnd
			$V_{IHmax}$	$V_{ILmin}$	$V_{IHmin}$	$V_{ILmax}$	$V_{EE}$	
			-30°C	-30°C	-30°C	-30°C	-30°C	
			+25°C	+25°C	+25°C	+25°C	+25°C	
			+85°C	+85°C	+85°C	+85°C	+85°C	
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V <sub>CC</sub> ) Gnd
			$V_{IHmax}$	$V_{ILmin}$	$V_{IHmin}$	$V_{ILmax}$	$V_{EE}$	
Power Supply Drain Current	$I_E$	8	2,7,9,14,15				8	1,16
Input Current	$I_{inH}$	14	14				8	1,16
	$I_{inL}$	14		14			8	1,16
Output Voltage Logic 1	$V_{OH}$	13	2				8	1,16
		13	15				8	1,16
Output Voltage Logic 0	$V_{OL}$	13	14				8	1,16
Threshold Voltage Logic 1	$V_{OHA}$	13			2		8	1,16
		13			15		8	1,16
Threshold Voltage Logic 0	$V_{OLA}$	13			14		8	1,16
Switching Times (50 $\Omega$ Load)					Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	$t_{14+13-}$	13			14	13	8	1,16
	$t_{14-13+}$	13			14	13	8	1,16
Rise Time (20 to 80%)	$t_{13+}$	13			14	13	8	1,16
Fall Time (20 to 80%)	$t_{13-}$	13			14	13	8	1,16

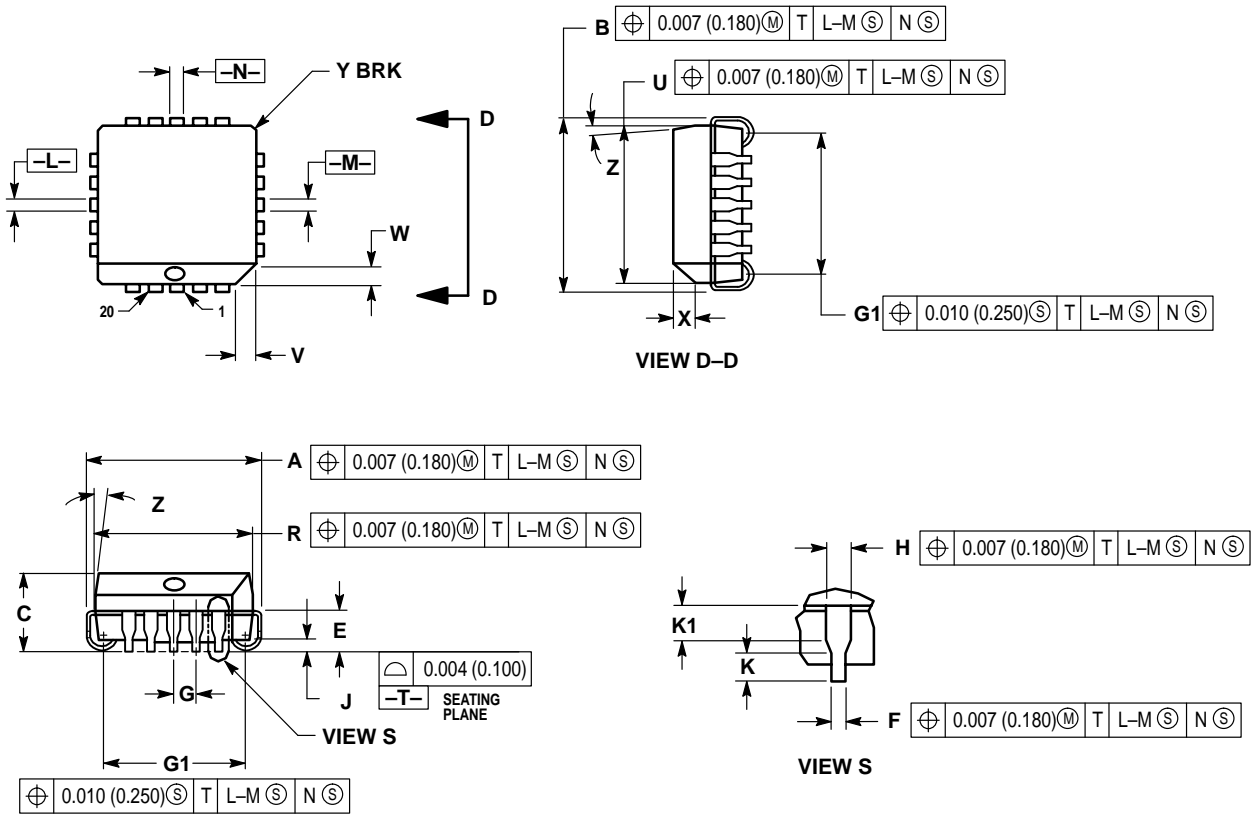
Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

FIGURE 1 — HIGH SPEED 16-BIT MULTIPLEXER/DEMULTIPLEXER



OUTLINE DIMENSIONS

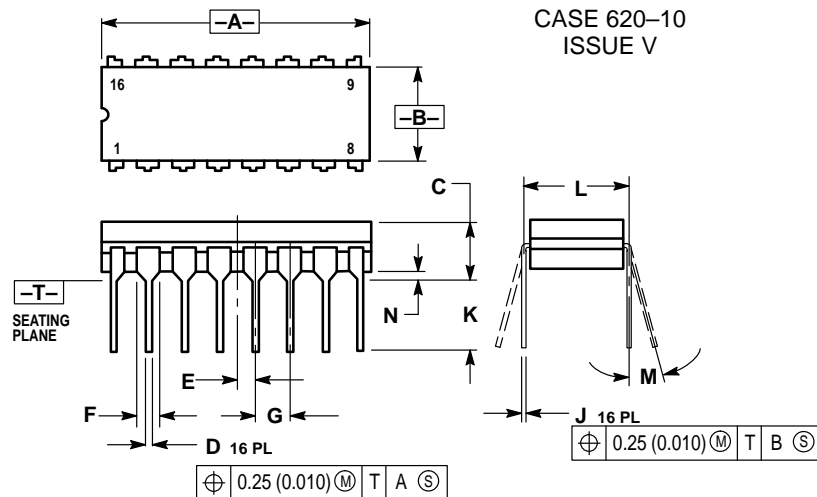
FN SUFFIX  
PLASTIC PLCC PACKAGE  
CASE 775-02  
ISSUE C



- NOTES:
- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
  - DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
  - DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
  - DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  - CONTROLLING DIMENSION: INCH.
  - THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
  - DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2 °	10 °	2 °	10 °
G1	0.310	0.330	7.88	8.38
K1	0.040	—	1.02	—

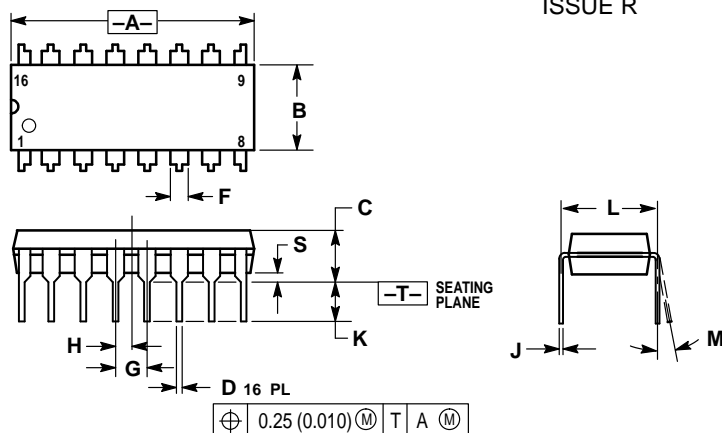
## OUTLINE DIMENSIONS

**L SUFFIX**  
**CERAMIC DIP PACKAGE**  
**CASE 620-10**  
**ISSUE V**


## NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

**P SUFFIX**  
**PLASTIC DIP PACKAGE**  
**CASE 648-08**  
**ISSUE R**


## NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

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