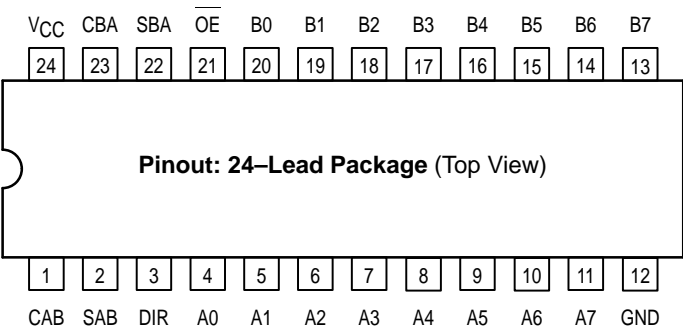


Low-Voltage CMOS Octal
Transceiver/Registered
Transceiver
With 5V-Tolerant Inputs and Outputs
(3-State, Non-Inverting)

The MC74LCX646 is a high performance, non-inverting octal transceiver/registered transceiver operating from a 2.7 to 3.6V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5V allows MC74LCX646 inputs to be safely driven from 5V devices. The MC74LCX646 is suitable for memory address driving and all TTL level bus oriented transceiver applications.

Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes from a LOW-to-HIGH logic level. Output Enable (OE) and DIR pins are provided to control the transceiver outputs. In the transceiver mode, data present at the high impedance port may be stored in either the A or the B register or in both. The select controls (SBA, SAB) can multiplex stored and real-time (transparent mode) data. The direction control (DIR) determines which bus will receive data when the enable OE is active LOW. In the isolation mode (OE HIGH), A data may be stored in the B register or B data may be stored in the A register. Only one of the two buses, A or B, may be driven at one time.

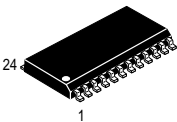
- Designed for 2.7 to 3.6V V_{CC} Operation
- 5V Tolerant — Interface Capability With 5V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When $V_{CC} = 0V$
- LVTTTL Compatible
- LVC MOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10 μ A) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V



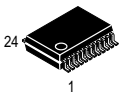
MC74LCX646

LCX

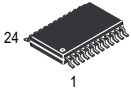
LOW-VOLTAGE CMOS
OCTAL TRANSCEIVER/
REGISTERED TRANSCEIVER



DW SUFFIX
PLASTIC SOIC
CASE 751E-04



SD SUFFIX
PLASTIC SSOP
CASE 940D-03



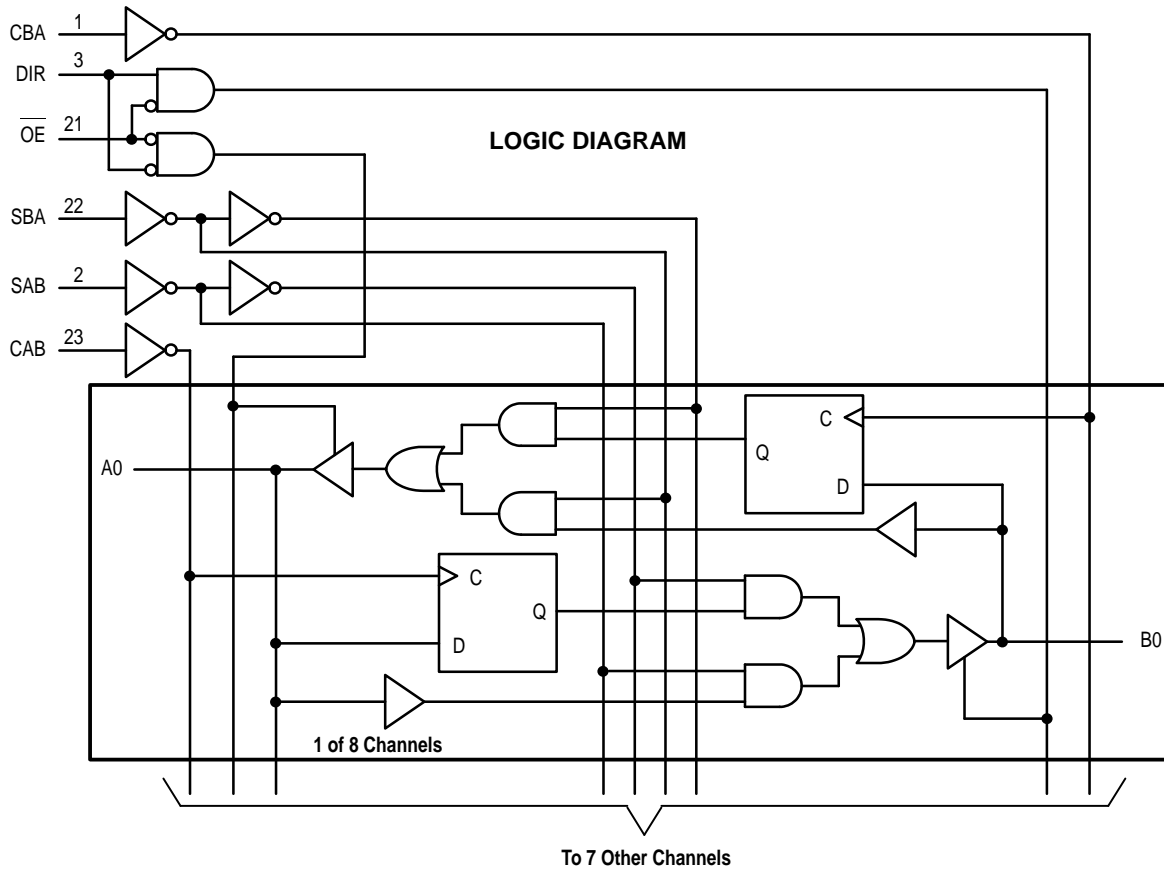
DT SUFFIX
PLASTIC TSSOP
CASE 948H-01

PIN NAMES

Pins	Function
A0–A7	Side A Inputs/Outputs
B0–B7	Side B Inputs/Outputs
CAB, CBA	Clock Pulse Inputs
SAB, SBA	Select Control Inputs
DIR, OE	Output Enable Inputs



MC74LCX646



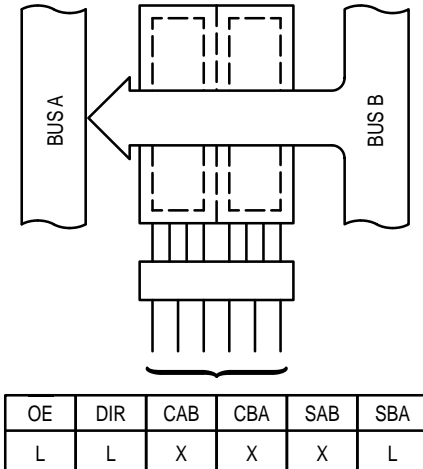
FUNCTION TABLE

Inputs						Data Ports		Operating Mode
OE	DIR	CAB	CBA	SAB	SBA	An	Bn	
H	X					Input	Input	
		↑	↑	X	X	X	X	Isolation, Hold Storage
		↑	↑	X	X	l h X X	X X l h	Store A and/or B Data
L	H					Input	Output	
		↑	X*	L	X	L H	L H	Real Time A Data to B Bus
				H	X	X	QA	Stored A Data to B Bus
		↑	X*	L	X	l h	L H	Real Time A Data to B Bus; Store A Data
				H	X	L H	QA QA	Clock A Data to B Bus; Store A Data
L	L					Output	Input	
		X*	↑	X	L	L H	L H	Real Time B Data to A Bus
				X	H	QB	X	Stored B Data to A Bus
		X*	↑	X	L	L H	l h	Real Time B Data to A Bus; Store B Data
				X	H	QB QB	L H	Clock B Data to A Bus; Store B Data

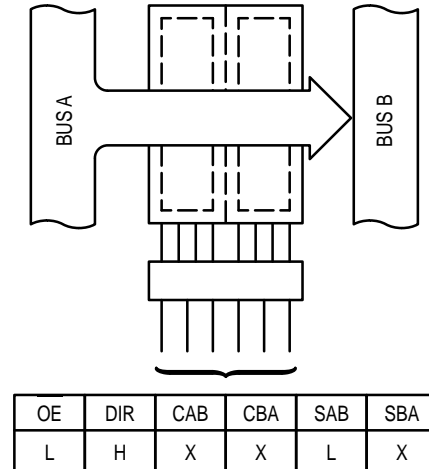
H = High Voltage Level; h = High Voltage Level One Setup Time Prior to the Low-to-High Clock Transition; L = Low Voltage Level; l = Low Voltage Level One Setup Time Prior to the Low-to-High Clock Transition; X = Don't Care; ↑ = Low-to-High Clock Transition; ↓ = NOT Low-to-High Clock Transition; QA = A input storage register; QB = B input storage register; * = The clocks are not internally gated with either the Output Enables or the Source Inputs. Therefore, data at the A or B ports may be clocked into the storage registers, at any time. For I_{CC} reasons, Do Not Float Inputs.

BUS APPLICATIONS

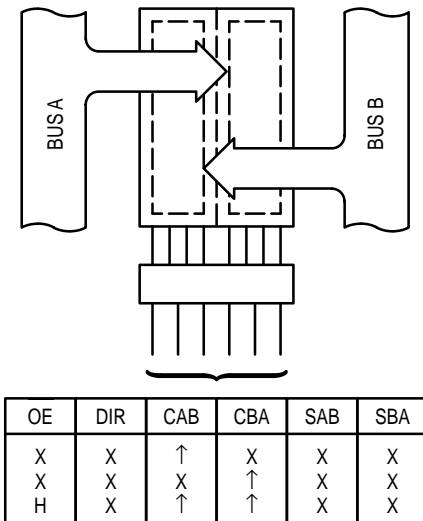
Real Time Transfer – Bus B to Bus A



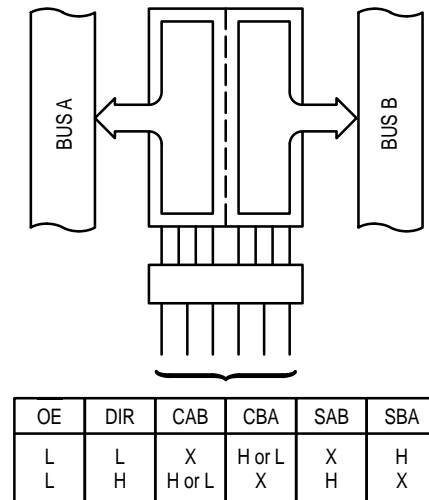
Real Time Transfer – Bus A to Bus B



Store Data from Bus A, Bus B or Busses A and B



Transfer Storage Data to Bus A or Bus B



ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	-0.5 to $+7.0$		V
V_I	DC Input Voltage	$-0.5 \leq V_I \leq +7.0$		V
V_O	DC Output Voltage	$-0.5 \leq V_O \leq +7.0$	Output in 3-State	V
		$-0.5 \leq V_O \leq V_{CC} + 0.5$	Note 1.	V
I_{IK}	DC Input Diode Current	-50	$V_I < \text{GND}$	mA
I_{OK}	DC Output Diode Current	-50	$V_O < \text{GND}$	mA
		$+50$	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	± 50		mA
I_{CC}	DC Supply Current Per Supply Pin	± 100		mA
I_{GND}	DC Ground Current Per Ground Pin	± 100		mA
T_{STG}	Storage Temperature Range	-65 to $+150$		$^{\circ}\text{C}$

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

1. Output in HIGH or LOW State. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	2.0	3.3	3.6	V
	Operating Data Retention Only	1.5	3.3	3.6	
V_I	Input Voltage	0		5.5	V
V_O	Output Voltage (HIGH or LOW State) (3-State)	0		V_{CC}	V
		0		5.5	
I_{OH}	HIGH Level Output Current, $V_{CC} = 3.0\text{V} - 3.6\text{V}$			-24	mA
I_{OL}	LOW Level Output Current, $V_{CC} = 3.0\text{V} - 3.6\text{V}$			24	mA
I_{OH}	HIGH Level Output Current, $V_{CC} = 2.7\text{V} - 3.0\text{V}$			-12	mA
I_{OL}	LOW Level Output Current, $V_{CC} = 2.7\text{V} - 3.0\text{V}$			12	mA
T_A	Operating Free-Air Temperature	-40		$+85$	$^{\circ}\text{C}$
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8V to 2.0V, $V_{CC} = 3.0\text{V}$	0		10	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$		Unit
			Min	Max	
V_{IH}	HIGH Level Input Voltage (Note 2.)	$2.7\text{V} \leq V_{CC} \leq 3.6\text{V}$	2.0		V
V_{IL}	LOW Level Input Voltage (Note 2.)	$2.7\text{V} \leq V_{CC} \leq 3.6\text{V}$		0.8	V
V_{OH}	HIGH Level Output Voltage	$2.7\text{V} \leq V_{CC} \leq 3.6\text{V}; I_{OH} = -100\mu\text{A}$	$V_{CC} - 0.2$		V
		$V_{CC} = 2.7\text{V}; I_{OH} = -12\text{mA}$	2.2		
		$V_{CC} = 3.0\text{V}; I_{OH} = -18\text{mA}$	2.4		
		$V_{CC} = 3.0\text{V}; I_{OH} = -24\text{mA}$	2.2		
V_{OL}	LOW Level Output Voltage	$2.7\text{V} \leq V_{CC} \leq 3.6\text{V}; I_{OL} = 100\mu\text{A}$		0.2	V
		$V_{CC} = 2.7\text{V}; I_{OL} = 12\text{mA}$		0.4	
		$V_{CC} = 3.0\text{V}; I_{OL} = 16\text{mA}$		0.4	
		$V_{CC} = 3.0\text{V}; I_{OL} = 24\text{mA}$		0.55	

2. These values of V_I are used to test DC electrical characteristics only.

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Characteristic	Condition	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$		Unit
			Min	Max	
I_I	Input Leakage Current	$2.7\text{V} \leq V_{CC} \leq 3.6\text{V}; 0\text{V} \leq V_I \leq 5.5\text{V}$		± 5.0	μA
I_{OZ}	3-State Output Current	$2.7 \leq V_{CC} \leq 3.6\text{V}; 0\text{V} \leq V_O \leq 5.5\text{V}; V_I = V_{IH} \text{ or } V_{IL}$		± 5.0	μA
I_{OFF}	Power-Off Leakage Current	$V_{CC} = 0\text{V}; V_I \text{ or } V_O = 5.5\text{V}$		10	μA
I_{CC}	Quiescent Supply Current	$2.7 \leq V_{CC} \leq 3.6\text{V}; V_I = \text{GND or } V_{CC}$		10	μA
		$2.7 \leq V_{CC} \leq 3.6\text{V}; 3.6 \leq V_I \text{ or } V_O \leq 5.5\text{V}$		± 10	μA
ΔI_{CC}	Increase in I_{CC} per Input	$2.7 \leq V_{CC} \leq 3.6\text{V}; V_{IH} = V_{CC} - 0.6\text{V}$		500	μA

AC CHARACTERISTICS ($t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 500\Omega$)

Symbol	Parameter	Waveform	Limits				Unit	
			T _A = −40°C to +85°C					
			V _{CC} = 3.0V to 3.6V		V _{CC} = 2.7V			
			Min	Max	Min	Max		
f _{max}	Clock Pulse Frequency	3	150					MHz
t _{PLH} t _{PHL}	Propagation Delay Input to Output	1	1.5 1.5	7.0 7.0	1.5 1.5	8.0 8.0		ns
t _{PLH} t _{PHL}	Propagation Delay Clock to Output	3	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5		ns
t _{PLH} t _{PHL}	Propagation Delay Select to Output	1	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5		ns
t _{PZH} t _{PZL}	Output Enable Time to High and Low Level	2	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5		ns
t _{PHZ} t _{PLZ}	Output Disable Time From High and Low Level	2	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5		ns
t _S	Setup Time, HIGH or LOW Data to Clock	3	2.5		2.5			ns
t _H	Hold Time, HIGH or LOW Data to Clock	3	1.5		1.5			ns
t _W	Clock Pulse Width, HIGH or LOW	3	3.3		3.3			ns
t _{OSHL} t _{OSLH}	Output-to-Output Skew (Note 3.)			1.0 1.0				ns

3. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

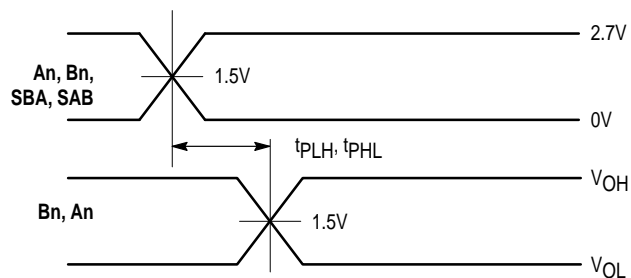
DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	$T_A = +25^{\circ}\text{C}$			Unit
			Min	Typ	Max	
V_{OLP}	Dynamic LOW Peak Voltage (Note 4.)	$V_{CC} = 3.3\text{V}, C_L = 50\text{pF}, V_{IH} = 3.3\text{V}, V_{IL} = 0\text{V}$		0.8		V
V_{OLV}	Dynamic LOW Valley Voltage (Note 4.)	$V_{CC} = 3.3\text{V}, C_L = 50\text{pF}, V_{IH} = 3.3\text{V}, V_{IL} = 0\text{V}$		0.8		V

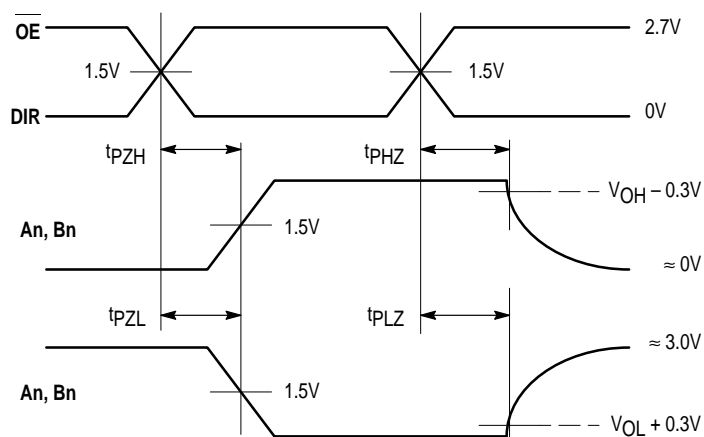
4. Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{IN}	Input Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	7	pF
$C_{I/O}$	Input/Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	10MHz, $V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	25	pF

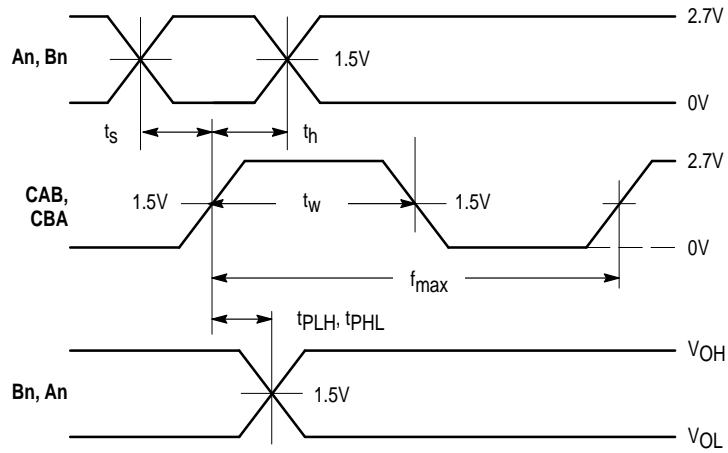


WAVEFORM 1 – SAB to B and SBA to A, An to Bn PROPAGATION DELAYS
 $t_R = t_F = 2.5ns$, 10% to 90%; $f = 1MHz$; $t_W = 500ns$



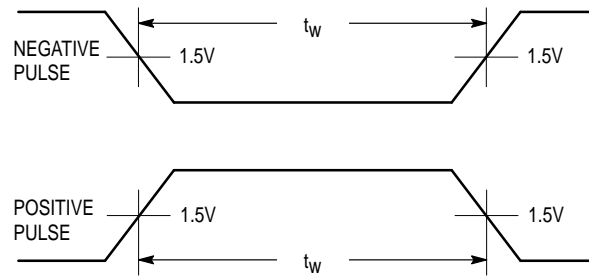
WAVEFORM 2 – OE/DIR to An/Bn OUTPUT ENABLE AND DISABLE TIMES
 $t_R = t_F = 2.5ns$, 10% to 90%; $f = 1MHz$; $t_W = 500ns$

Figure 1. AC Waveforms



WAVEFORM 3 – CLOCK to Bn/An PROPAGATION DELAYS, CLOCK MINIMUM PULSE WIDTH, An/Bn to CLOCK SETUP AND HOLD TIMES

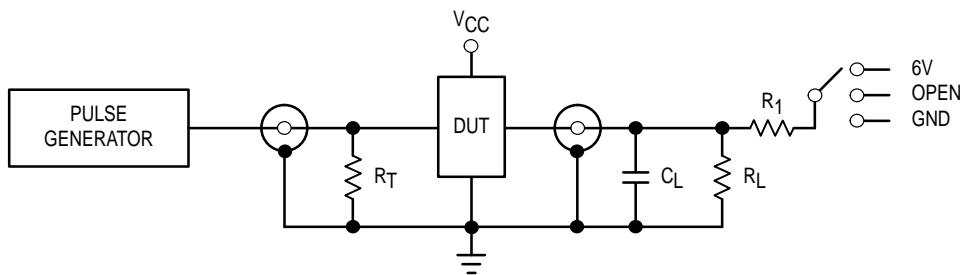
$t_R = t_F = 2.5\text{ns}$, 10% to 90%; $f = 1\text{MHz}$; $t_W = 500\text{ns}$ except when noted



WAVEFORM 4 – INPUT PULSE DEFINITION

$t_R = t_F = 2.5\text{ns}$, 10% to 90% of 0V to 2.7V

Figure 2. AC Waveforms



TEST	SWITCH
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PLZ}	6V
Open Collector/Drain t_{PLH} and t_{PHL}	6V
t_{PZH} , t_{PHZ}	GND

$C_L = 50\text{pF}$ or equivalent (Includes jig and probe capacitance)

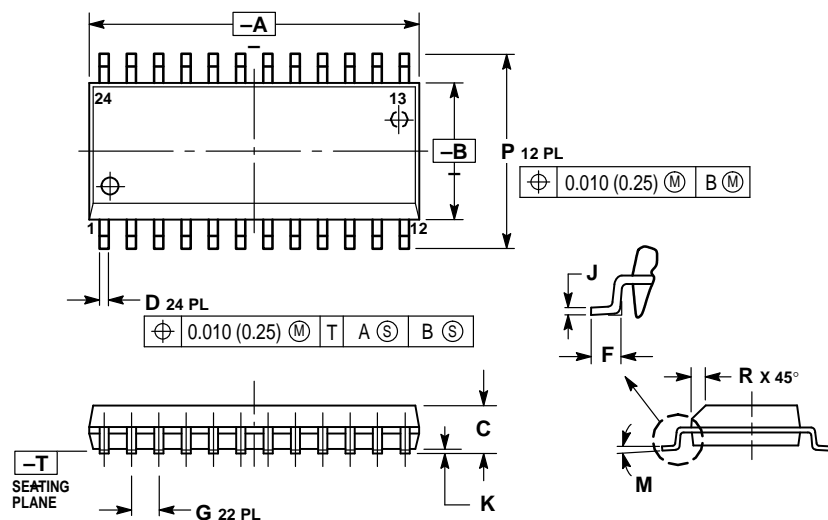
$R_L = R_1 = 500\Omega$ or equivalent

$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 3. Test Circuit

OUTLINE DIMENSIONS

DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751E-04
ISSUE E

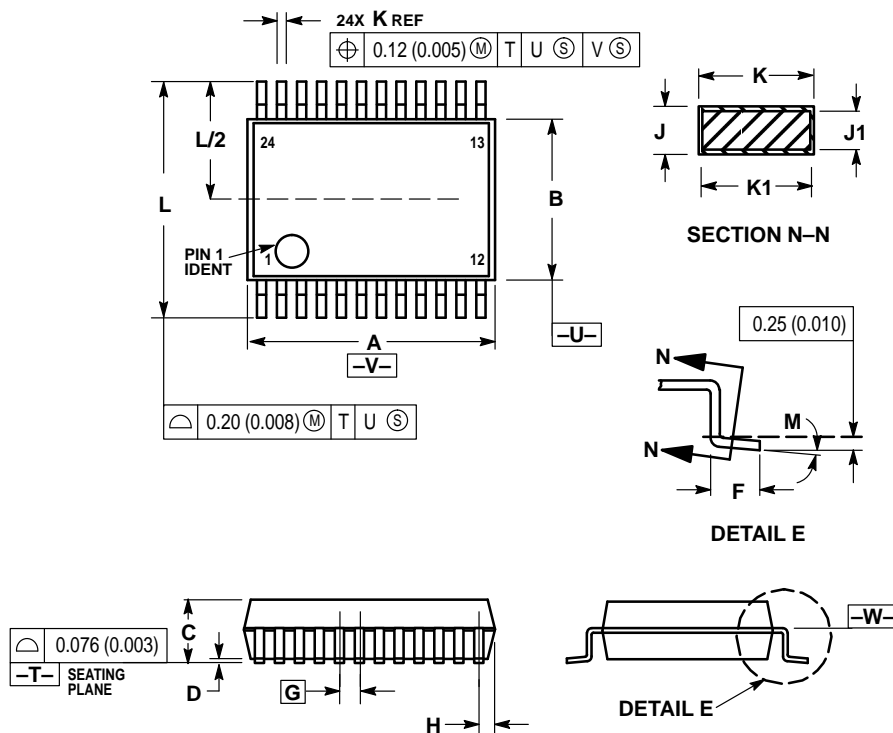


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

SD SUFFIX
PLASTIC SSOP PACKAGE
CASE 940D-03
ISSUE B



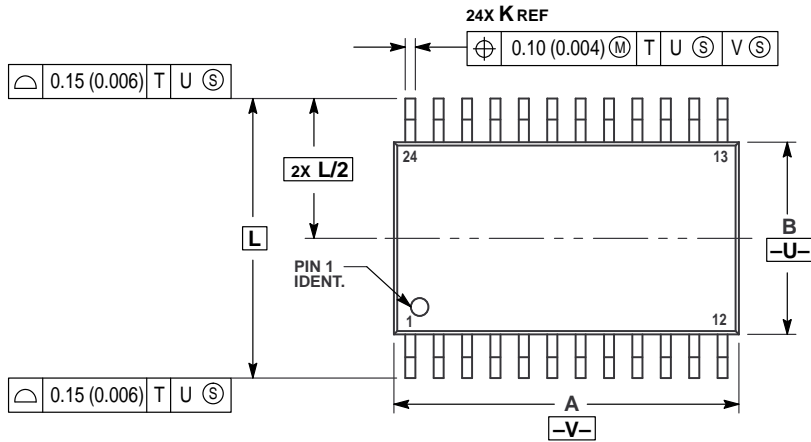
NOTES:

4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: MILLIMETER.
6. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
7. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
8. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF K DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION K BY MORE THAN 0.07 (0.002) AT LEAST MATERIAL CONDITION.
9. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
10. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.07	8.33	0.317	0.328
B	5.20	5.38	0.205	0.212
C	1.73	1.99	0.068	0.078
D	0.05	0.21	0.002	0.008
F	0.63	0.95	0.024	0.037
G	0.65 BSC		0.026 BSC	
H	0.44	0.60	0.017	0.024
J	0.09	0.20	0.003	0.008
J1	0.09	0.16	0.003	0.006
K	0.25	0.38	0.010	0.015
K1	0.25	0.33	0.010	0.013
L	7.65	7.90	0.301	0.311
M	0°	8°	0°	8°

OUTLINE DIMENSIONS

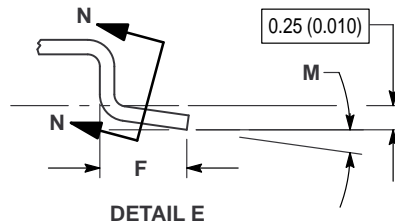
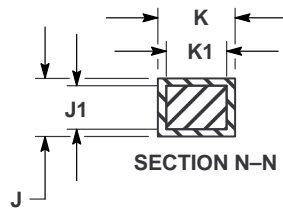
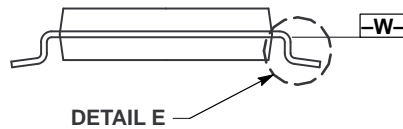
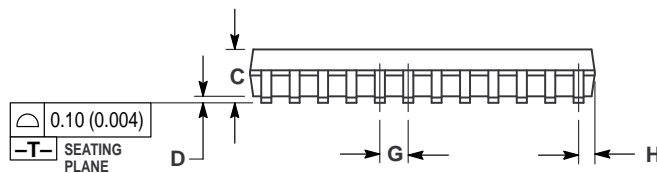
DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948H-01
ISSUE O




NOTES:

- 1 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- 2 CONTROLLING DIMENSION: MILLIMETER.
- 3 DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- 4 DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
- 5 DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
- 6 TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- 7 DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	7.70	7.90	0.303	0.311
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°



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USA/EUROPE/Locations Not Listed: Motorola Literature Distribution;
P.O. Box 5405, Denver, Colorado 80217. 1-800-441-2447

Mfax™: RMFAX0@email.sps.mot.com – TOUCHTONE 602-244-6609
INTERNET: <http://Design-NET.com>

JAPAN: Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, 6F Seibu-Butsuryu-Center,
3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 03-81-3521-8315

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298

