

## Triple PECL to LVPECL Translator

The MC100LVEL92 is a triple PECL to LVPECL translator. The device receives standard PECL signals and translates them to differential LVPECL output signals.

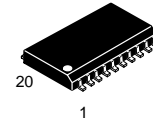
- 500ps Propagation Delays
- Fully Differential Design
- 20-Lead SOIC Package
- 5V and 3.3V Supplies Required
- >1500V ESD

A PECL  $V_{BB}$  output is provided for interfacing single ended PECL signals at the inputs. If a single ended PECL input is to be used the PECL  $V_{BB}$  output should be connected to the D input and the active signal will drive the D input. When used the PECL  $V_{BB}$  should be bypassed to ground via a 0.01 $\mu$ f capacitor. The PECL  $V_{BB}$  is designed to act as a switching reference for the MC100LVEL92 under single ended input conditions, as a result the pin can only source/sink 0.5mA of current.

To accomplish the PECL to LVPECL level translation, the MC100LVEL92 requires three power rails. The  $V_{CC}$  supply is to be connected to the standard PECL supply, the LVCC supply is to be connected to the LVPECL supply, and Ground is connected to the system ground plane. Both the  $V_{CC}$  and LVCC should be bypassed to ground with a 0.01 $\mu$ f capacitor.

Under open input conditions, the  $\bar{D}$  input will be biased at a  $V_{CC}/2$  voltage level and the D input will be pulled to ground. This condition will force the "Q" output low, ensuring stability.

# MC100LVEL92

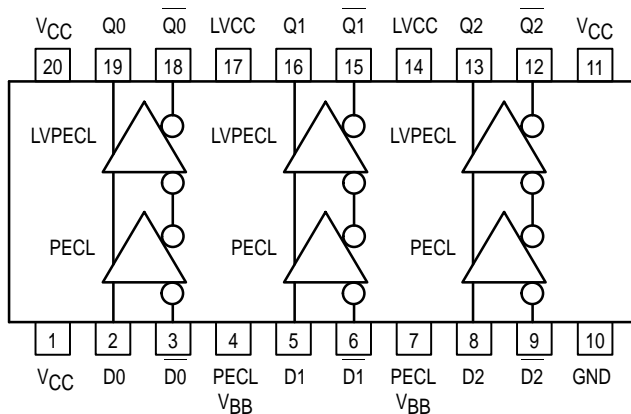


**DW SUFFIX**  
PLASTIC SOIC PACKAGE  
CASE 751D-04

### PIN NAMES

Pins	Function
Dn	PECL Inputs
Qn	LVPECL Outputs
$V_{BB}$	PECL Reference Voltage Output
LVCC	$V_{CC}$ for LVPECL Output
$V_{CC}$	$V_{CC}$ for PECL Inputs
GND	Common Ground Rail

**Logic Diagram and Pinout: 20-Lead SOIC (Top View)**



**PECL INPUT DC CHARACTERISTICS**

Symbol	Characteristic	-40°C		0°C		25°C			85°C		Unit	Condition
		Min	Max	Min	Max	Min	Typ	Max	Min	Max		
V <sub>CC</sub>	Power Supply Voltage	4.5	5.5	4.5	5.5	4.5		5.5	4.5	5.5	V	
I <sub>IH</sub>	Input HIGH Current		150		150			150		150	μA	
I <sub>IL</sub>	Input LOW Current D <sub>n</sub> D <sub>n</sub>	0.5 -600		0.5 -600		0.5 -600			0.5 -600		μA	
V <sub>PP</sub>	Minimum Peak-to-Peak Input <sup>1</sup>	150		150		150			150		mV	
V <sub>IH</sub>	Input HIGH Voltage <sup>2</sup>	3835	4120	3835	4120	3835		4120	3835	4120	mV	V <sub>CC</sub> = 5.0V
V <sub>IL</sub>	Input LOW Voltage <sup>2</sup>	3190	3515	3190	3525	3190		3525	3190	3525	mV	V <sub>CC</sub> = 5.0V
V <sub>BB</sub>	Reference Output <sup>2</sup>	3620	3740	3620	3740	3620		3740	3620	3740	mV	V <sub>CC</sub> = 5.0V
I <sub>VCC</sub>	Power Supply Current		12		12		8.0	12		12	mA	

- 150mV input guarantees full logic swing at the output.
- DC levels vary 1:1 with V<sub>CC</sub>.

**LVPECL OUTPUT DC CHARACTERISTICS**

Symbol	Characteristic	-40°C		0°C		25°C			85°C		Unit	Condition
		Min	Max	Min	Max	Min	Typ	Max	Min	Max		
V <sub>CC</sub>	Power Supply Voltage	3.0	3.8	3.0	3.8	3.0	3.3	3.8	3.0	3.8	V	
V <sub>OH</sub>	Output HIGH Voltage <sup>3</sup>	2.215	2.42	2.275	2.42	2.275	2.35	2.42	2.275	2.42	V	V <sub>CC</sub> = 3.3V
V <sub>OL</sub>	Output LOW Voltage <sup>3</sup>	1.47	1.745	1.49	1.68	1.49	1.60	1.68	1.49	1.68	V	V <sub>CC</sub> = 3.3V
I <sub>GND</sub>	Power Supply Current		20		20		15	20		21	mA	

- DC levels will vary 1:1 with V<sub>CC</sub>.

**MC100LVEL92**

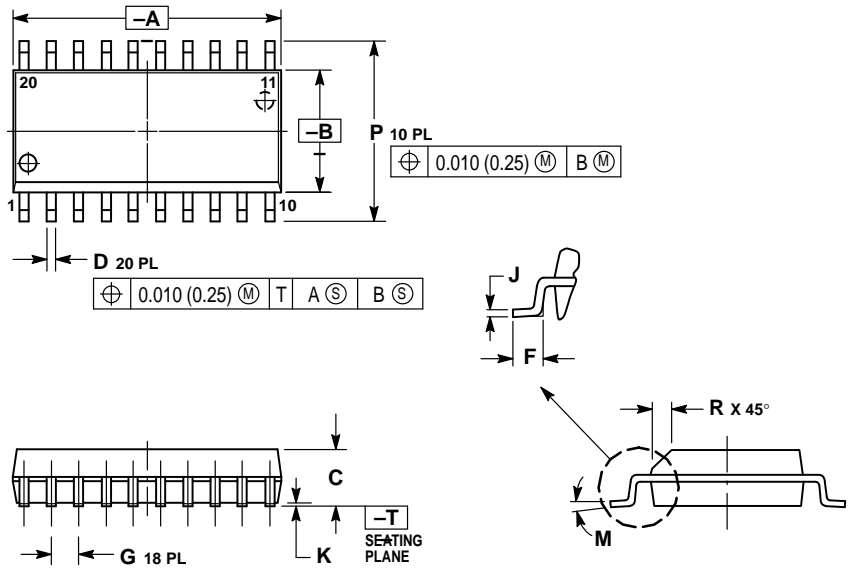
**AC CHARACTERISTICS** (LV<sub>CC</sub> = 3.0V to 3.8V; V<sub>CC</sub> = 4.5V to 5.5V)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay D to Q Diff S.E.	490 440	590 590	690 740	510 460	610 610	710 760	510 460	610 610	710 760	530 480	630 630	730 780	ps
t <sub>SKEW</sub>	Skew Output-to-Output <sup>4</sup> Part-to-Part (Diff) <sup>4</sup> Duty Cycle (Diff) <sup>5</sup>		20 20 25	100 200		20 20 25	100 200		20 20 25	100 200		20 20 25	100 200	ps
V <sub>PP</sub>	Minimum Input Swing <sup>6</sup>	150			150			150			150			mV
V <sub>CMR</sub>	Common Mode Range <sup>7</sup> V <sub>PP</sub> < 500mV  V <sub>PP</sub> ≥ 500mV	1.3		V <sub>CC</sub> -0.2	1.2		V <sub>CC</sub> -0.2	1.2		V <sub>CC</sub> -0.2	1.2		V <sub>CC</sub> -0.2	V
t <sub>r</sub> t <sub>f</sub>	Output Rise/Fall Times Q (20% – 80%)	320		580	320		580	320		580	320		580	ps

- Skews are valid across specified voltage range, part-to-part skew is for a given temperature.
- Duty cycle skew is the difference between a TPLH and TPHL propagation delay through a device. Common Mode Range
- Minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈40.
- The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V<sub>ppmin</sub> and 1V.

OUTLINE DIMENSIONS

DW SUFFIX  
PLASTIC SOIC PACKAGE  
CASE 751D-04  
ISSUE E



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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