# **10-Bit Low Power Bus Switch**

The ON Semiconductor 74FST3384 is a 10-bit low power bus switch. The device is CMOS TTL compatible when operating between 4 and 5.5 Volts. The device exhibits extremely low RON and adds nearly zero propagation delay. The device adds no noise or ground bounce to the system.

- $R_{ON} < 4 \Omega$  Typical
- Less Than 0.25 ns-Max Delay Through Switch
- Nearly Zero Standby Current
- No Circuit Bounce
- Control Inputs are TTL/CMOS Compatible
- Pin-For-Pin Compatible With QS3384, FST3384, CBT3384
- All Popular Packages: SOIC-24, TSSOP-24, QSOP-24

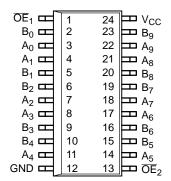


Figure 1. 24-Lead Pinout

### **TRUTH TABLE**

ŌĒ <sub>1</sub>	OE <sub>2</sub>	B <sub>0</sub> -B <sub>4</sub>	B <sub>5</sub> -B <sub>9</sub>	Function
L	L	A <sub>0</sub> _A <sub>4</sub>	A <sub>5</sub> -A <sub>9</sub>	Connect
L	Н	A <sub>0</sub> _A <sub>4</sub>	HIGH-Z State	Connect
Н	L	HIGH-Z State	A <sub>5</sub> -A <sub>9</sub>	Connect
Н	Н	HIGH-Z State	HIGH-Z State	Disconnect

NOTE: H = HIGH Voltage Level, L = LOW Voltage Level

#### **PIN NAMES**

Pin	Description
$\overline{OE}_1$ , $\overline{OE}_2$	Bus Switch Enable
A <sub>0</sub> -A <sub>9</sub>	Bus A
B <sub>0</sub> -B <sub>9</sub>	Bus B

1



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## **MARKING DIAGRAMS**



**DW SUFFIX CASE 751E** 

24 **AAAAAAAAAA** FST3384 o AWLYWW 1 9 9 9 9 9 9 9 9 9 9 9 9



TSSOP-24

24 ARRARARARA **FST** 3384 ALYW 







QSOP-24 **QS SUFFIX CASE 492B** 

> = Assembly Location Α

L, WL = Wafer Lot Y, YY = Year W, WW = Work Week

#### ORDERING INFORMATION

	Device	Package	Shipping				
74	FST3384DW	SO-24	48 Units/Rail				
74	FST3384DWR2	SO-24	2500 Units/Reel				
74	FST3384DT	TSSOP-24	96 Units/Rail				
74	FST3384DTR2	TSSOP-24	2500 Units/Reel				
74	FST3384QS	QSOP-24	96 Units/Rail				
74	FST3384QSR	QSOP-24	2500 Units/Reel				

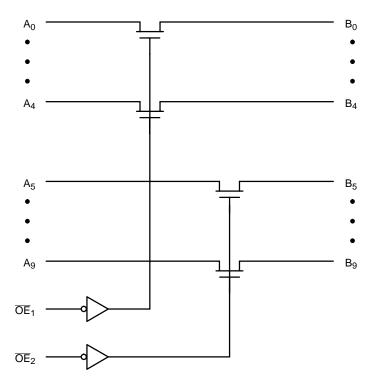


Figure 2. Logic Diagram

#### **MAXIMUM RATINGS**

Symbol	Parameter		Value	Unit
V <sub>CC</sub>	DC Supply Voltage		-0.5 to $+7.0$	V
VI	DC Input Voltage		-0.5  to  +7.0	V
Vo	DC Output Voltage		-0.5  to  +7.0	V
I <sub>IK</sub>	DC Input Diode Current	$V_{I} < GND$	-50	mA
I <sub>OK</sub>	DC Output Diode Current	V <sub>O</sub> < GND	-50	mA
I <sub>O</sub>	DC Output Sink Current		128	mA
I <sub>CC</sub>	DC Supply Current per Supply Pin		±100	mA
I <sub>GND</sub>	DC Ground Current per Ground Pin		±100	mA
T <sub>STG</sub>	Storage Temperature Range		-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Second	ls	260	°C
TJ	Junction Temperature Under Bias		+150	°C
$\theta_{\sf JA}$	Thermal Resistance	SOIC TSSOP QSOP	125 170 200	°C/W
MSL	Moisture Sensitivity		Level 1	
F <sub>R</sub>	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
V <sub>ESD</sub>	ESD Withstand Voltage	Human Body Model (Note 1) Machine Model (Note 2) Charged Device Model (Note 3)	>2000 >200 N/A	V
I <sub>LATCH-UP</sub>	Latch–Up Performance Above V <sub>CC</sub>	and Below GND at 85°C (Note 4)	±500	mA

Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum–rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

- 1. Tested to EIA/JESD22-A114-A.
- 2. Tested to EIA/JESD22-A115-A.
- 3. Tested to JESD22-C101-A.
- 4. Tested to EIA/JESD78.

### RECOMMENDED OPERATING CONDITIONS

Symbol	Pa	Min	Max	Unit	
V <sub>CC</sub>	Supply Voltage	Operating, Data Retention Only	4.0	5.5	V
VI	Input Voltage	(Note 5)	0	5.5	V
V <sub>O</sub>	Output Voltage	(HIGH or LOW State)	0	5.5	V
T <sub>A</sub>	Operating Free–Air Temperature		-40	+85	°C
Δt/ΔV	Input Transition Rise or Fall Rate Switch I/O	Switch Control Input $V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$	0	DC 5	ns/V

5. Unused control inputs may not be left open. All control inputs must be tied to a high or low logic input voltage level.

### DC ELECTRICAL CHARACTERISTICS

			Vcc	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$			
Symbol	Parameter	Conditions	(V)	Min	Тур*	Max	Unit
V <sub>IK</sub>	Clamp Diode Resistance	$I_{IN} = -18mA$	4.5			-1.2	V
V <sub>IH</sub>	High-Level Input Voltage		4.0 to 5.5	2.0			V
V <sub>IL</sub>	Low-Level Input Voltage		4.0 to 5.5			0.8	V
I <sub>I</sub>	Input Leakage Current	$0 \le V_{IN} \le 5.5 V$	5.5			±1.0	μΑ
I <sub>OZ</sub>	OFF-STATE Leakage Current	$0 \le A, B \le V_{CC}$	5.5			±1.0	μΑ
R <sub>ON</sub>	Switch On Resistance (Note 6)	V <sub>IN</sub> = 0 V, I <sub>IN</sub> = 64 mA	4.5		4	7	Ω
		V <sub>IN</sub> = 0 V, I <sub>IN</sub> = 30 mA	4.5		4	7	
		V <sub>IN</sub> = 2.4 V, I <sub>IN</sub> = 15 mA	4.5		8	15	
		V <sub>IN</sub> = 2.4 V, I <sub>IN</sub> = 15 mA	4.0		11	20	
I <sub>CC</sub>	Quiescent Supply Current	V <sub>IN</sub> = V <sub>CC</sub> or GND, I <sub>OUT</sub> = 0	5.5			3	μΑ
$\Delta I_{CC}$	Increase In I <sub>CC</sub> per Input	One input at 3.4 V, Other inputs at $V_{\mbox{\footnotesize CC}}$ or GND	5.5			2.5	mA

#### **AC ELECTRICAL CHARACTERISTICS**

				$f_A = -40^{\circ}C = 50$		<b>)</b> Ω	
			V <sub>CC</sub> = 4	.5–5.5 V	V <sub>CC</sub> =	4.0 V	
Symbol	Parameter	Conditions	Min	Max	Min	Max	Unit
t <sub>PHL</sub> , t <sub>PLH</sub>	Prop Delay Bus to Bus (Note 7)	V <sub>I</sub> = OPEN		0.25		0.25	ns
t <sub>PZH</sub> , t <sub>PZL</sub>	Output Enable Time, IOE to Bus A, B	$V_I = OPEN \text{ for } t_{PZH}$	1.0	5.7		6.2	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Output Disable Time, I <sub>OE</sub> to Bus A, B	$V_I = OPEN \text{ for } t_{PHZ}$	1.0	5.2		5.5	ns

<sup>7.</sup> This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).

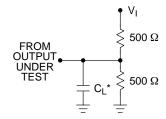
# **CAPACITANCE** (Note 8)

Symbol	Parameter	Conditions	Тур	Max	Unit
C <sub>IN</sub>	Control Pin Input Capacitance	V <sub>CC</sub> = 5.0 V	6		pF
C <sub>I/O</sub>	Port Input/Output Capacitance	$V_{CC}$ , $\overline{OE} = 5.0 \text{ V}$	13		pF

<sup>8.</sup>  $T_A = +25$ °C, f = 1 MHz, Capacitance is characterized but not tested.

<sup>\*</sup>Typical values are at V<sub>CC</sub> = 5.0 V and T<sub>A</sub> = 25°C.
6. Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

### **AC Loading and Waveforms**



#### NOTES:

- 1. Input driven by 50  $\Omega$  source terminated in 50  $\Omega.$
- 2. CL includes load and stray capacitance.

Figure 3. AC Test Circuit

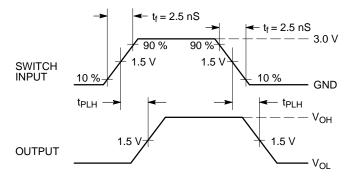


Figure 4. Propagation Delays

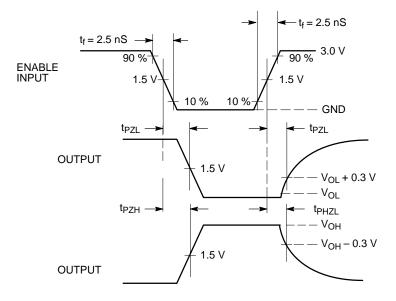
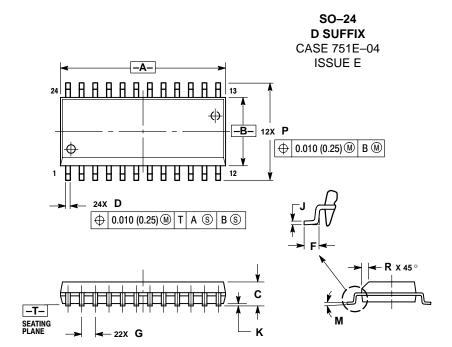


Figure 5. Enable/Disable Delays

 $<sup>{}^{*}</sup>C_{L} = 50 pF$ 

### **PACKAGE DIMENSIONS**



#### NOTES:

- NOTES:

  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

  2. CONTROLLING DIMENSION: MILLIMETER.

  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.

  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

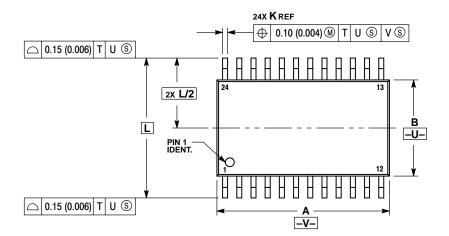
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

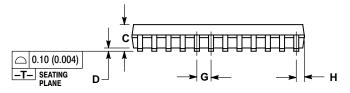
	MILLIN	IETERS	INCHES		
DIM	MIN	MAX	MIN	MAX	
Α	15.25	15.54	0.601	0.612	
В	7.40	7.60	0.292	0.299	
С	2.35	2.65	0.093	0.104	
D	0.35	0.49	0.014	0.019	
F	0.41	0.90	0.016	0.035	
G	1.27	BSC	0.050 BSC		
J	0.23	0.32	0.009	0.013	
K	0.13	0.29	0.005	0.011	
M	0°	8°	0°	8°	
Р	10.05	10.55	0.395	0.415	
R	0.25	0.75	0.010	0.029	

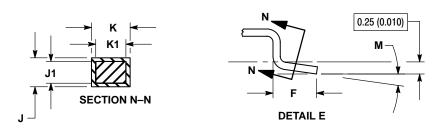
#### PACKAGE DIMENSIONS

# TSSOP-24 **DT SUFFIX**

CASE 948H-01 **ISSUE A** 



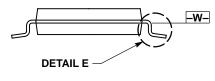




- NOTES:
  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
- 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006)
- PER SIDE.

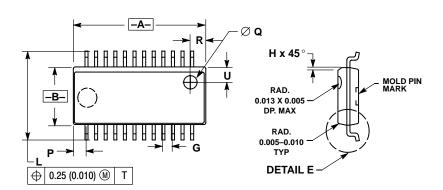
  4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED
- PROTRUSION SHALL NOT EXCEED
  0.25 (0.010) PER SIDE
  5. DIMENSION K DOES NOT INCLUDE DAMBAR
  PROTRUSION. ALLOWABLE DAMBAR
  PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN
  EXCESS OF THE K DIMENSION AT MAXIMUM
  MATERIAL CONDITION.
  6. TERMINAL NUMBERS ARE SHOWN FOR
  REFERENCE ONLY.
  DIMENSION A MAID A ARE TO BE DETERMINED.
- DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

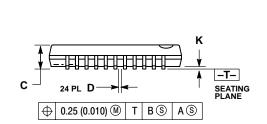
	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	7.70	7.90	0.303	0.311
В	4.30	4.50	0.169	0.177
С		1.20		0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65	BSC	0.026	BSC
Н	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40			
M	0°	8°	0°	8°

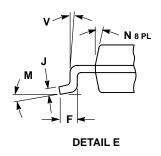


#### PACKAGE DIMENSIONS

### QSOP-24 **QS SUFFIX** CASE 492B-01 **ISSUE O**







- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
  THE BOTTOM PACKAGE SHALL BE BIGGER THAN THE TOP PACKAGE BY 4 MILS (NOTE: LEAD SIDE ONLY). BOTTOM PACKAGE DIMENSION SHALL FOLLOW THE DIMENSION STATED IN THIS DRAWING.
- PLASTIC DIMENSIONS DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 6 MILS PER
- BOTTOM EJECTOR PIN WILL INCLUDE THE COUNTRY OF ORIGIN (COO) AND MOLD CAVITY I.D.

	INC	HES	MILLIM	ETERS
DIM	MAX	MIN	MAX	MIN
Α	0.337	0.344	8.56	8.74
В	0.150	0.157	3.81	3.99
С	0.061	0.068	1.55	1.73
D	0.008	0.012	0.20	0.31
F	0.016	0.035	0.41	0.89
G	0.025	BSC	0.64	BSC
Н	0.008	0.018	0.20	0.46
J	0.0098	0.0075	0.249	0.191
K	0.004	0.010	0.10	0.25
L	0.230	0.244	5.84	6.20
M	0°	8°	0°	8°
N	0°	7°	0°	7°
P	0.027	0.037	0.69	0.94
Q	0.035	DIA	0.89	DIA
R	0.035	0.045	0.89	1.14
U	0.035	0.045	0.89	1.14
٧	0°	8°	0°	8°

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