Product Preview **Trench Power MOSFET** -8.0 V Dual, P-Channel, Gate Zener, SC-88

This P-Channel dual device was designed with a small footprint package (2 X 2 mm) and ON Semiconductor's leading trench process featuring low $R_{DS(on)}$ for reduced footprint and increased circuit efficiency. The low $R_{DS(on)}$ performance is particularly suited for single or dual cell Li-Ion battery supplied devices such as cell phones, media players, digital cameras, PDAs, etc.

Features & Benefits

- Leading -8.0 V Trench for Low R_{DS(on)}
- Small Footprint Package for Less Board Space
- ESD Protected Gate
- Pb Free Package for Green Manufacturing

Applications

- Load/Power Management
- Charging Circuits
- Buck-Boost Synchronous Rectification

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V _{DSS}	-8.0	V
Gate-to-Source Voltage	V _{GS}	±8.0	V
Drain Current - Continuous @ T _A = 25°C (Note 1) - Pulsed Drain Current (t = 10 μs)	I _D I _{DM}	-0.59 ±1.0	A
Steady State Power Dissipation @ $T_A = 25^{\circ}C$ (Note 1)	PD	0.27	W
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150	°C
Continuous Source Current (Body Diode)	ا _S	-0.59	А
Lead Temperature for Soldering Purposes (1/8" from case for 10 seconds)	ΤL	260	°C

THERMAL RESISTANCE RATINGS

Thermal Resistance			°C/W
- Junction- to- Ambient - Steady State (Note 1)	$R_{\theta JA}$	TBD	
- Junction-to-Ambient - $t = 10 \text{ s}$ (Note 1)	$R_{\theta JA}$	TBD	
- Junction-to-Lead - Steady State (Note 2)	$R_{ extsf{ heta}JL}$	TBD	

- Surface-mounted on FR4 board using 1" sq pad size (Cu area = 1.127 in sq [1 oz] including traces)
- Surface-mounted on FR4 board using the minimum recommended pad size (Cu area = TBD in sq)

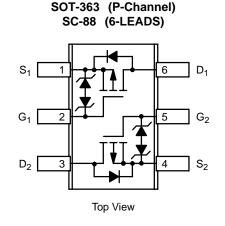
This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

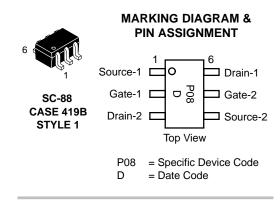


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 $\begin{array}{l} {\sf V}_{{\sf BR}({\sf DSS})} = \text{-8.0 VOLTS} \\ {\sf R}_{{\sf DS}({\sf on})} \; ({\sf max}) @ {\sf V}_{{\sf GS}} = 600 \; {\sf m\Omega} @ -4.5 \; {\sf V} \\ {\sf I}_{{\sf D}({\sf max})} \; ({\sf Note}\; 1) = -0.57 \; {\sf A} \\ {\sf R}_{{\sf DS}({\sf on})} \; ({\sf max}) @ {\sf V}_{{\sf GS}} = 850 \; {\sf m\Omega} @ -2.5 \; {\sf V} \\ {\sf I}_{{\sf D}({\sf max})} \; ({\sf Note}\; 1) = -0.48 \; {\sf A} \\ {\sf R}_{{\sf DS}({\sf on})} \; ({\sf max}) @ {\sf V}_{{\sf GS}} = 1200 \; {\sf m\Omega} \; @ -1.8 {\sf V} \\ {\sf I}_{{\sf D}({\sf max})} \; ({\sf Note}\; 1) = -0.20 \; {\sf A} \end{array}$





ORDERING INFORMATION

Device	Package	Shipping
NTJD2101PT1	SC-88	3000/Tape & Reel

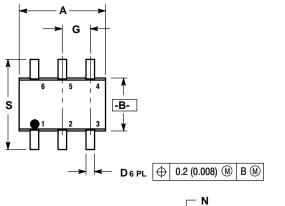
ELECTRICAL CHARACTERISTICS ($T_A = 25^{\circ}C$ unless otherwise noted)

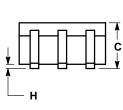
Cha	Symbol	Min	Тур	Max	Unit	
OFF CHARACTERISTICS		•				
Drain-to-Source Breakdown Voltage (Note 3) ($V_{GS} = 0 V$, $I_D = -250 \mu A$)			-8.0	-	-	V
Zero Gate Voltage Drain Current (Note 3) $(V_{GS} = 0 V, V_{DS} = -6.4 V)$		I _{DSS}	-	-	1.0	μA
Gate-to-Source Leakage Current (V _{GS} = ± 8.0 V, V _{DS} = 0 V)	•		-	-	1.0	μΑ
ON CHARACTERISTICS					I	
Gate Threshold Voltage (Note 3) ($V_{GS} = V_{DS}$, $I_D = -250 \ \mu A$)			-0.45	-	-	V
Drain-to-Source On-Resistance $(V_{GS} = -4.5 \text{ V}, I_D = -0.57 \text{ A})$ $(V_{GS} = -2.5 \text{ V}, I_D = -0.48 \text{ A})$ $(V_{GS} = -1.8 \text{ V}, I_D = -0.20 \text{ A})$		R _{DS(on)}	-	TBD TBD TBD	600 850 1200	mΩ
Forward Transconductance (V _{DS} =	9FS	-	TBD	-	S	
CHARGES, CAPACITANCES & GAT	E RESISTANCE					
Input Capacitance		C _{iss}	-	TBD	-	pF
Output Capacitance	(V _{GS} = 0 V, f = 1 MHz, V _{DS} = -8.0 V)	C _{oss}	-	TBD	-	
Reverse Transfer Capacitance		C _{rss}	-	TBD	-	
Total Gate Charge		Q _{G(tot)}	-	TBD	-	nC
Gate-to-Source Gate Charge	$(V_{GS} = -4.5 \text{ V}, V_{DS} = -4.0 \text{ V},$ $I_{D} = -0.57 \text{ A})$	Q _{GS}	-	TBD	-	
Gate-to-Drain "Miller" Charge		Q _{GD}	-	TBD	-	
	Note 4)	·				
Turn-On Delay Time		t _{d(on)}	-	TBD	-	ns
Rise Time	(V _{GS} = -4.5 V, V _{DS} = -4.0 V,	t _r	-	TBD	-	
Turn-Of f Delay Time	$I_D = -0.57 \text{ A}, \text{ R}_G = 3.0 \Omega$	t _{d(off)}	-	TBD	-	
Fall Time]	t _f	-	TBD	-	
DRAIN-SOURCE DIODE CHARACT	ERISTICS					
Forward Diode Voltage	(V _{GS} = 0 V, I _{SD} = -0.23 A)	V _{SD}	-	TBD	-	V
Reverse Recovery Time	(dI _{SD} /dt = 100 A/µs, I _{SD} = -0.23 A)	t _{rr}	-	TBD	TBD	ns

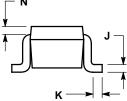
Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
Switching characteristics are independent of operating junction temperature.

PACKAGE DIMENSIONS

SC-88 (SOT-363) CASE 419B-02 **ISSUE N**







NOTES: 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: INCH. 3. 419B-01 DBSOLETE, NEW STANDARD 419B-02.

	INC	HES	MILLIMETERS		
DIM	MIN	MAX	MIN	MAX	
Α	0.071	0.087	1.80	2.20	
в	0.045	0.053	1.15	1.35	
С	0.031	0.043	0.80	1.10	
D	0.004	0.012	0.10	0.30	
G	0.026 BSC		0.65 BSC		
н		0.004		0.10	
J	0.004	0.010	0.10	0.25	
κ	0.004	0.012	0.10	0.30	
Ν	0.008 REF 0.20 REF		REF		
S	0.079	0.087	2.00	2.20	

STYLE 1: PIN 1. EMITTER 2 2. BASE 2 3. COLLECTOR 1 4. EMITTER 1 5. BASE 1 6. COLLECTOR 2

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