NTGD3122C

Power MOSFET

Complementary, 20 V, +3.3/−2.5 A, TSOP−6 Dual

Features

- Complementary N−Channel and P−Channel MOSFET
- Small Size (3 x 3 mm) Dual TSOP−6 Package
- Leading Edge Trench Technology for Low On Resistance
- Reduced Gate Charge to Improve Switching Response
- Independently Connected Devices to Provide Design Flexibility
- This is a Pb−Free Device

Applications

- DC−DC Conversion Circuits
- Load/Power Switching
- LCD Display Inverter
- Portable Devices like PDA's, Cellular Phones, and Hard Drives

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	20	V
Gate−to−Source Voltage (N & P−Ch)			V_{GS}	±12	V
N−Channel Continuous Drain Current (Note 1)	Steady State	T_A = 25°C	I_D	3.0	A
		T_A = 85°C		2.1	
	t ≤ 5 s	T_A = 25°C		3.3	
P−Channel Continuous Drain Current (Note 1)	Steady State	T_A = 25°C	I_D	2.3	A
		T_A = 85°C		1.6	
	t ≤ 5 s	T_A = 25°C		2.5	
Power Dissipation (Note 1)	Steady State	T_A = 25°C	P_D	1.1	W
	t ≤ 5 s			1.3	
N−Channel Continuous Drain Current (Note 2)		T_A = 25°C	I_D	2.1	A
		T_A = 85°C		1.6	
P−Channel Continuous Drain Current (Note 2)		T_A = 25°C	I_D	1.6	A
		T_A = 85°C		1.2	
Power Dissipation (Note 2)		T_A = 25°C	P_D	0.56	W
Pulsed Drain Current	N−Ch	t_p = 10 μs	I_{DM}	9.0	A
	P−Ch			7.0	
Operating Junction and Storage Temperature			T_J, T_{STG}	−55 to 150	°C
Source Current (Body Diode) (Note 2)			I_S	0.8	A
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces). Both die on.
2. Surface Mounted on FR4 Board using the minimum recommended pad size. (Cu area = 30 mm^2 [2 oz]). Both die on.

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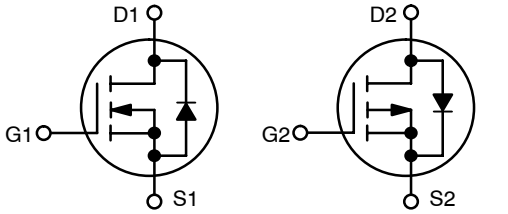
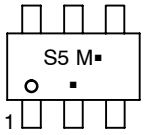
$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX (Note 1)
N−Ch 20 V	80 mΩ @ 4.5 V	3.3 A
	110 mΩ @ 2.5 V	
P−Ch −20 V	145 mΩ @ 4.5 V	−2.5 A
	200 mΩ @ 2.5 V	



N−CHANNEL MOSFET **P−CHANNEL MOSFET**

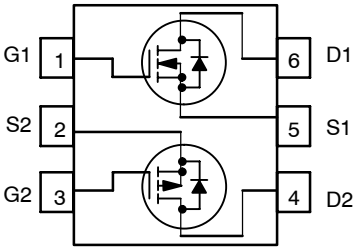
TSOP6
CASE 318G

MARKING DIAGRAM



S5 = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN CONNECTION



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

THERMAL RESISTANCE RATINGS (NTGD3122C)

Parameter	Symbol	Max	Unit
BOTH DIE ON			
Junction−to−Ambient − Steady State (Note 3)	$R_{\theta JA}$	115	°C/W
Junction−to−Ambient − t ≤ 5 s (Note 3)	$R_{\theta JA}$	95	
Junction−to−Ambient − Steady State (Note 4)	$R_{\theta JA}$	225	
ONE DIE ON			
Junction−to−Ambient − Steady State (Note 3)	$R_{\theta JA}$	175	°C/W
Junction−to−Ambient − t ≤ 5 s (Note 3)	$R_{\theta JA}$	160	
Junction−to−Ambient − Steady State (Note 4)	$R_{\theta JA}$	305	

3. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
4. Surface Mounted on FR4 Board using the minimum recommended pad size (Cu area = 30 mm^2 [2 oz] including traces).

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	N/P	Test Conditions		Min	Typ	Max	Unit
OFF CHARACTERISTICS (Note 5)								
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	N	V_{GS} = 0 V	I_D = 250 μA	20			V
		P		I_D = −250 μA	−20			
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	N				13.6		mV/°C
		P				14.4		
Zero Gate Voltage Drain Current	I_{DSS}	N	V_{GS} = 0 V, V_{DS} = 16 V	T_J = 25 °C			1.0	μA
		P	V_{GS} = 0 V, V_{DS} = −16 V				−1.0	
		N	V_{GS} = 0 V, V_{DS} = 16 V	T_J = 85 °C			10	
		P	V_{GS} = 0 V, V_{DS} = −16 V				−10	
Gate−to−Source Leakage Current	I_{GSS}	N	V_{DS} = 0 V, V_{GS} = ±12 V				±100	nA
		P	V_{DS} = 0 V, V_{GS} = ±12 V				±100	
ON CHARACTERISTICS (Note 5)								
Gate Threshold Voltage	$V_{GS(TH)}$	N	V_{GS} = V_{DS}	I_D = 250 μA	0.6	0.9	1.4	V
		P		I_D = −250 μA	−0.6	−0.9	−1.4	
Drain−to−Source On Resistance	$R_{DS(on)}$	N	V_{GS} = 4.5 V , I_D = 2.5 A			60	80	mΩ
			V_{GS} = 2.5 V , I_D = 2.2 A			70	110	
		P	V_{GS} = −4.5 V , I_D = −1.9 A			95	145	
			V_{GS} = −2.5 V, I_D = −1.6 A			150	200	
Forward Transconductance	g_{FS}	N	V_{DS} = 5.0 V, I_D = 2.5 A			4.8		S
		P	V_{DS} = −5.0 V , I_D = −2.5 A			4.0		
CHARGES AND CAPACITANCES								
Input Capacitance	C_{ISS}	N	f = 1 MHz, V_{GS} = 0 V	V_{DS} = 10 V		320		pF
Output Capacitance	C_{OSS}					72		
Reverse Transfer Capacitance	C_{RSS}					43		
Input Capacitance	C_{ISS}	P		V_{DS} = −10 V		390		
Output Capacitance	C_{OSS}					75		
Reverse Transfer Capacitance	C_{RSS}					37		

5. Pulse Test: pulse width ≤ 250 μs, duty cycle ≤ 2%.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	N/P	Test Conditions	Min	Typ	Max	Unit
CHARGES AND CAPACITANCES							
Total Gate Charge	$Q_{G(TOT)}$	N	V_{GS} = 4.5 V, V_{DS} = 10 V, I_D = 3.0 A		3.9	5.5	nC
Threshold Gate Charge	$Q_{G(TH)}$				0.7		
Gate−to−Source Gate Charge	Q_{GS}				1.0		
Gate−to−Drain “Miller” Charge	Q_{GD}				1.0		
Total Gate Charge	$Q_{G(TOT)}$	P	V_{GS} = −4.5 V, V_{DS} = −10 V, I_D = −2.2 A		3.7	5.5	
Threshold Gate Charge	$Q_{G(TH)}$				0.7		
Gate−to−Source Gate Charge	Q_{GS}				1.1		
Gate−to−Drain “Miller” Charge	Q_{GD}				1.2		
SWITCHING CHARACTERISTICS (Note 6)							
Turn−On Delay Time	$t_{d(ON)}$	N	V_{GS} = 4.5 V, V_{DD} = 10 V, I_D = 1.0 A, R_G = 6.0 Ω		5.8		ns
Rise Time	t_r				5.9		
Turn−Off Delay Time	$t_{d(OFF)}$				11.8		
Fall Time	t_f				2.1		
Turn−On Delay Time	$t_{d(ON)}$	P	V_{GS} = −4.5 V, V_{DD} = −10 V, I_D = −1.0 A, R_G = 6.0 Ω		6.7		
Rise Time	t_r				12.7		
Turn−Off Delay Time	$t_{d(OFF)}$				13.2		
Fall Time	t_f				11		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	N	V_{GS} = 0 V, T_J = 25 °C, I_S = 0.8 A		0.8	1.2	V
		P	V_{GS} = 0 V, T_J = 25 °C, I_S = −0.8 A		−0.8	−1.2	
Reverse Recovery Time	t_{RR}	N	V_{GS} = 0 V, dI_S / dt = 100 A/μs, I_S = 1.0 A		10.3		ns
Charge Time	t_a				6.5		
Discharge Time	t_b				3.8		
Reverse Recovery Charge	Q_{RR}				3.0		nC
Reverse Recovery Time	t_{RR}	P	V_{GS} = 0 V, dI_S / dt = 100 A/μs, I_S = −1.0 A		7.4		ns
Charge Time	t_a				4.8		
Discharge Time	t_b				2.6		
Reverse Recovery Charge	Q_{RR}				2.4		nC

6. Switching characteristics are independent of operating junction temperatures.

N−CHANNEL

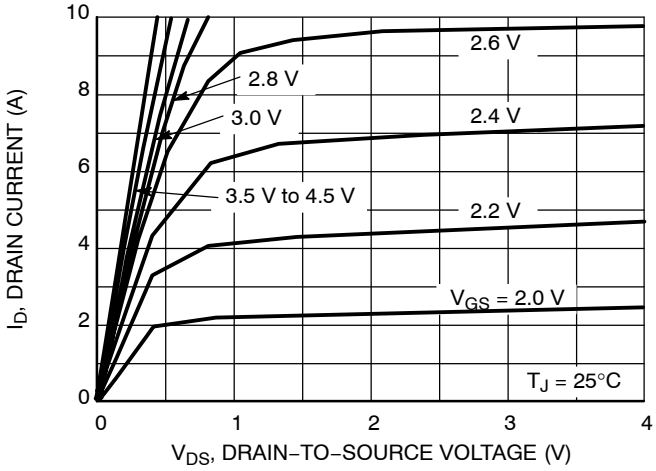


Figure 1. On−Region Characteristics

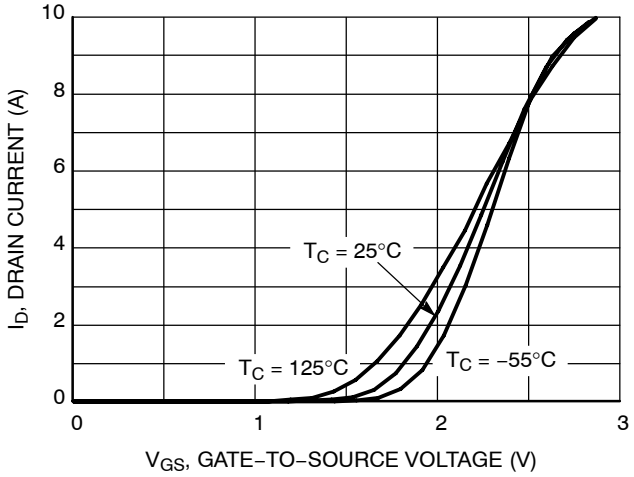


Figure 2. Transfer Characteristics

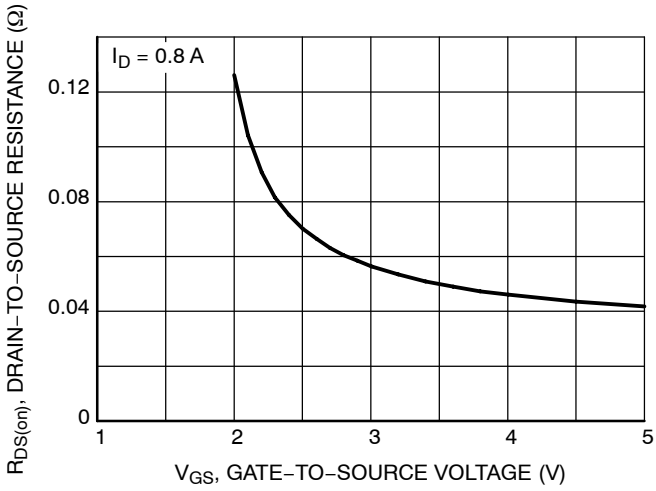


Figure 3. On−Resistance versus Gate−to−Source Voltage

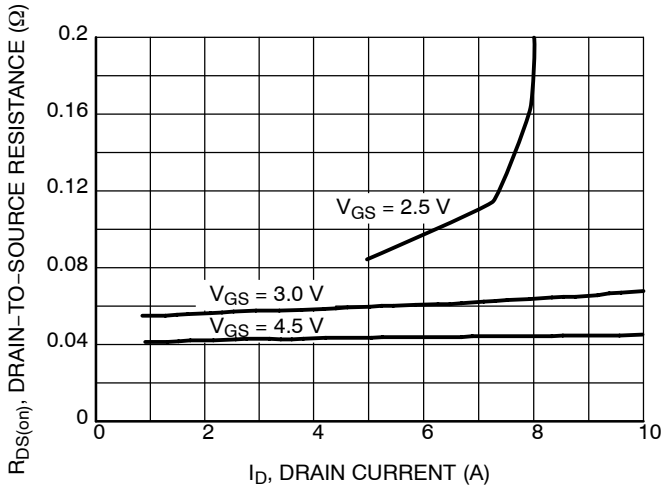


Figure 4. On−Resistance versus Drain Current and Temperature

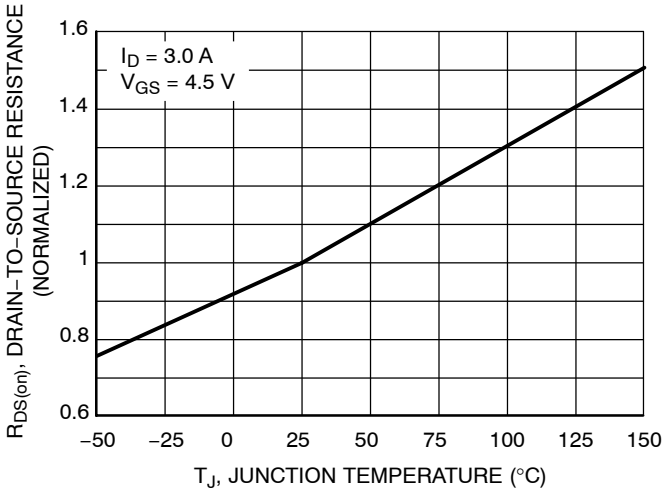


Figure 5. On−Resistance Variation with Temperature

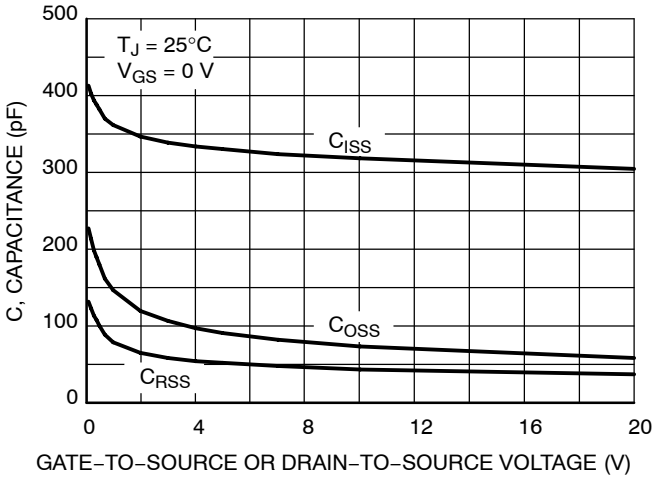


Figure 6. Capacitance Variation

N−CHANNEL

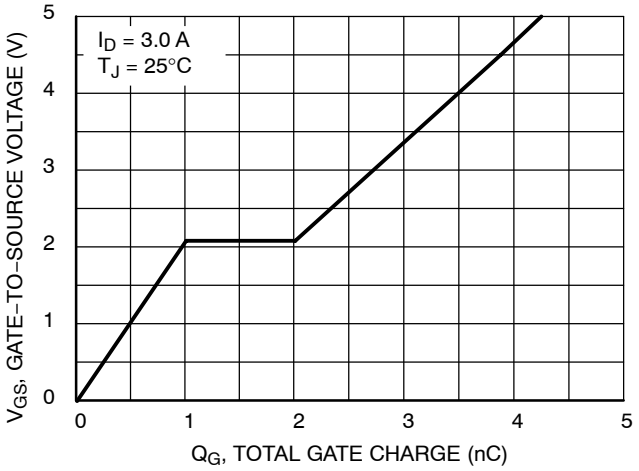


Figure 7. Gate−to−Source and Drain−to−Source Voltage versus Total Charge

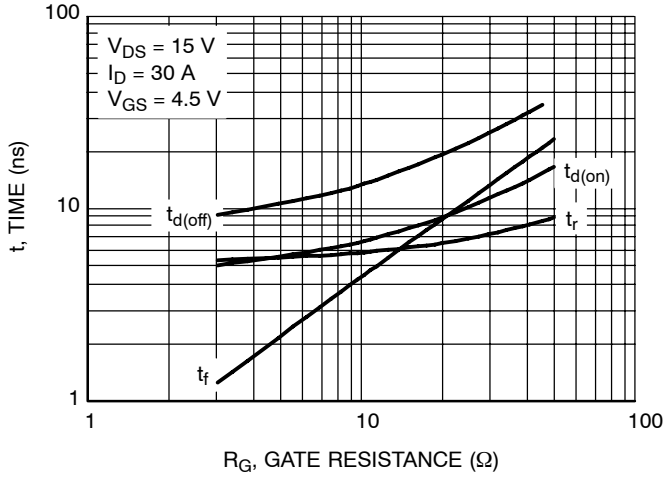


Figure 8. Resistive Switching Time Variation versus Gate Resistance

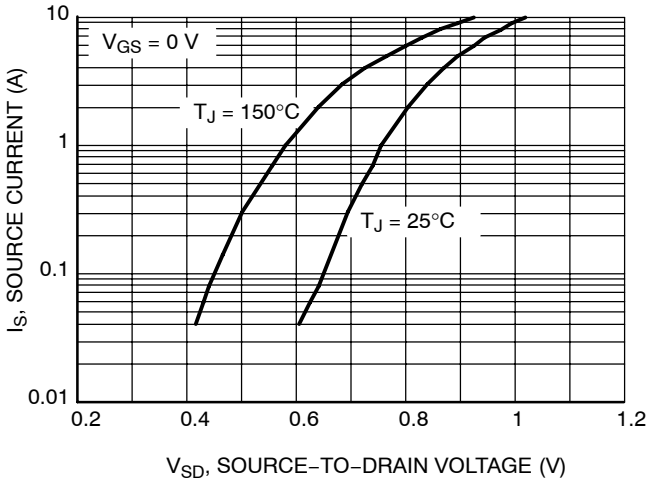


Figure 9. Diode Forward Voltage versus Current

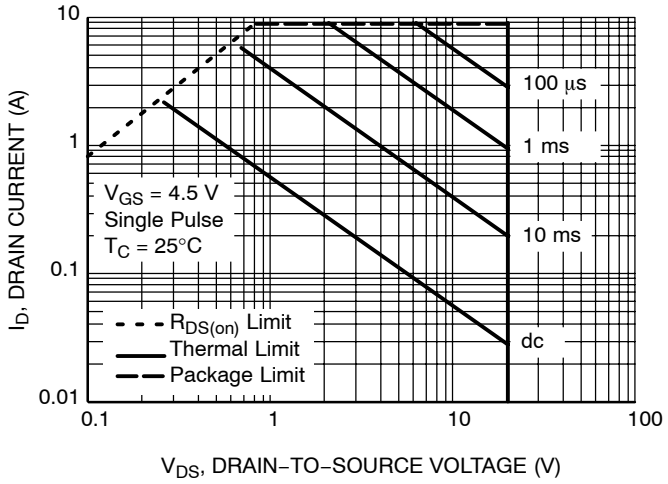


Figure 10. Maximum Rated Forward Biased Safe Operating Area

P−CHANNEL

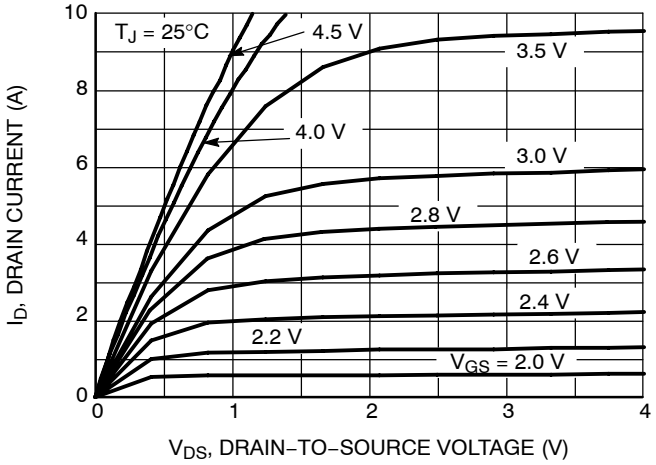


Figure 11. On−Region Characteristics

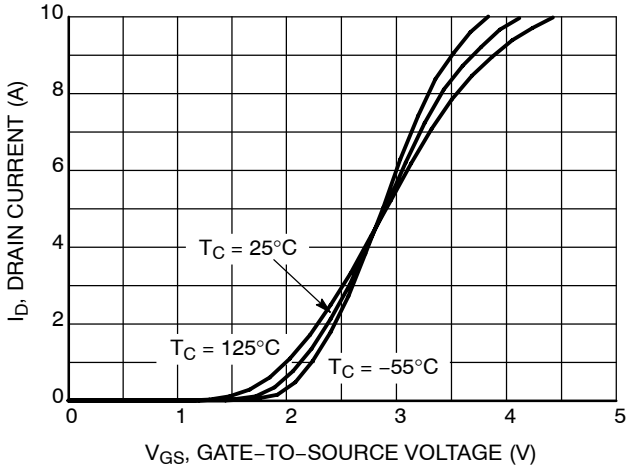


Figure 12. Transfer Characteristics

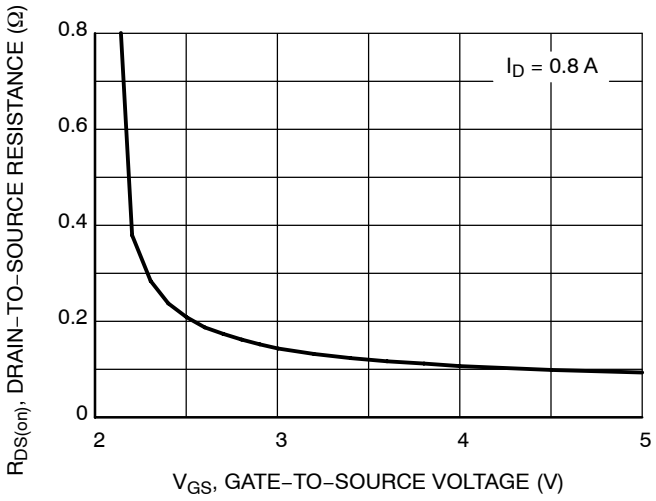


Figure 13. On−Resistance versus Gate−to−Source Voltage

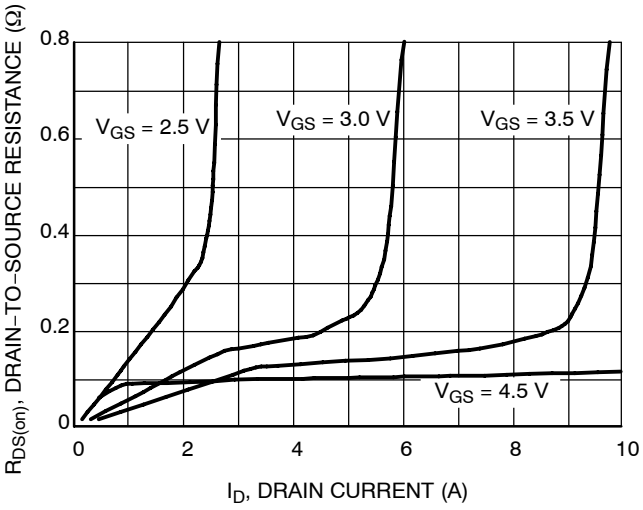


Figure 14. On−Resistance versus Drain Current and Gate Voltage

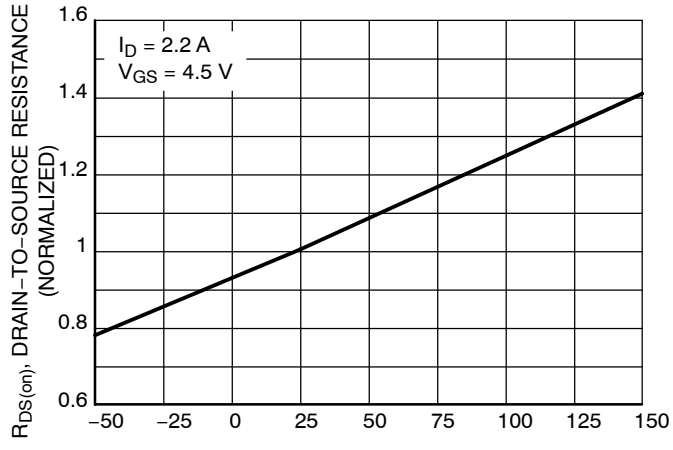


Figure 15. On−Resistance Variation with Temperature

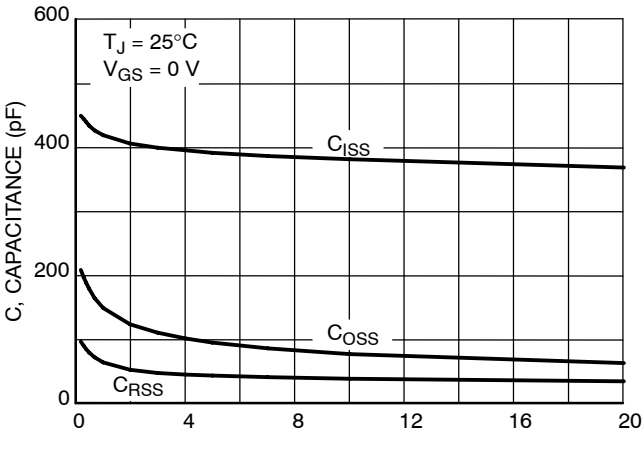


Figure 16. Capacitance Variation

P−CHANNEL

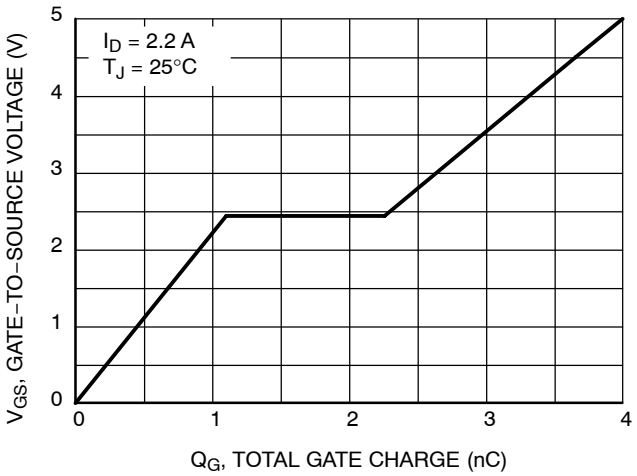


Figure 17. Gate−to−Source and Drain−to−Source Voltage versus Total Charge

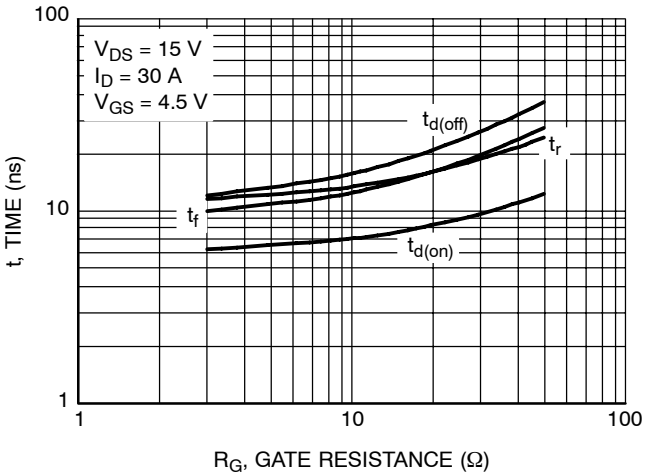


Figure 18. Resistive Switching Time Variation versus Gate Resistance

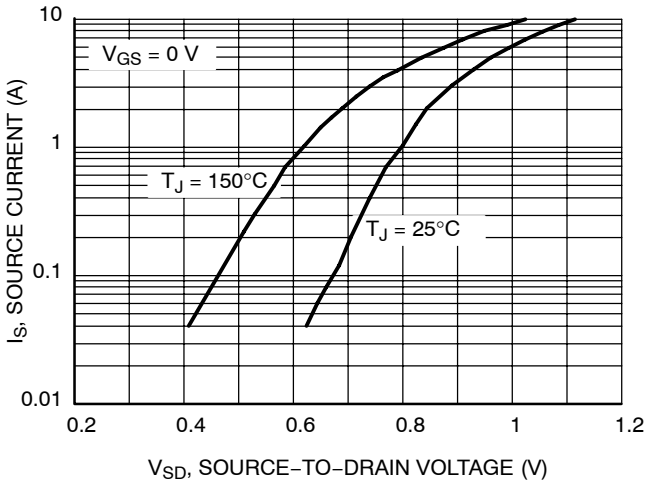


Figure 19. Diode Forward Voltage versus Current

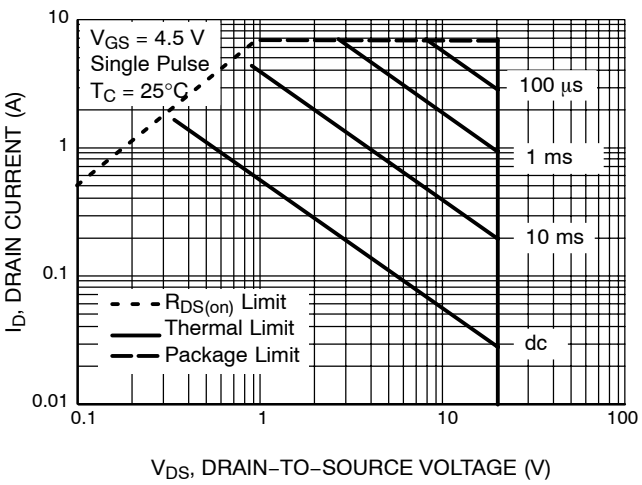


Figure 20. Maximum Rated Forward Biased Safe Operating Area

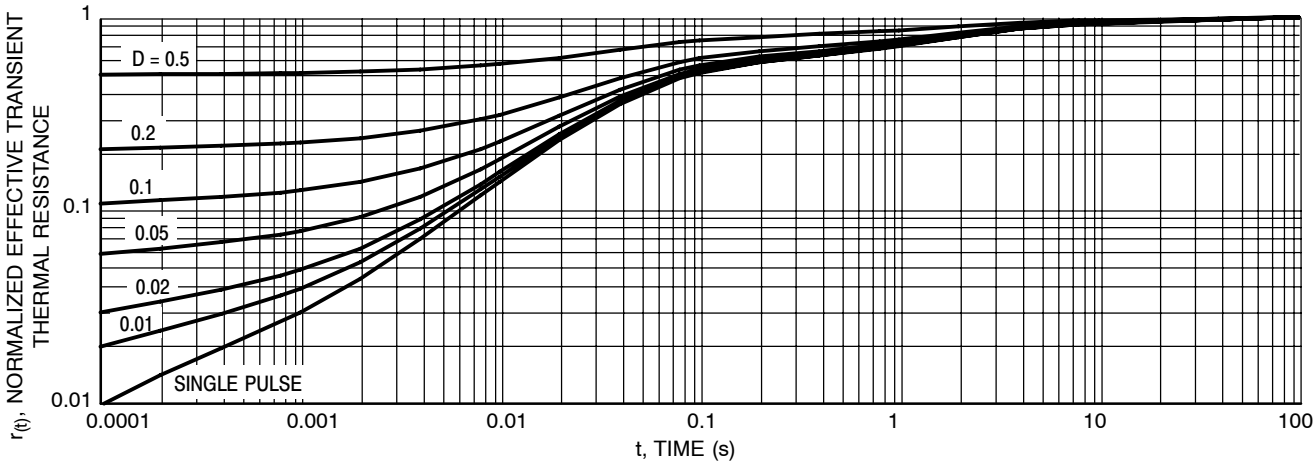


Figure 21. Thermal Response

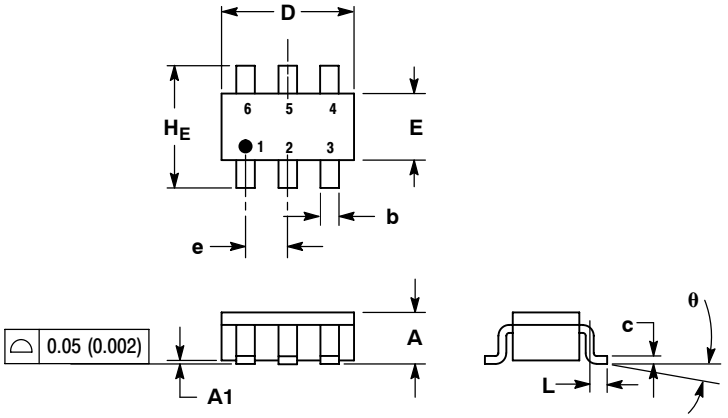
ORDERING INFORMATION

Device	Package	Shipping†
NTGD3122CT1G	TSOP6 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

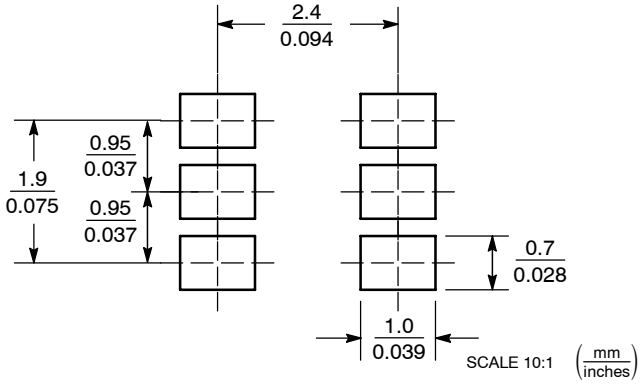
TSOP−6
CASE 318G−02
ISSUE S



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.38	0.50	0.010	0.014	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
L	0.20	0.40	0.60	0.008	0.016	0.024
H_E	2.50	2.75	3.00	0.099	0.108	0.118
θ	0°	–	10°	0°	–	10°

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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Fax: 480−829−7709 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

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2−9−1 Kamimeguro, Meguro−ku, Tokyo, Japan 153−0051
Phone: 81−3−5773−3850

ON Semiconductor Website: http://onsemi.com

Order Literature: http://www.onsemi.com/litorder

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