

# NTLMS4502N

## Advance Information Power MOSFET

### 17 A, 24 V N-Channel SO-8 Leadless

The SO-8LL (Leadless) package uses the power QFN package technology. It's footprint matches that of the standard SO-8 single die device. This Leadless SO-8 package provides low parasitic inductance compared to the standard SO-8 package allowing for higher frequency operation.

#### Features

- Planar HD3E Process for Fast Switching Performance
- Low  $R_{DS(on)}$  to Minimize Conduction Loss
- Low  $C_{iss}$  to Minimize Driver Loss
- Low Gate Charge
- Surface Mount
- Fast Switching

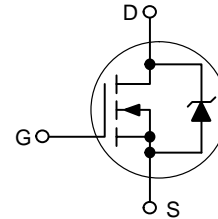
#### Product Summary

Symbol	Value
$V_{DS}$	24 V
$R_{DS(on)}$ @ 10 V	8 m $\Omega$
$Q_g$	8 nC
$I_D$	17 A
$Q_{gd}$	3 nC

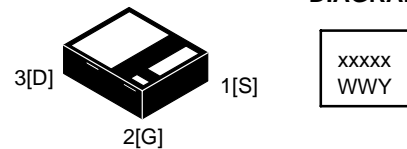


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#### MARKING DIAGRAM



#### SO-8 Leadless CASE 751S

xxxxx = Specific Device Code  
Y = Year  
WW = Work Week

#### PIN ASSIGNMENT

PIN	FUNCTION
1	S – SOURCE
2	G – GATE
3	D – DRAIN

#### ORDERING INFORMATION

Device	Package	Shipping
NTLMS4502N	SO-8 Leadless	2500 Tape & Reel

This document contains information on a new product. Specifications and information herein are subject to change without notice.

# NTLMS4502N

## MAXIMUM RATINGS (T<sub>J</sub> = 25°C Unless otherwise specified)

Parameter	Symbol	Value	Units
Drain-to-Source Voltage	V <sub>DSS</sub>	24	V <sub>dc</sub>
Gate-to-Source Voltage Continuous	V <sub>GS</sub>	±20	V <sub>dc</sub>
Drain Current	Continuous @ T <sub>A</sub> = 25°C (Note 1)	I <sub>D</sub>	12 A
	Continuous @ T <sub>A</sub> = 25°C (Note 2)	I <sub>DM</sub>	17 A
	Single Pulse (t <sub>p</sub> = 10 μs) (Note 4)	I <sub>DM</sub>	40 A
Maximum Power Dissipation (Steady State) @ T <sub>A</sub> = 25°C (Note 1)	P <sub>D</sub>	2.3	W
	Single Pulse (t <sub>p</sub> = 10 Secs) T <sub>A</sub> = 25°C (Note 2)	P <sub>D</sub>	5.0
Operating and Storage Temperature	T <sub>J</sub> and T <sub>stg</sub>	-55 to 150	°C
Single Pulse Drain-to Source Avalanche Energy – Starting T <sub>J</sub> = 25°C	E <sub>AS</sub>	220	mJ
Thermal Resistance	Junction-to-Ambient (Note 1)	R <sub>θJA</sub>	55 °C/W
	Junction-to-Ambient (Note 2)	R <sub>θJA</sub>	25
	Junction-to-Ambient (Note 3)	R <sub>θJA</sub>	110
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 Secs	T <sub>L</sub>	260	°C

1. When surface mounted to an FR4 board using 1" pad size, (Cu Area 1.127 in<sup>2</sup>).
2. 1" pad (Cu Area 0.911 in<sup>2</sup>), t < 10 sec.
3. When surface mounted to an FR4 board using minimum recommended pad size, (Cu Area 0.412 in<sup>2</sup>).
4. Chip current capability limited by package.

# NTLMS4502N

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C Unless otherwise specified)

Characteristics	Symbol	Min	Typ	Max	Unit	
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Breakdown Voltage (Note 5) (V <sub>GS</sub> = 0 V <sub>dc</sub> , I <sub>D</sub> = 250 μA <sub>dc</sub> ) Temperature Coefficient (Positive)	V(br) <sub>DSS</sub>	24 –	28 25	– –	V <sub>dc</sub> mV/°C	
Zero Gate Voltage Drain Current (V <sub>DS</sub> = 20 V <sub>dc</sub> , V <sub>GS</sub> = 0 V <sub>dc</sub> ) (V <sub>DS</sub> = 20 V <sub>dc</sub> , V <sub>GS</sub> = 0 V <sub>dc</sub> , T <sub>J</sub> = 150 °C)	I <sub>DSS</sub>	– –	– –	0.8 10	μA <sub>dc</sub>	
Gate-Body Leakage Current (V <sub>GS</sub> = ±20 V <sub>dc</sub> , V <sub>DS</sub> = 0 V <sub>dc</sub> )	I <sub>GSS</sub>	–	–	±100	nA <sub>dc</sub>	
<b>ON CHARACTERISTICS</b> (Note 5)						
Gate Threshold Voltage (Note 5) (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA <sub>dc</sub> ) Threshold Temperature Coefficient (Negative)	V <sub>GS(th)</sub>	1.0 –	1.5 –4.0	2.0 –	V <sub>dc</sub> mV/°C	
Static Drain-to-Source On-Resistance (Note 5) V <sub>GS</sub> = 10 V <sub>dc</sub> , I <sub>D</sub> = 17 A <sub>dc</sub> V <sub>GS</sub> = 4.5 V <sub>dc</sub> , I <sub>D</sub> = 15 A <sub>dc</sub>	R <sub>DS(on)</sub>	– –	8.0 12	10.8 14.8	mΩ	
Forward Transconductance (Note 5) (V <sub>DS</sub> = 10 V <sub>dc</sub> , I <sub>D</sub> = 17 A <sub>dc</sub> )	g <sub>FS</sub>	–	20	–	Mhos	
<b>DYNAMIC CHARACTERISTICS</b>						
Input Capacitance	(V <sub>DS</sub> = 20 V <sub>dc</sub> , V <sub>GS</sub> = 0 V, f = 1 MHz)	C <sub>iss</sub>	–	1150	1190	pF
Output Capacitance		C <sub>oss</sub>	–	435	460	
Transfer Capacitance		C <sub>rss</sub>	–	110	25	
<b>SWITCHING CHARACTERISTICS</b> (Note 6)						
Turn-On Delay Time	(V <sub>GS</sub> = 10 V <sub>dc</sub> , V <sub>DD</sub> = 15 V <sub>dc</sub> , I <sub>D</sub> = 17 A <sub>dc</sub> , R <sub>G</sub> = 2.5 Ω)	t <sub>d(on)</sub>	–	7	9	ns
Rise Time		t <sub>r</sub>	–	21	25	
Turn-Off Delay Time		t <sub>d(off)</sub>	–	20	22	
Fall Time		t <sub>f</sub>	–	3.5	5	
Gate Charge	(V <sub>GS</sub> = 4.5 V <sub>dc</sub> , I <sub>D</sub> = 17 A <sub>dc</sub> , V <sub>ds</sub> = 10 V)	Q <sub>T(g)</sub>	–	8	9.5	nC
		Q <sub>1(gs)</sub>	–	2.0	–	
		Q <sub>2(gd)</sub>	–	3.0	–	
		Q <sub>sw</sub>	–	TBD	–	
		Q <sub>oss</sub>	–	TBD	–	
<b>SOURCE-DRAIN DIODE CHARACTERISTICS</b>						
Forward On-Voltage	(I <sub>S</sub> = 8 A <sub>dc</sub> , V <sub>GS</sub> = 0 V <sub>dc</sub> ) (Note 5) (I <sub>S</sub> = 1.5 A <sub>dc</sub> , V <sub>GS</sub> = 0 V <sub>dc</sub> , T <sub>J</sub> = 150°C)	V <sub>SD</sub>	–	0.95 0.8	1.2 –	V <sub>dc</sub>
Reverse Recovery Time		(I <sub>S</sub> = 8 A <sub>dc</sub> , V <sub>GS</sub> = 0 V <sub>dc</sub> , di <sub>S</sub> /dt = 100 A/μs) (Note 5)	t <sub>rr</sub>	–	33	45
	t <sub>a</sub>		–	15	–	
	t <sub>b</sub>		–	18	–	
Reverse Recovery Stored Charge		Q <sub>RR</sub>	–	0.025	–	μC

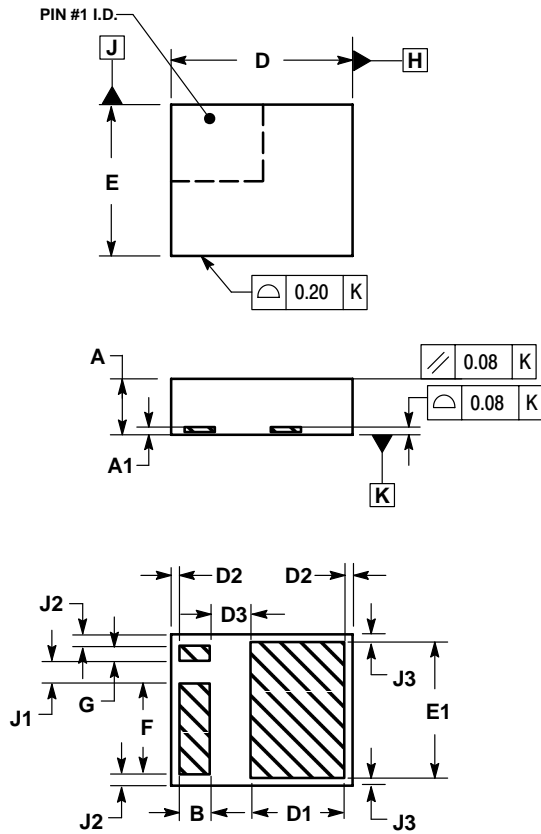
5. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

6. Switching characteristics are independent of operating junction temperatures.

# NTLMS4502N


## PACKAGE DIMENSIONS

SO-8 Leadless  
CASE 751S-02  
ISSUE A



- NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETER.

DIM	MILLIMETERS	
	MIN	MAX
A	1.750	1.950
A1	0.254 REF	
B	0.900	1.100
D	6.000 BSC	
D1	3.046	3.246
D2	0.154	0.354
D3	1.246	1.446
E	5.000 BSC	
E1	4.392	4.592
F	2.940	3.140
G	0.400	0.600
J1	0.680	0.880
J2	0.250	0.450
J3	0.154	0.354

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