NTLMS4502N

Advance Information

Power MOSFET

17 A, 24 V N–Channel SO–8 Leadless

The SO–8LL (Leadless) package uses the power QFN package technology. It's footprint matches that of the standard SO–8 single die device. This Leadless SO–8 package provides low parasitic inductance compared to the standard SO–8 package allowing for higher frequency operation.

Features

- Planar HD3E Process for Fast Switching Performance
- Low R_{DSon} to Minimize Conduction Loss
- Low C_{iss} to Minimize Driver Loss
- Low Gate Charge
- Surface Mount
- Fast Switching

Product Summary

Symbol	Value
V_{DS}	24 V
R_{DSon} @ 10 V	8 mΩ
Q_g	8 nC
I_D	17 A
Q_{gd}	3 nC

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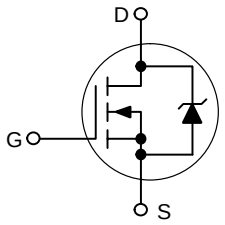
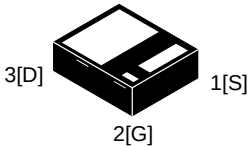


MARKING DIAGRAM



SO–8 Leadless
CASE 751S

xxxxx = Specific Device Code
Y = Year
WW = Work Week

PIN ASSIGNMENT

PIN	FUNCTION
1	S – SOURCE
2	G – GATE
3	D – DRAIN

ORDERING INFORMATION

Device	Package	Shipping
NTLMS4502N	SO–8 Leadless	2500 Tape & Reel

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS (T_J = 25°C Unless otherwise specified)

Parameter		Symbol	Value	Units
Drain–to–Source Voltage		V_{DSS}	24	V_{dc}
Gate–to–Source Voltage	Continuous	V_{GS}	±20	V_{dc}
Drain Current	Continuous @ T_A = 25°C (Note 1) Continuous @ T_A = 25°C (Note 2) Single Pulse (t_p = 10 μs) (Note 4)	I_D I_{DM} I_{DM}	12 17 40	A A A
Maximum Power Dissipation (Steady State) @ T_A = 25°C (Note 1) Single Pulse (t_p = 10 Secs) T_A = 25°C (Note 2)		P_D P_D	2.3 5.0	W W
Operating and Storage Temperature		T_J and T_{stg}	–55 to 150	°C
Single Pulse Drain–to Source Avalanche Energy – Starting T_J = 25°C		E_{AS}	220	mJ
Thermal Resistance	Junction–to–Ambient (Note 1) Junction–to–Ambient (Note 2) Junction–to–Ambient (Note 3)	$R_{\theta JA}$ $R_{\theta JA}$ $R_{\theta JA}$	55 25 110	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8” from case for 10 Secs		T_L	260	°C

1. When surface mounted to an FR4 board using 1” pad size, (Cu Area 1.127 in^2).
2. 1” pad (Cu Area 0.911 in^2), t < 10 sec.
3. When surface mounted to an FR4 board using minimum recommended pad size, (Cu Area 0.412 in^2).
4. Chip current capability limited by package.

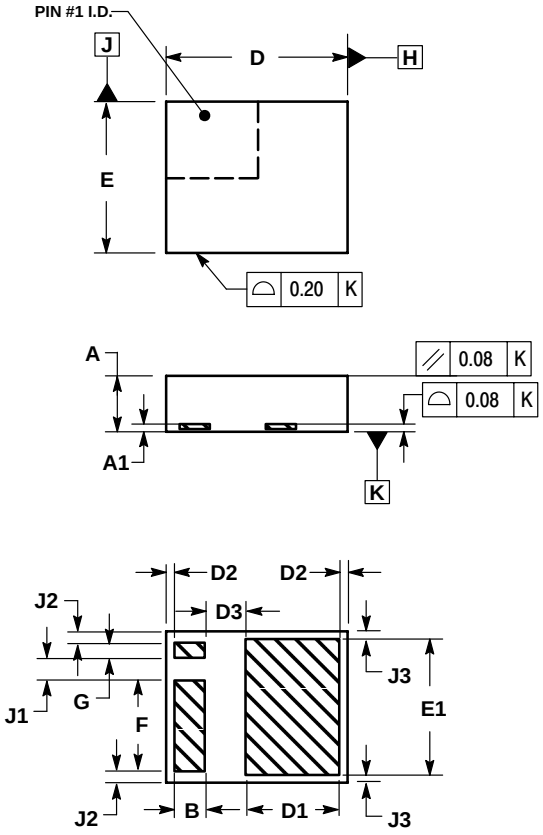
ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless otherwise specified)

Characteristics		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (Note 5) (V_{GS} = 0 V_{dc}, I_D = 250 μA_{dc}) Temperature Coefficient (Positive)		$V(br)_{DSS}$	 24 –	 28 25	 – –	 V_{dc} mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 20 V_{dc}, V_{GS} = 0 V_{dc}) (V_{DS} = 20 V_{dc}, V_{GS} = 0 V_{dc}, T_J = 150 °C)		I_{DSS}	 – –	 – –	 0.8 10	μA_{dc}
Gate–Body Leakage Current	(V_{GS} = ±20 V_{dc}, V_{DS} = 0 V_{dc})	I_{GSS}	–	–	±100	nA_{dc}
ON CHARACTERISTICS (Note 5)						
Gate Threshold Voltage (Note 5) (V_{DS} = V_{GS}, I_D = 250 μA_{dc}) Threshold Temperature Coefficient (Negative)		V_{GS}(th)	 1.0 –	 1.5 –4.0	 2.0 –	 V_{dc} mV/°C
Static Drain–to–Source On–Resistance (Note 5) V_{GS} = 10 V_{dc}, I_D = 17 A_{dc} V_{GS} = 4.5 V_{dc}, I_D = 15 A_{dc}		R_{DS}(on)	 – –	 8.0 12	 10.8 14.8	mΩ
Forward Transconductance (Note 5)	(V_{DS} = 10 V_{dc}, I_D = 17 A_{dc})	g_{FS}	–	20	–	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 20 V_{dc}, V_{GS} = 0 V, f = 1 MHz)	C_{iss}	–	1150	1190	pF
Output Capacitance		C_{oss}	–	435	460	
Transfer Capacitance		C_{rss}	–	110	25	
SWITCHING CHARACTERISTICS (Note 6)						
Turn–On Delay Time	(V_{GS} = 10 V_{dc}, V_{DD} = 15 V_{dc}, I_D = 17 A_{dc}, R_G = 2.5 Ω)	t_d(on)	–	7	9	ns
Rise Time		t_r	–	21	25	
Turn–Off Delay Time		t_d(off)	–	20	22	
Fall Time		tf	–	3.5	5	
Gate Charge	(V_{GS} = 4.5 V_{dc}, I_D = 17 A_{dc}, Vds = 10 V)	$Q_{T(g)}$	–	8	9.5	nC
		$Q_{1(gs)}$	–	2.0	–	
		$Q_{2(gd)}$	–	3.0	–	
		Q_{sw}	–	TBD	–	
		Q_{oss}	–	TBD	–	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 8 A_{dc}, V_{GS} = 0 V_{dc}) (Note 5) (I_S = 1.5 A_{dc}, V_{GS} = 0 V_{dc}, T_J = 150°C)	V_{SD}	–	0.95 0.8	1.2 –	V_{dc}
Reverse Recovery Time	(I_S = 8 A_{dc}, V_{GS} = 0 V_{dc}, dI_S/dt = 100 A/μs) (Note 5)	t_{rr}	–	33	45	ns
		t_a	–	15	–	
		t_b	–	18	–	
Reverse Recovery Stored Charge		Q_{RR}	–	0.025	–	μC

5. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.
6. Switching characteristics are independent of operating junction temperatures.

PACKAGE DIMENSIONS

SO–8 Leadless
CASE 751S–02
ISSUE A



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS	
DIM	MIN	MAX
A	1.750	1.950
A1	0.254 REF	
B	0.900	1.100
D	6.000 BSC	
D1	3.046	3.246
D2	0.154	0.354
D3	1.246	1.446
E	5.000 BSC	
E1	4.392	4.592
F	2.940	3.140
G	0.400	0.600
J1	0.680	0.880
J2	0.250	0.450
J3	0.154	0.354

PUBLICATION ORDERING INFORMATION

Literature Fulfillment:
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