

MC10E337, MC100E337

5V ECL 3-Bit Scannable Registered Bus Transceiver

The MC10E/100E337 is a 3-bit registered bus transceiver with scan. The bus outputs (BUS0–BUS2) are specified for driving a 25 Ω bus; the receive outputs (Q0–Q2) are specified for 50 Ω . The bus outputs feature a normal HIGH level (V_{OH}) and a cutoff LOW level — when LOW, the outputs go to –2.0 V and the output emitter-follower is “off”, presenting a high impedance to the bus. The bus outputs also feature edge slow-down capacitors.

Both drive and receive sides feature the same logic, including a loopback path to hold data. The $\overline{\text{HOLD/LOAD}}$ function is controlled by Transmit Enable (TEN) and Receive Enable (REN) on the transmit and receive sides respectively, with a HIGH selecting LOAD. Note that the implementation of the E337 Receive Enable differs from that of the E336.

A synchronous bus enable (SBUSEN) is provided for normal, non-scan operation. The asynchronous bus disable ($\overline{\text{ABUSDIS}}$) disables the bus immediately for scan mode.

The $\overline{\text{SYNCEN}}$ input is provided for flexibility when re-enabling the bus after disabling with $\overline{\text{ABUSDIS}}$, allowing either synchronous or asynchronous re-enabling. An alternative use is asynchronous-only operation with $\overline{\text{ABUSDIS}}$, in which case $\overline{\text{SYNCEN}}$ is tied LOW, or left open. $\overline{\text{SYNCEN}}$ is implemented as an overriding SET control (active-LOW) to the enable flip-flop.

Scan mode is selected by a HIGH at the SCAN input. Scan input data is shifted in through S_IN and output data appears at the Q2 output.

All registers are clocked on the positive transition of CLK. Additional lead-frame grounding is provided through the Ground pins (GND) which should be connected to 0V. The GND pins are not electrically connected to the chip.

The 100 Series contains temperature compensation.

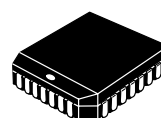
- Scannable Version of E336
 - 25 Ω Cutoff Bus Outputs
 - 50 Ω Receiver Outputs
 - Scannable Registers
 - Sync. and Async. Bus Enables
 - Non-inverting Data Path
 - 1500 ps Max. Clock to Bus (Data Transmit)
 - 1000 ps Max. Clock to Q (Data Receive)
 - Bus Outputs Feature Internal Edge Slow-Down Capacitors
 - Additional Package Ground Pins
 - PECL Mode Operating Range: V_{CC} = 4.2 V to 5.7 V with V_{EE} = 0 V
 - NECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = –4.2 V to –5.7 V
 - Internal Input Pulldown Resistors
 - ESD Protection: > 1 KV HBM, > 75 V MM
 - Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
 - Moisture Sensitivity Level 1
- For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”, Oxygen Index 28 to 34
 - Transistor Count = 471 devices



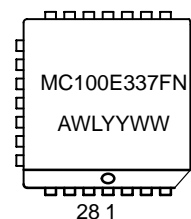
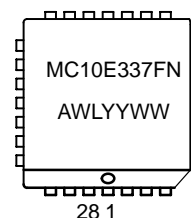
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MARKING DIAGRAMS



PLCC–28
FN SUFFIX
CASE 776



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

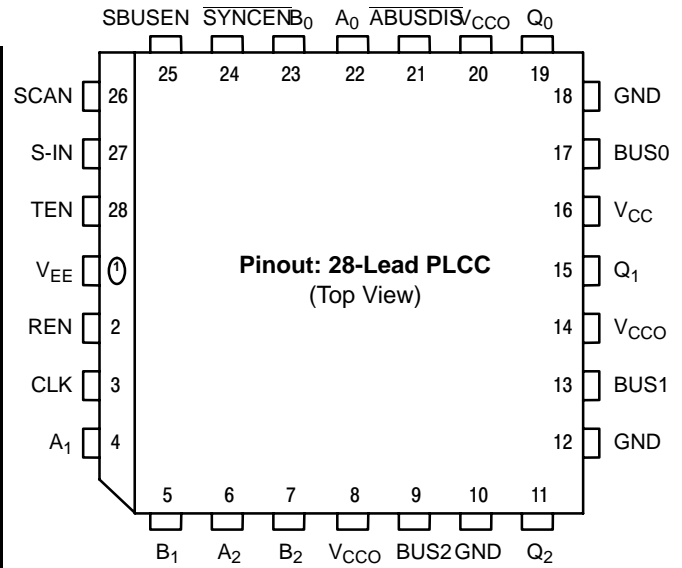
Device	Package	Shipping
MC10E337FN	PLCC–28	37 Units/Rail
MC10E337FNR2	PLCC–28	500 Units/Reel
MC100E337FN	PLCC–28	37 Units/Rail
MC100E337FNR2	PLCC–28	500 Units/Reel

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PIN DESCRIPTION

PIN	FUNCTION
A ₀ – A ₂	ECL Data Inputs A
B ₀ – B ₂	ECL Data Inputs B
S-IN	ECL Serial (Scan) Data Input
TEN, REN	HOLD/ \overline{LOAD} Controls
SCAN	ECL Scan Control
$\overline{ABUSDIS}$	ECL Asynchronous Bus Disable
SBUSEN	ECL Synchronous Bus Enable
\overline{SYNCEN}	ECL Synchronous Enable Control
CLK	ECL Clock
BUS0 – BUS2	ECL 25 Ω Cutoff Bus Outputs
Q ₀ – Q ₂	ECL Receive Data Outputs (Q ₂ serves as SCAN_OUT in scan mode)
V _{CC} , V _{CCO}	Positive Supply
V _{EE}	Negative Supply
GND	Ground

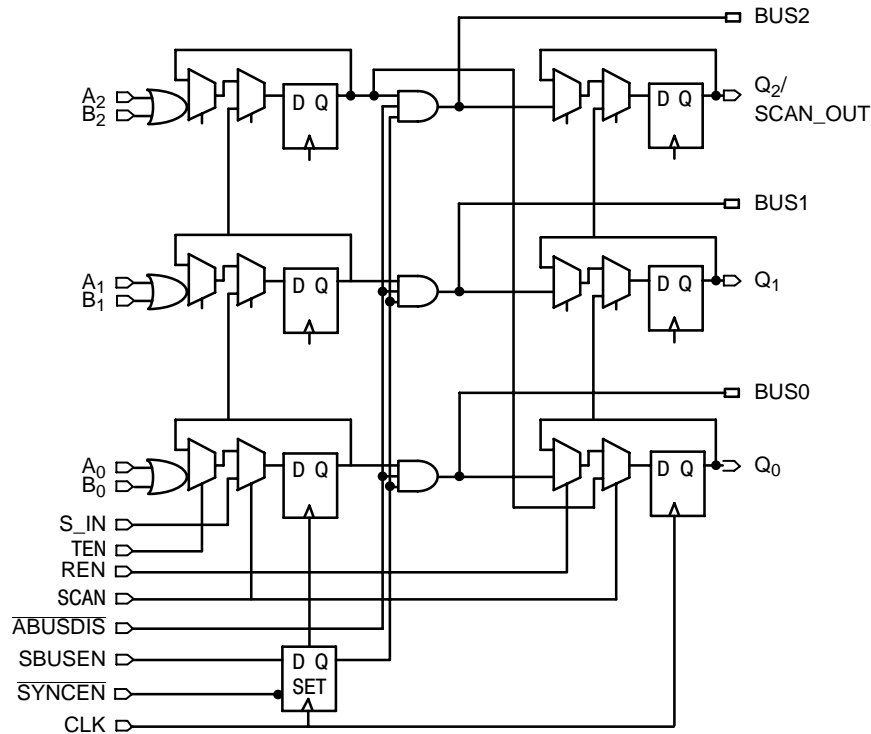
LOGIC DIAGRAM AND PINOUT ASSIGNMENT



* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

LOGIC DIAGRAM



MC10E337, MC100E337

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V _{CC}	PECL Mode Power Supply	V _{EE} = 0 V		8	V
V _{EE}	NECL Mode Power Supply	V _{CC} = 0 V		−8	V
V _I	PECL Mode Input Voltage	V _{EE} = 0 V	V _I ≤ V _{CC}	6	V
	NECL Mode Input Voltage	V _{CC} = 0 V	V _I ≥ V _{EE}	−6	V
I _{out}	Output Current	Continuous Surge		50	mA
				100	mA
T _A	Operating Temperature Range			0 to +85	°C
T _{stg}	Storage Temperature Range			−65 to +150	°C
θ _{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ _{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V _{EE}	PECL Operating Range			4.2 to 5.7	V
	NECL Operating Range			−5.7 to −4.2	V
T _{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx} = 5.0 V; V_{EE} = 0.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I _{EE}	Power Supply Current		145	174		145	174		145	174	mA
V _{OH}	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V _{OL}	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V _{IH}	Input HIGH Voltage	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V _{IL}	Input LOW Voltage	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
V _{CUT}	Cut-off Output Voltage (Note 2.)	2.9		2.97	2.9		2.97	2.9		2.97	V
I _{IH}	Input HIGH Current			150			150			150	μA
I _{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / −0.06 V.

2. Outputs are terminated through a 50 ohm resistor to V_{CC} −2.10 volts.

10E SERIES NECL DC CHARACTERISTICS V_{CCx} = 0.0 V; V_{EE} = −5.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I _{EE}	Power Supply Current		145	174		145	174		145	174	mA
V _{OH}	Output HIGH Voltage (Note 2.)	−1020	−930	−840	−980	−895	−810	−910	−815	−720	mV
V _{OL}	Output LOW Voltage (Note 2.)	−1950	−1790	−1630	−1950	−1790	−1630	−1950	−1773	−1595	mV
V _{IH}	Input HIGH Voltage	−1170	−1005	−840	−1130	−970	−810	−1060	−890	−720	mV
V _{IL}	Input LOW Voltage	−1950	−1715	−1480	−1950	−1715	−1480	−1950	−1698	−1445	mV
V _{CUT}	Cut-off Output Voltage (Note 2.)	2.9		2.97	2.9		2.97	2.9		2.97	V
I _{IH}	Input HIGH Current			150			150			150	μA
I _{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / −0.06 V.

2. Outputs are terminated through a 50 ohm resistor to V_{CC} −2.10 volts.

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100E SERIES PECL DC CHARACTERISTICS $V_{CCx}=5.0\text{ V}$; $V_{EE}=0.0\text{ V}$ (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		145	174		145	174		167	200	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
V_{CUT}	Cut-off Output Voltage (Note 2.)	2.9		2.97	2.9		2.97	2.9		2.97	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.46 V / -0.8 V.

2. Outputs are terminated through a 50 ohm resistor to V_{CC} -2.10 volts.

100E SERIES NECL DC CHARACTERISTICS $V_{CCx}=0.0\text{ V}$; $V_{EE}=-5.0\text{ V}$ (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		145	174		145	174		167	200	mA
V_{OH}	Output HIGH Voltage (Note 2.)	-1025	-950	-880	-1025	-950	-880	-1025	-950	-880	mV
V_{OL}	Output LOW Voltage (Note 2.)	-1810	-1705	-1620	-1810	-1745	-1620	-1810	-1740	-1620	mV
V_{IH}	Input HIGH Voltage	-1165	-950	-880	-1165	-880	-880	-1165	-880	-880	mV
V_{IL}	Input LOW Voltage	-1810	-1700	-1475	-1810	-1475	-1475	-1810	-1475	-1475	mV
V_{CUT}	Cut-off Output Voltage (Note 2.)	2.9		2.97	2.9		2.97	2.9		2.97	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.46 V / -0.8 V.

2. Outputs are terminated through a 50 ohm resistor to V_{CC} -2.10 volts.

AC CHARACTERISTICS $V_{CCx}=5.0\text{ V}$; $V_{EE}=0.0\text{ V}$ or $V_{CCx}=0.0\text{ V}$; $V_{EE}=-5.0\text{ V}$ (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output Clk to Q Clk to BUS ABUSDIS SYNCSN	450 800 500 800		1000 1800 1500 1800	450 800 500 800		1000 1800 1500 1800	450 800 500 800		1000 1800 1500 1800	ps
t_s	Setup Time BUS SBUSEN Data, S-IN TEN, REN, SCAN	350 100 400 550			350 100 400 550			350 100 400 550			ps
t_h	Hold Time BUS SBUSEN Data, S-IN TEN, REN, SCAN	350 500 350 200			350 500 350 200			350 500 350 200			ps
t_{PW}	Minimum Pulse Width Clk	400			400			400			ps
t_{JITTER}	Cycle-to-Cycle Jitter		TBD			TBD			TBD		ps
t_r t_f	Rise/Fall Times 20 - 80% (Qn) 20 - 80% (BUSn Rise) 20 - 80% (BUSn Fall)	300 500 300		800 1000 800	300 500 300		800 1000 800	300 500 300		800 1000 800	ps

1. 10 Series: V_{EE} can vary +0.46 V / -0.06 V.

100 Series: V_{EE} can vary +0.46 V / -0.8 V.

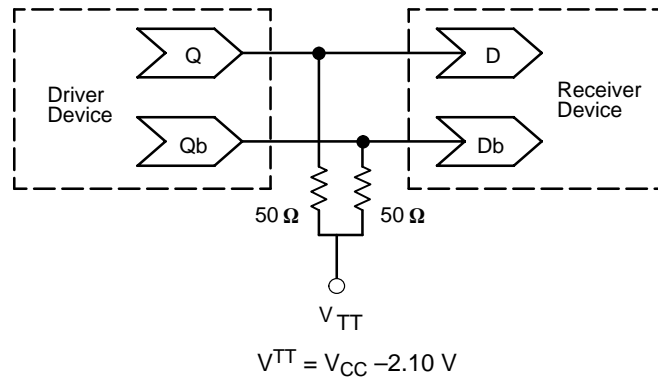


Figure 1. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020 – Termination of ECL Logic Devices.)

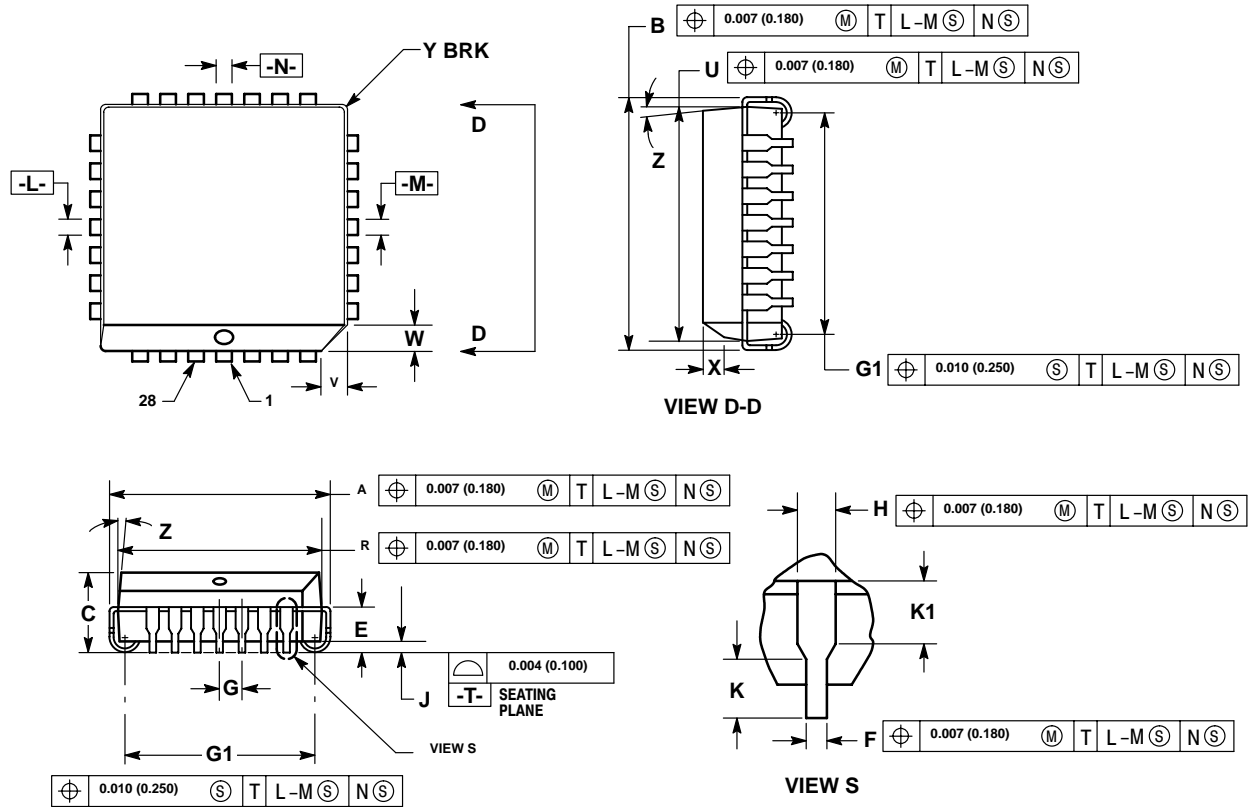
Resource Reference of Application Notes

- AN1404** – ECLinPS Circuit Performance at Non-Standard V_{IH} Levels
- AN1405** – ECL Clock Distribution Techniques
- AN1406** – Designing with PECL (ECL at +5.0 V)
- AN1503** – ECLinPS I/O SPICE Modeling Kit
- AN1504** – Metastability and the ECLinPS Family
- AN1568** – Interfacing Between LVDS and ECL
- AN1596** – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
- AN1650** – Using Wire-OR Ties in ECLinPS Designs
- AN1672** – The ECL Translator Guide
- AND8001** – Odd Number Counters Design
- AND8002** – Marking and Date Codes
- AND8020** – Termination of ECL Logic Devices

MC10E337, MC100E337

PACKAGE DIMENSIONS

PLCC-28
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 776-02
ISSUE E



Notes

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