

MC100ELT23

5V Dual Differential PECL to TTL Translator

The MC100ELT23 is a dual differential PECL to TTL translator. Because PECL (Positive ECL) levels are used, only +5 V and ground are required. The small outline 8-lead package and the dual gate design of the ELT23 makes it ideal for applications which require the translation of a clock and a data signal.

The PECL inputs are differential; therefore, the MC100ELT23 can accept any standard differential PECL input referenced from a V_{CC} of 5.0 V.

- 3.5 ns Typical Propagation Delay
- 24 mA TTL Outputs
- Flow Through Pinouts
- ESD Protection: >2 KV HBM, > 400 V MM
- The 100 Series Contains Temperature Compensation
- Operating Range V_{CC} = 4.75 V to 5.25 V with GND = 0 V
- Internal Input Pulldown Resistors
- Q Output Will Default High with Inputs Left Open or < 1.3 V
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
- For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL-94 code V-0 @ 1/8", Oxygen Index 28 to 34
- Transistor Count = 91 devices

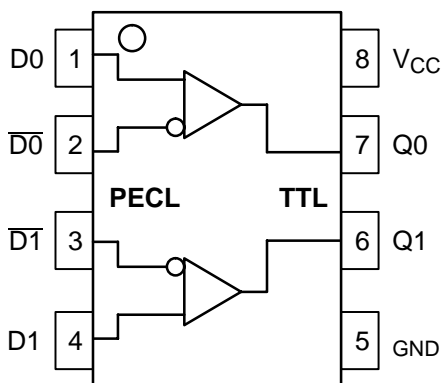


Figure 1. 8-Lead Pinout and Logic Diagram
(Top View)

PIN DESCRIPTION

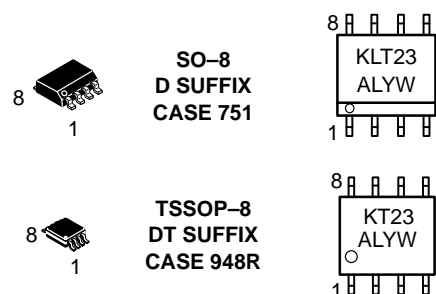
PIN	FUNCTION
Qn	TTL Outputs
Dn, \overline{Dn}	PECL Differential Inputs
V_{CC}	Positive Supply
GND	Ground



ON Semiconductor™

<http://onsemi.com>

MARKING DIAGRAMS*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100ELT23D	SO-8	98 Units / Rail
MC100ELT23DR2	SO-8	2500 / Reel
MC100ELT23DT	TSSOP-8	98 Units / Rail
MC100ELT23DTR2	TSSOP-8	2500 / Reel

MC100ELT23

MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V _{CC}	Power Supply	GND = 0 V		7	V
V _I	Input Voltage	GND = 0 V	V _I ≤ V _{CC}	0 to 6	V
T _A	Operating Temperature Range			−40 to +85	°C
T _{stg}	Storage Temperature Range			−65 to +150	°C
θ _{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W
θ _{JC}	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44	°C/W
θ _{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W
θ _{JC}	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44 ± 5%	°C/W
T _{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

PECL INPUT DC CHARACTERISTICS V_{CC}= 5.0 V; GND= 0.0 V (Note 2)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V _{IH}	Input HIGH Voltage (Single Ended)	3835		4120	3835		4120	3835		4120	mV
V _{IL}	Input LOW Voltage (Single Ended)	3190		3525	3190		3525	3190		3525	mV
V _{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3)	2.2		5.0	2.2		5.0	2.2		5.0	V
I _{IH}	Input HIGH Current			150			150			150	μA
I _{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

2. Input parameters vary 1:1 with V_{CC}. V_{CC} can vary ± 0.25 V.

3. V_{IHCMR} min varies 1:1 with GND, V_{IHCMR} max varies 1:1 with V_{CC}.

TTL OUTPUT DC CHARACTERISTICS V_{CC} = 4.75V to 5.25V; T_A = −40°C to 85°C

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V _{OH}	Output HIGH Voltage	I _{OH} = −3.0 mA	2.4		(Note 4)	V
V _{OL}	Output LOW Voltage	I _{OL} = 24 mA			0.5	V
I _{CCH}	Power Supply Current			23	33	mA
I _{CCL}	Power Supply Current			26	36	mA
I _{OS}	Output Short Circuit Current		−150		−60	mA

4. Max level is V_{CC}−0.7 V by design.

AC CHARACTERISTICS V_{CC}= 5.0 V; GND= 0.0 V (Note 5 and Note 6.)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f _{max}	Maximum Toggle Frequency		TBD			TBD			TBD		MHz
t _{JITTER}	Cycle-to-Cycle Jitter		TBD			TBD			TBD		ps
t _{PLH}	Propagation Delay @ 1.5 V C _L = 20 pF	2.0		5.5	2.0		5.5	2.0		5.5	ns
t _{PHL}	Propagation Delay @ 1.5 V C _L = 20 pF	2.0		5.5	2.0		5.5	2.0		5.5	ns
V _{PP}	Input Swing (Note 7)	200		1000	200		1000	200		1000	mV
t _r /t _f	Output Rise Time (10–90%) C _L = 20pF					1.6					ns
	Output Fall Time (10–90%) C _L = 20pF					1.1					ns

5. V_{CC} can vary ± 0.25 V.

6. All loading with 500 ohms to GND, C_L = 20 pF.

7. V_{PP}(min) is the minimum input swing for which AC parameters are guaranteed. The device has a DC gain of ≈40.

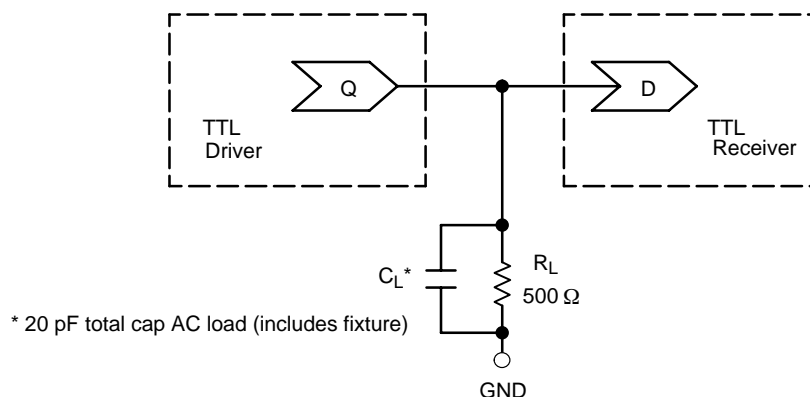


Figure 2. TTL Output Loading Used for Device Evaluation

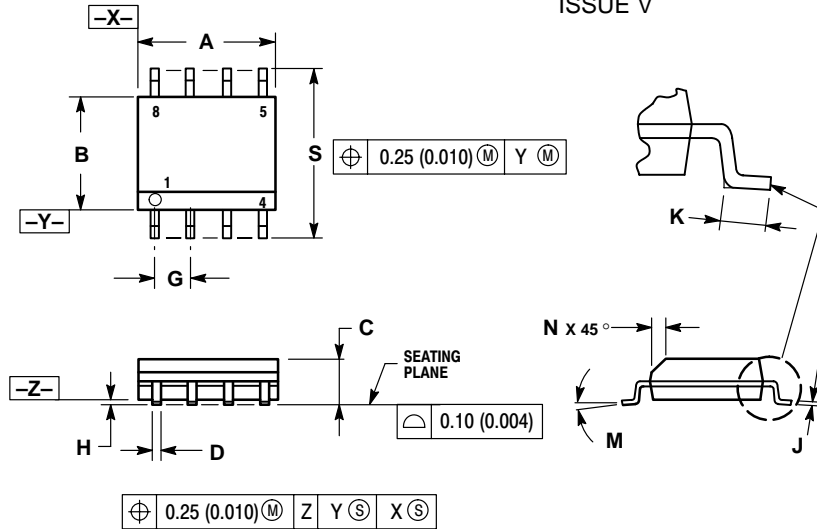
Resource Reference of Application Notes

- AN1404** – ECLinPS Circuit Performance at Non-Standard V_{IH} Levels
- AN1405** – ECL Clock Distribution Techniques
- AN1406** – Designing with PECL (ECL at +5.0 V)
- AN1503** – ECLinPS I/O SPICE Modeling Kit
- AN1504** – Metastability and the ECLinPS Family
- AN1560** – Low Voltage ECLinPS SPICE Modeling Kit
- AN1568** – Interfacing Between LVDS and ECL
- AN1596** – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
- AN1650** – Using Wire-OR Ties in ECLinPS Designs
- AN1672** – The ECL Translator Guide
- AND8001** – Odd Number Counters Design
- AND8002** – Marking and Date Codes
- AND8020** – Termination of ECL Logic Devices

MC100ELT23

PACKAGE DIMENSIONS

SO-8
D SUFFIX
 PLASTIC SOIC PACKAGE
 CASE 751-07
 ISSUE V



NOTES:

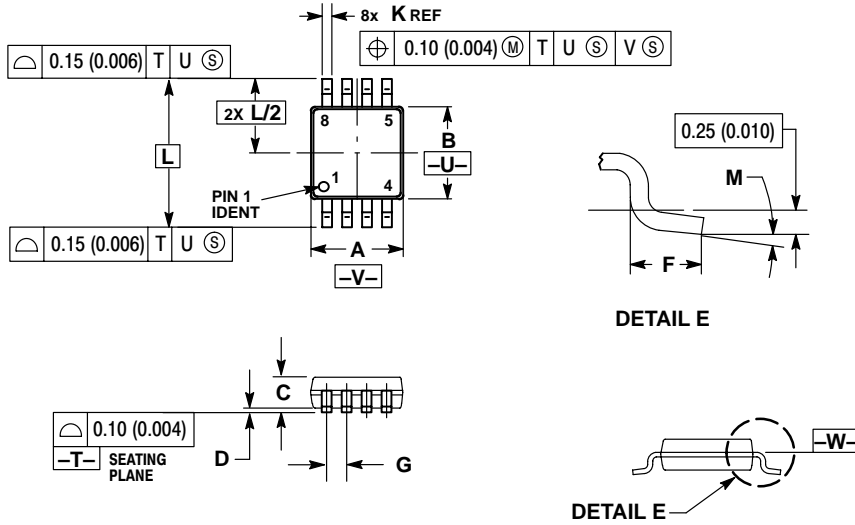
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

MC100ELT23

PACKAGE DIMENSIONS

TSSOP-8
DT SUFFIX
 PLASTIC TSSOP PACKAGE
 CASE 948R-02
 ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

Notes

Notes

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

PUBLICATION ORDERING INFORMATION

Literature Fulfillment:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

JAPAN: ON Semiconductor, Japan Customer Focus Center
4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-0031
Phone: 81-3-5740-2700
Email: r14525@onsemi.com

ON Semiconductor Website: <http://onsemi.com>

For additional information, please contact your local Sales Representative.