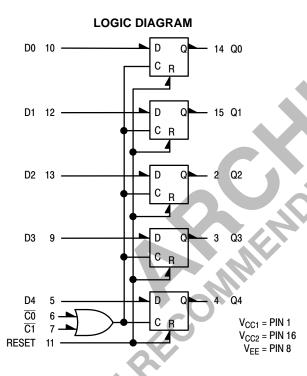
Quint Latch

The MC10175 is a high speed, low power quint latch. It features five D type latches with common reset and a common two-input clock. Data is transferred on the negative edge of the clock and latched on the positive edge. The two clock inputs are "OR"ed together.

Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information. The reset input is enabled only when the clock is in the high state.

- $P_D = 400 \text{ mW typ/pkg (No Load)}$
- $t_{pd} = 2.5$ ns typ (Data to Output)
- t_r , $t_f = 2.0$ ns typ (20%–80%)



TRUTH TABLE

| D | C 0 | C1 | Reset | Q _{n+1} |
|---|----------------|----|-------|------------------|
| L | 4 | L | Х | L |
| H | Ļ | L | Χ | Н |
| X | H | Χ | L | Qn |
| X | Χ | Н | L | Qn |
| X | Н | Χ | Н | L |
| X | X | Н | Н | L |



ON Semiconductor

http://onsemi.com





CDIP-16 L SUFFIX CASE 620





PDIP-16 P SUFFIX CASE 648





PLCC-20 FN SUFFIX CASE 775



A = Assembly Location

WL = Wafer Lot

YY = Year

WW = Work Week

DIP PIN ASSIGNMENT

| | 1 | $\overline{}$ | | 1 | |
|-------------------|---|---------------|----|---|------------------|
| V _{CC1} | | 1 | 16 | | V_{CC2} |
| Q2 | | 2 | 15 | | Q1 |
| Q3 | | 3 | 14 | | Q0 |
| Q4 | | 4 | 13 | | D2 |
| D4 | | 5 | 12 | | D1 |
| C0 | | 6 | 11 | | RESET |
| C1 | | 7 | 10 | | D0 |
| V_{EE} | | 8 | 9 | | D3 |
| | | | | | |

Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18 of the ON Semiconductor MECL Data Book (DL122/D).

ORDERING INFORMATION

| Device | Package | Shipping | | | | | |
|-----------|---------|-----------------|--|--|--|--|--|
| MC10175L | CDIP-16 | 25 Units / Rail | | | | | |
| MC10175P | PDIP-16 | 25 Units / Rail | | | | | |
| MC10175FN | PLCC-20 | 46 Units / Rail | | | | | |

ELECTRICAL CHARACTERISTICS

| | | Pin | Test Limits | | | | 1 | | | |
|----------------------------|--|----------|------------------|------------------|------------------|-------|------------------|------------------|------------------|-----|
| | | Under | - | 0°C | | +25°C | I | +85 | 1 | 4 |
| Characteristic | Symbol | Test | Min | Max | Min | Тур | Max | Min | Max | Uni |
| Power Supply Drain Current | I _E | 8 | | 107 | | 78 | 97 | | 107 | mAc |
| Input Current | I _{inH} | 6 7 | | 460 460 | | | 290 290 | | 290 290 | μAd |
| | | 10 | | 460 | | | 290 | | 290 | |
| | | 11 | | 1000 | | | 650 | | 650 | |
| | I _{inL} | All | 0.5 | | 0.5 | | | 0.3 | | μAd |
| Output Voltage Logic 1 | V _{OH} | 14 15 | -1.060 -1.060 | -0.890 -0.890 | -0.960 -0.960 | | -0.810 -0.810 | -0.890 -0.890 | -0.700 -0.700 | Vdo |
| Output Voltage Logic 0 | V _{OL} | 14 15 | -1.890 -1.890 | -1.675 -1.675 | -1.850 -1.850 | | -1.650 -1.650 | -1.825 -1.825 | -1.615 -1.615 | Vdd |
| Threshold Voltage Logic 1 | V _{OHA} | 14 | -1.080 | 1.073 | -0.980 | | 1.000 | -0.910 | 1.013 | Vdd |
| | | 15 | -1.080 | | -0.980 | | | -0.910 | 5 | |
| Threshold Voltage Logic 0 | V_{OLA} | 14 15 | | -1.655 -1.655 | | | -1.630 -1.630 | | -1.595 -1.595 | Vdo |
| Switching Times (50Ω Load) | | | | | | | | V | | ns |
| Data Input | t ₁₀₊₁₄₊ | 14 | 1.0 | 3.6 | 1.0 | | 3.5 | 1.0 | 3.6 | |
| | t ₁₀₋₁₄₋ | 14 | 1.0 | 3.6 | 1.0 | | 3.5 | 1.0 | 3.6 | |
| Clock Input | t ₆₋₁₄₊ t ₆₋₁₄₋ | 14 14 | 1.0 1.0 | 4.7 4.7 | 1.0 1.0 | | 4.3 4.3 | 1.0 1.0 | 4.4 4.4 | |
| Reset Input | t ₁₁₊₄ | 4 | 1.0 | 4.0 | 1.0 | 0 | 3.9 | 1.0 | 4.2 | |
| · | t ₁₁₊₁₄ | 14 | 1.0 | 4.0 | 1.0 | 0, | 3.9 | 1.0 | 4.2 | |
| Setup TIme Hold Time | t _{setup} t _{hold} | 14 14 | 2.5 1.5 | | 2.5 1.5 | | | 2.5 1.5 | | |
| Rise Time (20 to 80%) | t+ | 14 | 1.0 | 3.6 | 1.1 | | 3.5 | 1.1 | 3.7 | |
| Fall Time (20 to 80%) | t– | 14 | 1.0 | 3.6 | 1.1 | | 3.5 | 1.1 | 3.7 | |
| OENICE NO | | | r test. | | | | | | | |

ELECTRICAL CHARACTERISTICS (continued)

| | | | | | TEST VOI | TAGE VALU | JES (Volts) | | |
|-------------------------|-------------|--|--------------------|---|--------------------|---------------------|---------------------|-----------------|----------------------------------|
| | | @ Test Te | mperature | V _{IHmax} | V _{ILmin} | V _{IHAmin} | V _{ILAmax} | V _{EE} | |
| | | | –30°C | -0.890 | -1.890 | -1.205 | -1.500 | -5.2 | |
| | | +25°C | -0.810 | -1.850 | -1.105 | -1.475 | -5.2 | | |
| | | | +85°C | -0.700 | -1.825 | -1.035 | -1.440 | -5.2 | |
| | | | Pin | TEST VOLTAGE APPLIED TO PINS LISTED BELOW | | | | | |
| Characteristic | | Symbol | Under Test | V _{IHmax} | V _{ILmin} | V _{IHAmin} | V _{ILAmax} | V _{EE} | (V _{CC}) Gnd |
| Power Supply Drain C | Current | ΙE | 8 | | | | | 8 | 1, 16 |
| Input Current | | l _{inH} | 6 7 10 11 | 6 7 10 11 | | | | 8 8 8 | 1, 16 1, 16 1, 16 1, 16 |
| | | I _{inL} | All | | Note 1. | | | 8 | 1, 16 |
| Output Voltage | Logic 1 | V _{OH} | 14 15 | 10 12 | 6 6 | | | 8 8 | 1, 16 1, 16 |
| Output Voltage | Logic 0 | V _{OL} | 14 15 | | 6, 10 6, 12 | | | 8 8 | 1, 16 1, 16 |
| Threshold Voltage | Logic 1 | V _{OHA} | 14 15 | | 6 | 10 12 | | 8 8 | 1, 16 1, 16 |
| Threshold Voltage | Logic 0 | V _{OLA} | 14 15 | | 6 6 | | 10 12 | 8 8 | 1, 16 1, 16 |
| Switching Times | (50Ω Load) | | | +1.11V | +0.31V | Pulse In | Pulse Out | -3.2 V | +2.0 V |
| | Data Input | t ₁₀₊₁₄₊ t _{10–14–} | 14 14 | | 6, 7 6, 7 | 10 10 | 14 14 | 8 8 | 1, 16 1, 16 |
| | Clock Input | t ₆₋₁₄₊ t ₆₋₁₄₋ | 14 14 | | 7 7 | 10, 6 10, 6 | 14 14 | 8 8 | 1, 16 1, 16 |
| | Reset Input | t ₁₁₊₄₋ t ₁₁₊₁₄₋ | 4 14 | 5 10 | 6 6 | 7, 11 7, 11 | 4 (2.) 14 (2.) | 8 8 | 1, 16 1, 16 |
| Setup TIme Hold Time | | t _{setup} t _{hold} | 14 14 | | 7 7 | 6, 10 6, 10 | 14 14 | 8 8 | 1, 16 1, 16 |
| Rise Time | (20 to 80%) | t+ | 14 | | 6, 7 | 10 | 14 | 8 | 1, 16 |
| Fall Time | (20 to 80%) | t- | 14 | | 6, 7 | 10 | 14 | 8 | 1, 16 |

^{1.} Individually test each input; apply V_{ILmin} to pin under test.

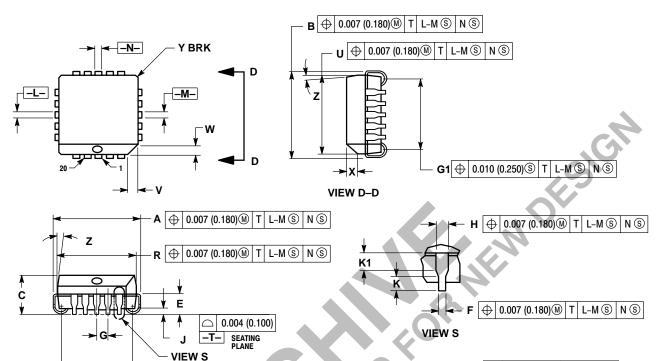
Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibitum has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

^{2.} Output latched to high logic state prior to test.

PACKAGE DIMENSIONS

PLCC-20 **FN SUFFIX**

PLASTIC PLCC PACKAGE CASE 775-02 ISSUE C



NOTES:

G1 ⊕ 0.010 (0.250)③ T L-M ⑤ N ⑤

OF MICE. NOT PERSON

- OTES:

 1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.

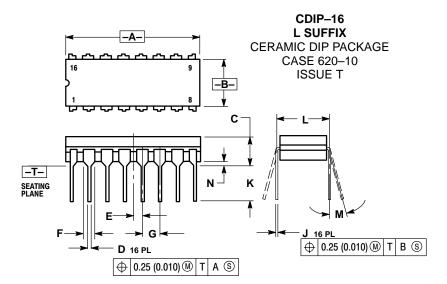
 2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.

 3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.

 4. DIMENSIONING AND TOLERANCING PER ANSI V14 5M 1982
- Y14.5M, 1982. CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

| | INC | HES | MILLIMETERS | | |
|-----|-------|-------|-------------|-------|--|
| DIM | MIN | MAX | MIN | MAX | |
| Α | 0.385 | 0.395 | 9.78 | 10.03 | |
| В | 0.385 | 0.395 | 9.78 | 10.03 | |
| С | 0.165 | 0.180 | 4.20 | 4.57 | |
| E | 0.090 | 0.110 | 2.29 | 2.79 | |
| F | 0.013 | 0.019 | 0.33 | 0.48 | |
| G | 0.050 | BSC | 1.27 | BSC | |
| Н | 0.026 | 0.032 | 0.66 | 0.81 | |
| J | 0.020 | | 0.51 | | |
| K | 0.025 | | 0.64 | | |
| R | 0.350 | 0.356 | 8.89 | 9.04 | |
| U | 0.350 | 0.356 | 8.89 | 9.04 | |
| ٧ | 0.042 | 0.048 | 1.07 | 1.21 | |
| W | 0.042 | 0.048 | 1.07 | 1.21 | |
| X | 0.042 | 0.056 | 1.07 | 1.42 | |
| Y | | 0.020 | | 0.50 | |
| Z | 2° | 10° | 2° | 10 ° | |
| G1 | 0.310 | 0.330 | 7.88 | 8.38 | |
| K1 | 0.040 | | 1.02 | | |

PACKAGE DIMENSIONS



NOTES:

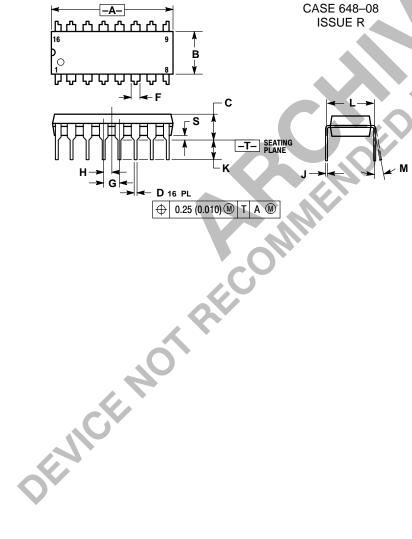
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 CONTROLLING DIMENSION: INCH.
 DIMENSION LTO CENTER OF LEAD WHEN CONTROLLING DIMENSION LTO CENTER OF LEAD WHEN

- FORMED PARALLEL

 DIMENSION F MAY NARROW TO 0.76 (0.030)
 WHERE THE LEAD ENTERS THE CERAMIC
 BODY.

| | INC | HES | MILLIMETERS | | | |
|-----|-------|-------|-------------|-------|--|--|
| DIM | MIN | MAX | MIN | MAX | | |
| Α | 0.750 | 0.785 | 19.05 | 19.93 | | |
| В | 0.240 | 0.295 | 6.10 | 7.49 | | |
| С | | 0.200 | | 5.08 | | |
| D | 0.015 | 0.020 | 0.39 | 0.50 | | |
| Е | 0.050 | BSC | 1.27 BSC | | | |
| F | 0.055 | 0.065 | 1.40 | 1.65 | | |
| G | 0.100 | BSC | 2.54 BSC | | | |
| Н | 0.008 | 0.015 | 0.21 | 0.38 | | |
| K | 0.125 | 0.170 | 3.18 | 4.31 | | |
| L | 0.300 | BSC | 7.62 BSC | | | |
| M | 0 ° | 15° | 0 ° | 15° | | |
| N | 0.020 | 0.040 | 0.51 | 1.01 | | |





- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
 5. ROUNDED CORNERS OPTIONAL

| | INC | HES | MILLIN | IETERS | |
|-----|-------|-------|----------|--------|--|
| DIM | MIN | MAX | MIN | MAX | |
| Α | 0.740 | 0.770 | 18.80 | 19.55 | |
| В | 0.250 | 0.270 | 6.35 | 6.85 | |
| C | 0.145 | 0.175 | 3.69 | 4.44 | |
| D | 0.015 | 0.021 | 0.39 | 0.53 | |
| F | 0.040 | 0.70 | 1.02 | 1.77 | |
| G | 0.100 | BSC | 2.54 BSC | | |
| Н | 0.050 | BSC | 1.27 | BSC | |
| J | 0.008 | 0.015 | 0.21 | 0.38 | |
| K | 0.110 | 0.130 | 2.80 | 3.30 | |
| L | 0.295 | 0.305 | 7.50 | 7.74 | |
| M | 0° | 10° | 0° | 10 ° | |
| S | 0.020 | 0.040 | 0.51 | 1.01 | |

Notes



Notes





ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

PUBLICATION ORDERING INFORMATION

Literature Fulfillment:

Literature Distribution Center for ON Semiconductor P.O. Box 5163, Denver, Colorado 80217 USA

Phone: 303–675–2175 or 800–344–3860 Toll Free USA/Canada **Fax**: 303–675–2176 or 800–344–3867 Toll Free USA/Canada

Email: ONlit@hibbertco.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

JAPAN: ON Semiconductor, Japan Customer Focus Center 4–32–1 Nishi–Gotanda, Shinagawa–ku, Tokyo, Japan 141–0031

Phone: 81–3–5740–2700 **Email**: r14525@onsemi.com

ON Semiconductor Website: http://onsemi.com

For additional information, please contact your local

Sales Representative.