

NCP4413, NCP4414

3 A High-Speed MOSFET Drivers

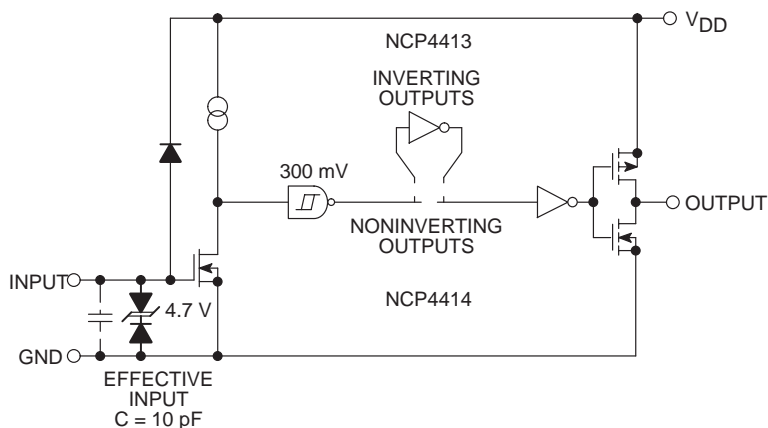
The NCP4413/4414 are 3 A CMOS buffer/drivers. They will not latch up under any conditions within their power and voltage ratings. They are not subject to damage when up to 5 V of noise spiking of either polarity that occurs on the ground pin. They can accept, without damage or logic upset, up to 500 mA of current of either polarity being forced back into their output. All terminals are fully protected against up to 4 kV of electrostatic discharge.

As MOSFET drivers, the NCP4413/4414 can easily switch 1800 pF gate capacitance in 20 nsec with matched rise and fall times, and provide low enough impedance in both the ON and the OFF states to ensure the MOSFET's intended state will not be affected, even by large transients. The rise and fall time edges are matched to allow driving short-duration inputs with greater output accuracy.

Features

- Latch-up Protected: Will Withstand 500 mA Reverse Current
- Input Will Withstand Negative Inputs Up to 5 V
- ESD Protected (4 kV)
- High Peak Output Current (3 A)
- Wide Operating Range (4.5 V to 16 V)
- High Capacitive Load Drive Capability (1800 pF in 20 nsec)
- Short Delay Time (35 nsec Typ)
- Consistent Delay Times with Changes in Supply Voltage
- Matched Delay Times
- Low Supply Current
 - With Logic "1" Input (500 μ A)
 - With Logic "0" Input (100 μ A)
- Low Output Impedance (2.7 Ω)

Functional Block Diagram



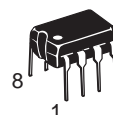
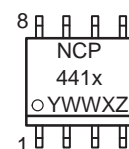
ON Semiconductor

<http://onsemi.com>

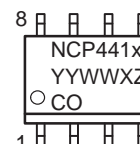
MARKING DIAGRAM



SO-8
D SUFFIX
CASE 751



PDIP-8
P SUFFIX
CASE 626



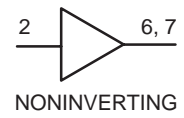
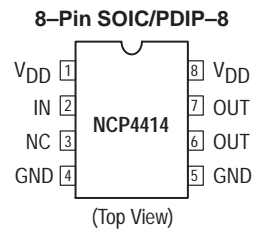
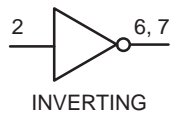
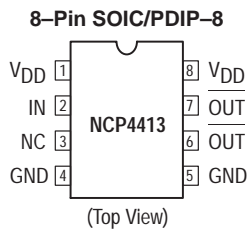
x = Device Number (3 or 4)
YY, Y = Year
WW, W = Work Week
X = Assembly ID Code
Z = Subcontractor ID Code
CO = Country of Origin

ORDERING INFORMATION

Device	Package	Shipping
NCP4413DR2 Inverting	SO-8	2500 Tape & Reel
NCP4413P Inverting	PDIP-8	50 Units/Rail
NCP4414DR2 Non-Inverting	SO-8	2500 Tape & Reel
NCP4414P Non-Inverting	PDIP-8	50 Units/Rail

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PIN CONNECTIONS



NC = NO INTERNAL CONNECTION

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ABSOLUTE MAXIMUM RATINGS*

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	+20	V
Input Voltage, IN A or IN B	V_{IN}	$V_{DD} + 0.3$ to $GND - 5.0$	V
Maximum Chip Temperature		+150	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Lead Temperature (Soldering, 10 sec)	T_{SOI}	+300	°C
Package Thermal Resistance SOIC SOIC	$R_{\theta JA}$ $R_{\theta JC}$	155 45	°C/W
Operating Temperature Range	T_A	-40 to +85	°C
Power Dissipation ($T_A \leq 70^\circ\text{C}$) SOIC	P_D	470	mW

*Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation section of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Over operating temperature range with $4.5\text{ V} \leq V_{DD} \leq 16\text{ V}$, unless otherwise specified. Typical values are measured at $T_A = 25^\circ\text{C}$; $V_{DD} = 16\text{ V}$.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Input						
Logic 1 High Input Voltage	V_{IH}	—	2.0	—	—	V
Logic 0 Low Input Voltage	V_{IL}	—	—	—	0.8	V
Input Current	I_{IN}	$0\text{V} \leq V_{IN} \leq V_{DD}$ $T_A = 25^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	-1.0 -10	— —	1.0 10	μA
Output						
High Output Voltage	V_{OH}	DC Test	$V_{DD} - 0.025$	—	—	V
Low Output Voltage	V_{OL}	DC Test	—	—	0.025	v
Output Resistance	R_O	$V_{DD} = 16\text{ V}$, $I_O = 10\text{ mA}$ $T_A = 25^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	— —	2.7 3.3	4.0 5.0	Ω
Peak Output Current	I_{PK}	$V_{DD} = 16\text{ V}$	—	3.0	—	A
Latch-Up Protection Withstand Reverse Current	I_{REV}	Duty Cycle $\leq 2\%$ $t \leq 300\text{ }\mu\text{sec}$ $V_{DD} = 16\text{ V}$	0.5	—	—	A
Switching Time (Note 1.)						
Rise Time	t_R	Figure 1 $T_A = 25^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	— —	20 24	28 33	nsec
Fall Time	t_F	Figure 1 $T_A = 25^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	— —	20 24	28 33	nsec
Delay Time	t_{D1}	Figure 1 $T_A = 25^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	— —	35 40	45 50	nsec
Delay Time	t_{D2}	Figure 1 $T_A = 25^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	— —	35 40	45 50	nsec
Power Supply						
Power Supply Current	I_S	$V_{IN} = 3\text{ V}$ $V_{IN} = 0\text{ V}$ $V_{DD} = 16\text{ V}$	— —	0.5 0.1	1.0 0.15	mA

1. Switching times are guaranteed by design.

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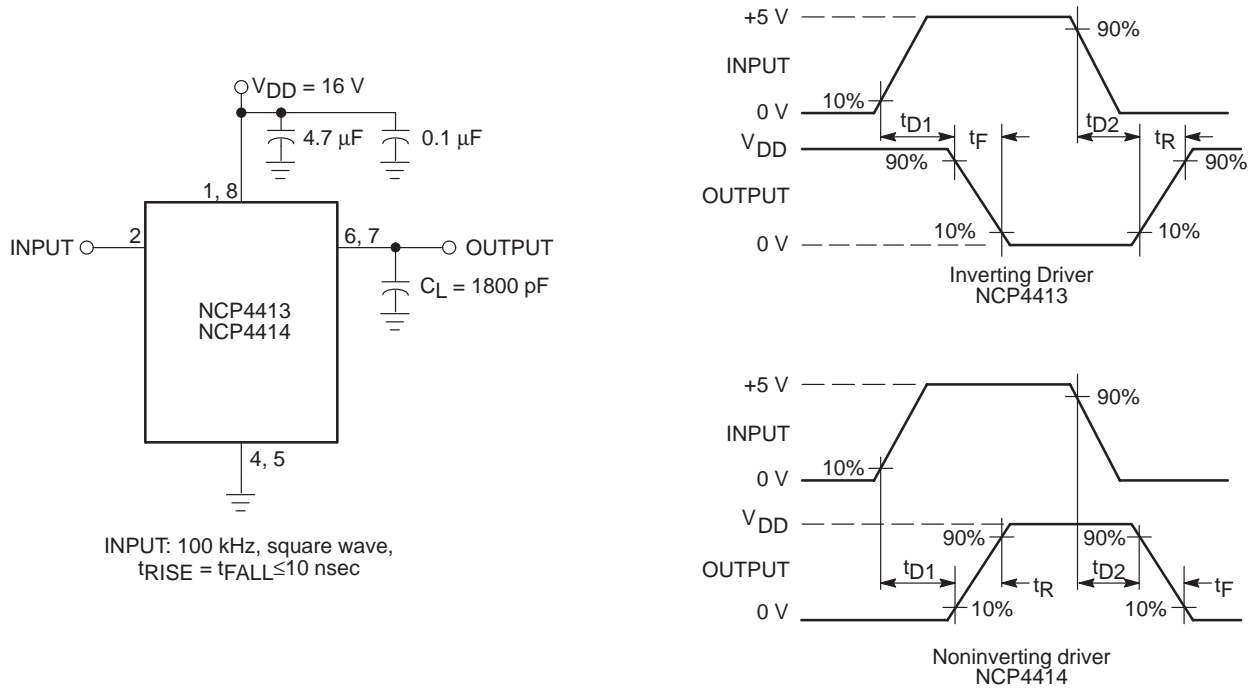


Figure 1. Switching Time Test Circuit

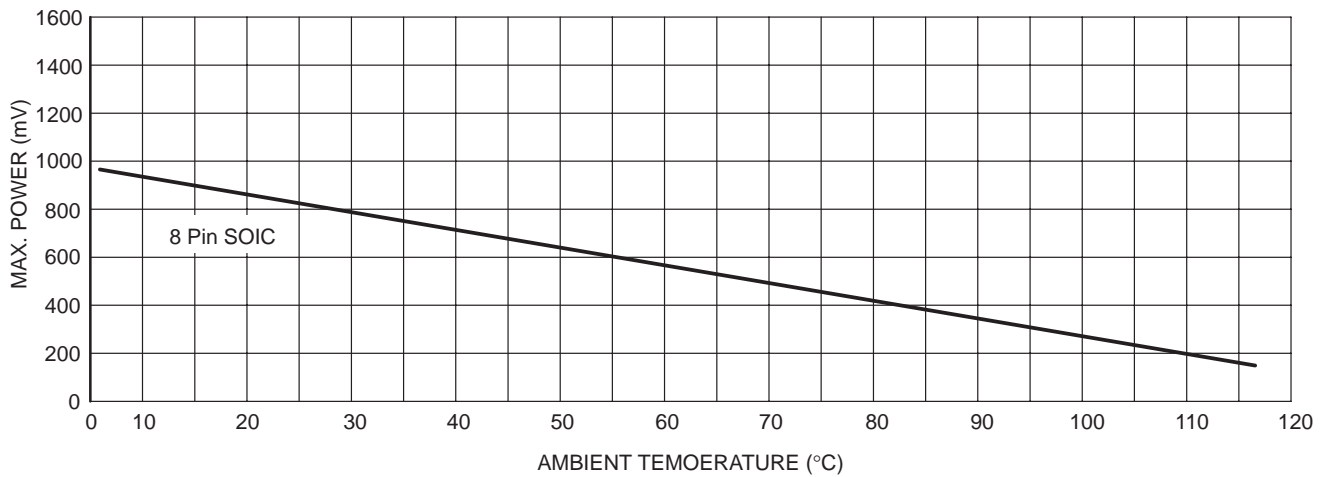


Figure 2. Thermal Derating Curves

TYPICAL CHARACTERISTICS

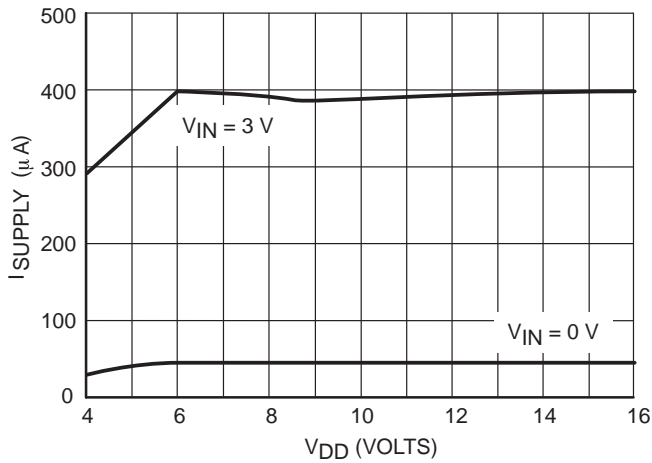


Figure 3. Quiescent Supply Current
vs. Supply Voltage
 $T_A = 25^\circ\text{C}$

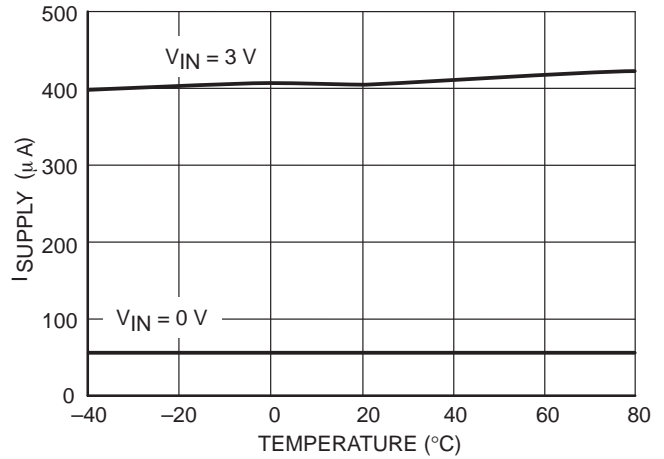


Figure 4. Quiescent Supply Current
vs. Temperature
 $V_{\text{SUPPLY}} = 16\text{ V}$

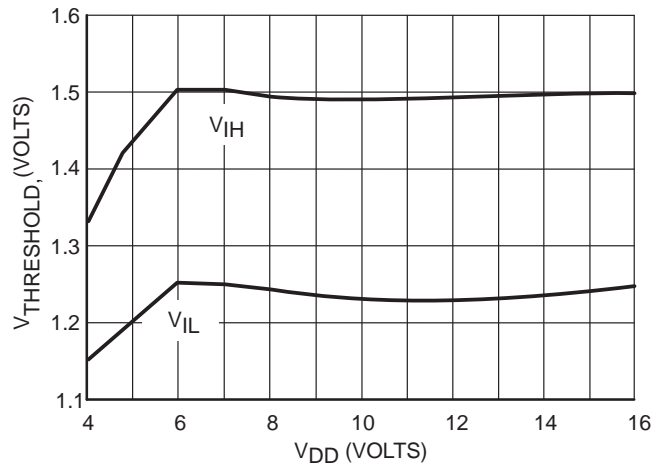


Figure 5. Input Threshold vs. Supply Voltage
 $T_A = 25^\circ\text{C}$

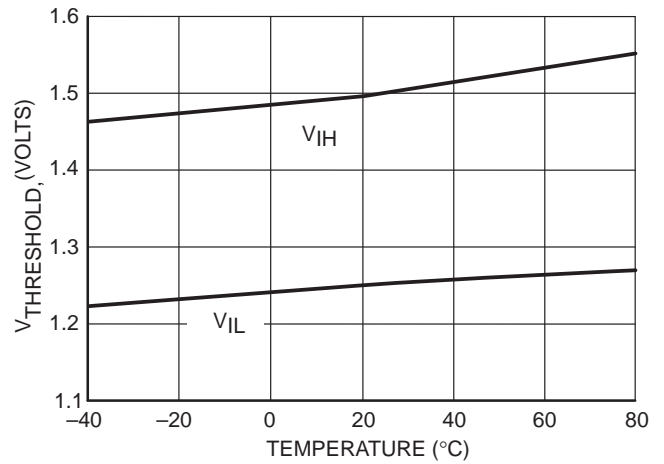


Figure 6. Input Threshold vs. Temperature
 $V_{\text{SUPPLY}} = 16\text{ V}$

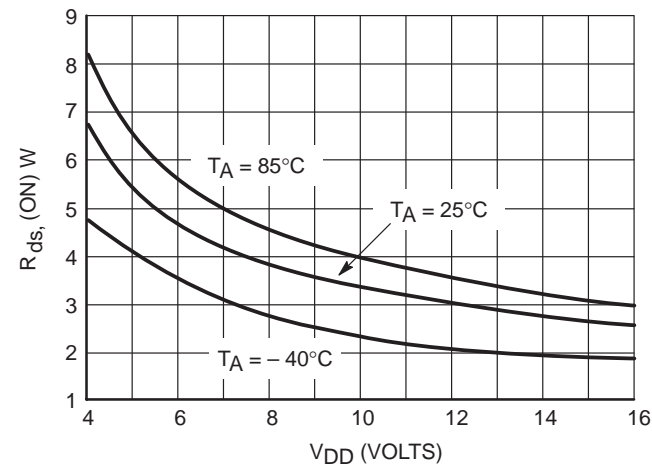


Figure 7. High-State Output Resistance

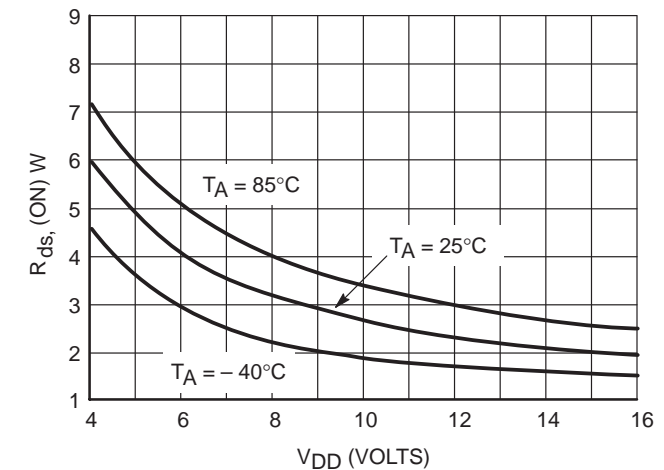


Figure 8. Low-State Output Resistance

TYPICAL CHARACTERISTICS

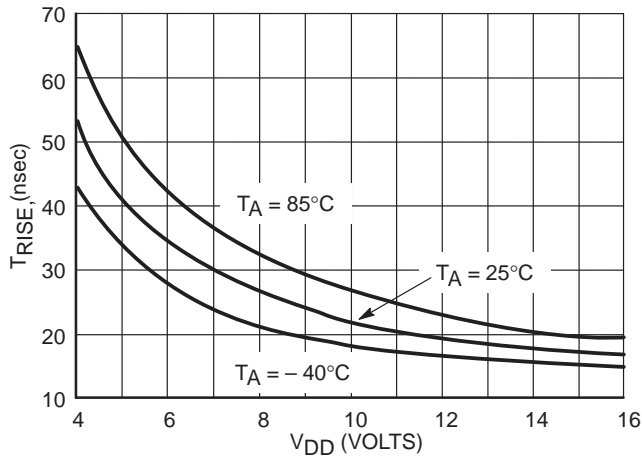


Figure 9. Rise Time vs. Supply Voltage
CLOAD = 1800 pF

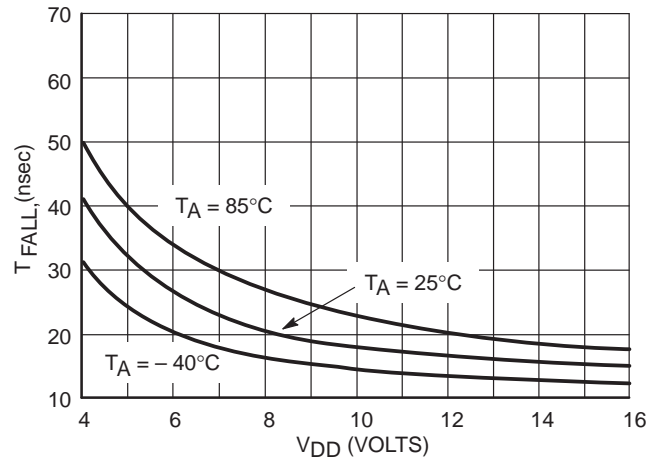


Figure 10. Fall Time vs. Supply Voltage
CLOAD = 1800 pF

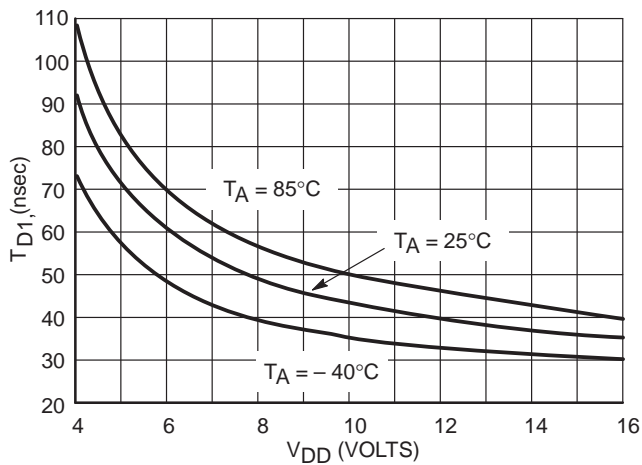


Figure 11. T_{D1} Propagation Delay
vs. Supply Voltage
CLOAD = 1800 pF

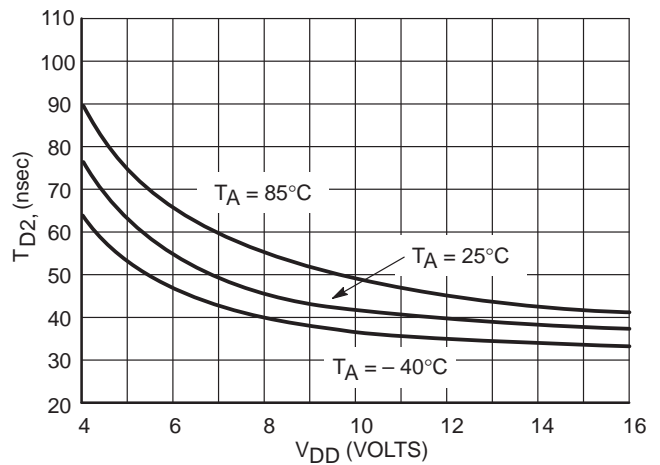


Figure 12. T_{D2} Propagation Delay
vs. Supply Voltage
CLOAD = 1800 pF

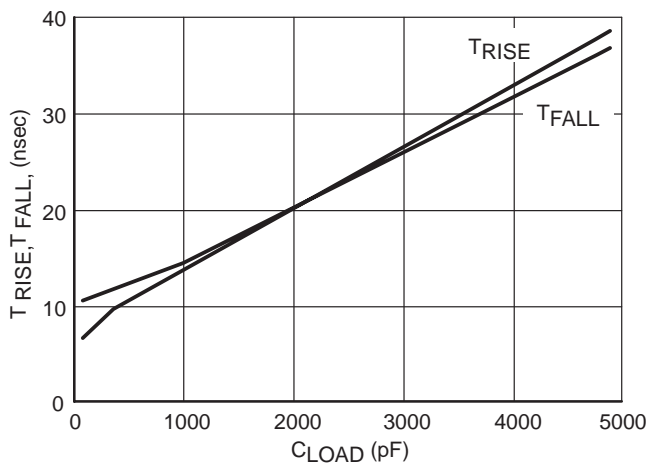


Figure 13. Rise and Fall Times
vs. Capacitive Load
 $T_A = 25^\circ\text{C}$, $V_{DD} = 16\text{ V}$

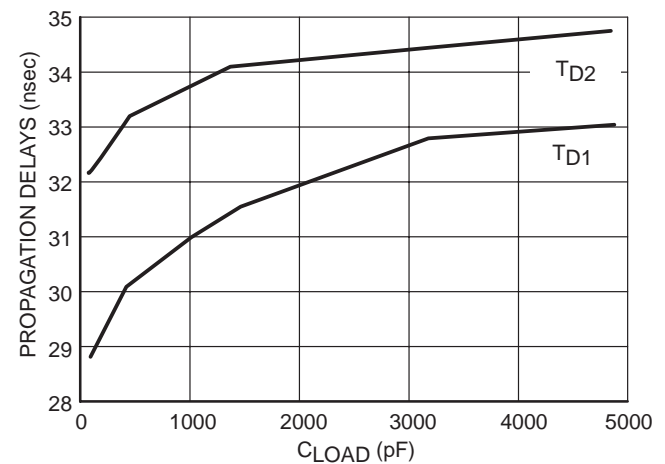
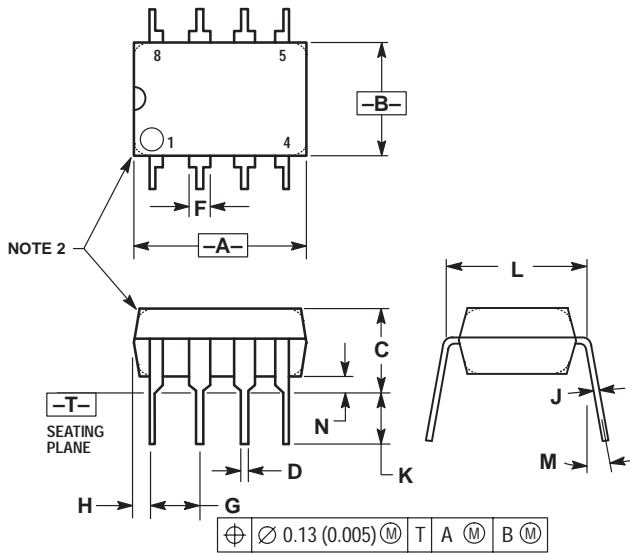


Figure 14. Propagation Delays
vs. Capacitive Load
 $T_A = 25^\circ\text{C}$, $V_{DD} = 16\text{ V}$

NCP4413, NCP4414

PACKAGE DIMENSIONS

PDIP-8
P SUFFIX
CASE 626-05
ISSUE K

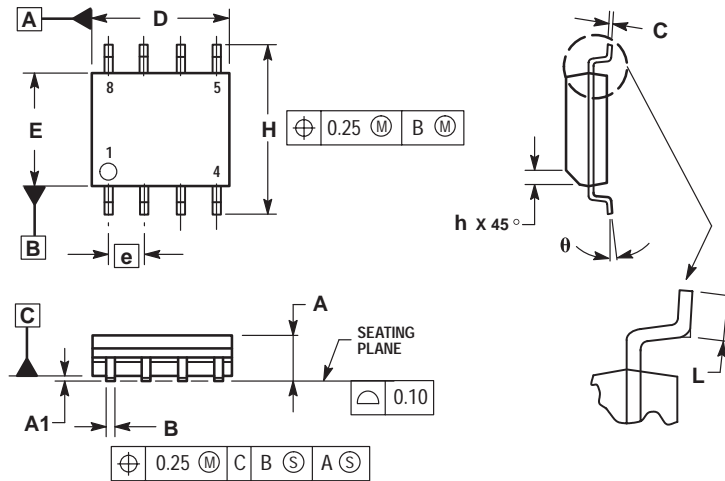


NOTES:

1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	10°		10°	
N	0.76	1.01	0.030	0.040


SO-8
D SUFFIX
CASE 751-06
ISSUE T



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETER.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

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