NCP4420, NCP4429

6 A High-Speed MOSFET Drivers

The NCP4420/NCP4429 are 6 A (peak), single output, MOSFET drivers. The NCP4429 is an inverting driver while the NCP4420 is a non–inverting driver. These drivers are fabricated in CMOS for lower power and more efficient operation versus bipolar drivers.

Both drivers have TTL–compatible inputs, which can be driven as high as V_{DD} + 0.3 V or as low as –5 V without upset or damage to the device. This eliminates the need for external level shifting circuitry and its associated cost and size. The output swing is rail–to–rail ensuring better drive voltage margin, especially during power up/power down sequencing. Propagational delay time is only 55 nsec (typ.) and the output rise and fall times are only 25 nsec (typ.) into 2500 pF across the useable power supply range.

Unlike other drivers, the NCP4420/NCP4429 are virtually latch–up proof. They can replace three or more discrete components saving PCB area, costs and improving overall system reliability.

Features

- Latch–Up Protected: Will Withstand > 1.5 A Reverse Output Current
- Logic Input Will Withstand Negative Swing Up to 5 V
- ESD Protected (4 kV)
- Matched Rise and Fall Times (25 nsec)
- High Peak Output Current (6 A Peak)
- Wide Operating Range (4.5 V to 18 V)
- High Capacitive Load Drive (10,000 pF)
- Short Delay Time (55 nsec Typ)
- Logic High Input, any Voltage (2.4 V to V_{DD})
- Low Supply Current with Logic “1’’ Input (450 μA)
- Low Output Impedance (2.5 Ω)
- Output Voltage Swing to within 25 mV of Ground or V_{DD}
- Temperature Range –40°C to +85°C

Applications

- Switch–Mode Power Supplies
- Motor Controls
- Pulse Transformer Driver
- Class D Switching Amplifiers

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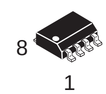
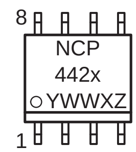
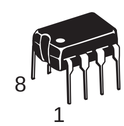
http://onsemi.com

MARKING DIAGRAM

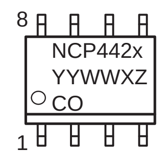


SO–8
D SUFFIX
CASE 751





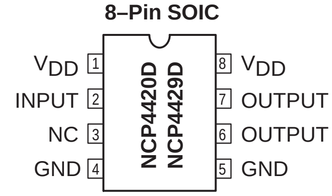
PDIP–8
P SUFFIX
CASE 626



x = Device Number (0 or 9)
YY, Y = Year
WW = Work Week
X = Assembly ID Code
Z = Subcontractor ID Code
CO = Country of Orgin

PIN CONNECTIONS

8–Pin SOIC



(Top View)

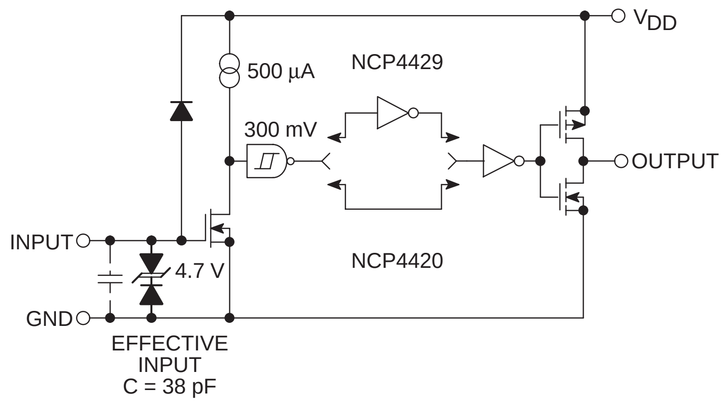
ORDERING INFORMATION

Device	Package	Shipping
NCP4420DR2 Non–Inverting	SO–8	2500 Tape & Reel
NCP4429DR2 Inverting	SO–8	2500 Tape & Reel
NCP4420P Non–Inverting	PDIP–8	50 Units/Rail
NCP4429P Inverting	PDIP–8	50 Units/Rail

June, 2000 – Rev. 0

Publication Order Number:
NCP4420/D

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Rating	Value	Unit
Supply Voltage	+20	V
Input Voltage	–5.0 to V_{DD}	V
Input Current (V_{IN} > V_{DD})	50	mA
Power Dissipation, $T_A \le 70°C$ SOIC PDIP	 470 730	mW
Derating Factors (To Ambient) SOIC PDIP	 4.0 8.0	mW/°C
Storage Temperature Range, T_{stg}	–65 to +150	°C
Operating Temperature (Chip)	+150	°C
Operating Temperature Range (Ambient), T_A	–40 to +85	°C
Lead Temperature (Soldering, 10 sec)	+300	°C

*Static–sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under “Absolute Maximum Ratings’’ may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_A = +25°C with 4.5 V ≤ V_{DD} ≤ 18 V, unless otherwise specified.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Input						
Logic 1 High Input Voltage	V_{IH}	–	2.4	1.8	–	V
Logic 0 Low Input Voltage	V_{IL}	–	–	1.3	0.8	V
Input Voltage Range	V_{IN} (Max)	–	–5.0	–	V_{DD} +0.3	V
Input Current	I_{IN}	0 V ≤ V_{IN} ≤ V_{DD}	–10	–	10	µA
Output						
High Output Voltage	V_{OH}	See Figure 1	V_{DD} –0.025	–	–	V
Low Output Voltage	V_{OL}	See Figure 1	–	–	0.025	V
Output Resistance, High	R_{OH}	I_{OUT} = 10 mA, V_{DD} = 18 V	–	2.1	2.8	Ω
Output Resistance, Low	R_{OL}	I_{OUT} = 10 mA, V_{DD} = 18 V	–	1.5	2.5	Ω

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output						
Peak Output Current	I_{PK}	V_{DD} = 18 V (See Figure 5)	–	6.0	–	A
Latch–Up Protection Withstand Reverse Current	I_{REV}	Duty Cycle ≤ 2% t ≤ 300 µs	1.5	–	–	A
Switching Time (Note 1.)						
Rise Time	t_R	Figure 1, C_L = 2500 pF	–	25	35	nsec
Fall Time	t_F	Figure 1, C_L = 2500 pF	–	25	35	nsec
Delay Time 1	t_{D1}	Figure 1	–	55	75	nsec
Delay Time 2	t_{D2}	Figure 1	–	55	75	nsec
Power Supply						
Power Supply Current	I_S	V_{IN} = 3.0 V V_{IN} = 0 V	– –	0.45 55	1.5 150	mA µA
Operating Input Voltage	V_{DD}	–	4.5	–	18	V

1. Switching times guaranteed by design.

ELECTRICAL CHARACTERISTICS (Measured over operating temperature range with 4.5 V ≤ V_{DD} ≤ 18 V, unless otherwise specified.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Input						
Logic 1 High Input Voltage	V_{IH}	–	2.4	–	–	V
Logic 0 Low Input Voltage	V_{IL}	–	–	–	0.8	V
Input Voltage Range	V_{IN} (Max)	–	–5.0	–	V_{DD} +0.3	V
Input Current	I_{IN}	0 V ≤ V_{IN} ≤ V_{DD}	–10	–	10	µA
Output						
High Output Voltage	V_{OH}	See Figure 1	V_{DD} –0.025	–	–	V
Low Output Voltage	V_{OL}	See Figure 1	–	–	0.025	V
Output Resistance, High	R_{OH}	I_{OUT} = 10 mA, V_{DD} = 18 V	–	3.0	5.0	Ω
Output Resistance, Low	R_{OL}	I_{OUT} = 10 mA, V_{DD} = 18 V	–	2.3	5.0	Ω
Switching Time (Note 1.)						
Rise Time	t_R	Figure 1, C_L = 2500 pF	–	32	60	nsec
Fall Time	t_F	Figure 1, C_L = 2500 pF	–	34	60	nsec
Delay Time 1	t_{D1}	Figure 1	–	50	100	nsec
Delay Time 2	t_{D2}	Figure 1	–	65	100	nsec
Power Supply						
Power Supply Current	I_S	V_{IN} = 3.0 V V_{IN} = 0 V	– –	0.45 60	3.0 400	mA µA
Operating Input Voltage	V_{DD}	–	4.5	–	18	V

1. Switching times guaranteed by design.

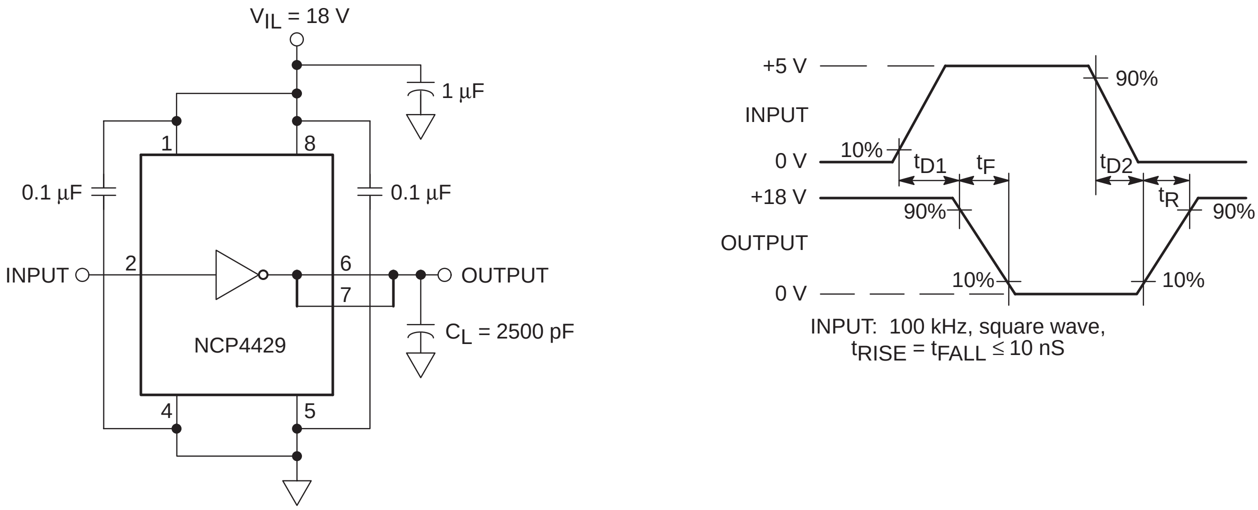


Figure 1. Switching Time Test Circuit

TYPICAL CHARACTERISTICS

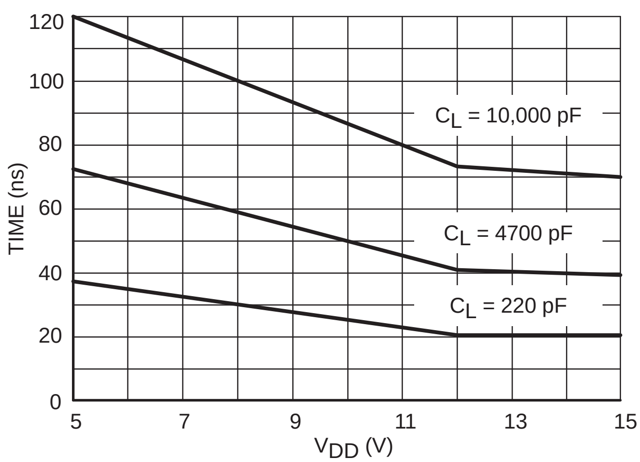


Figure 2. Rise Time vs. Supply Voltage

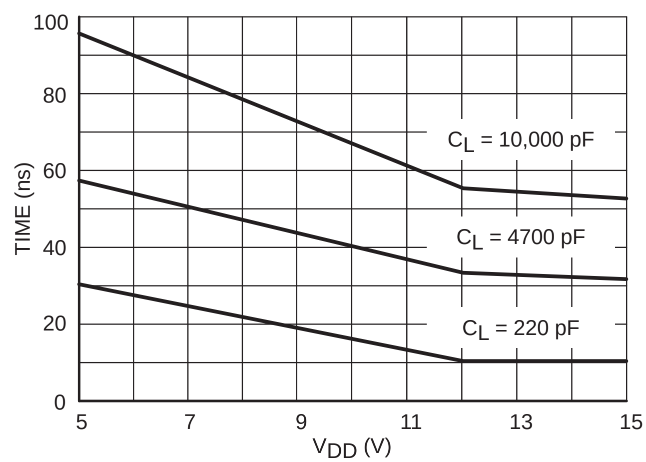


Figure 3. Fall Time vs. Supply Voltage

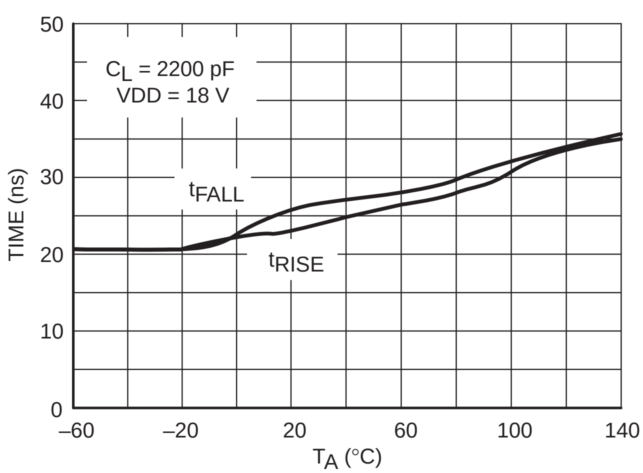


Figure 4. Rise and Fall Times vs. Temperature

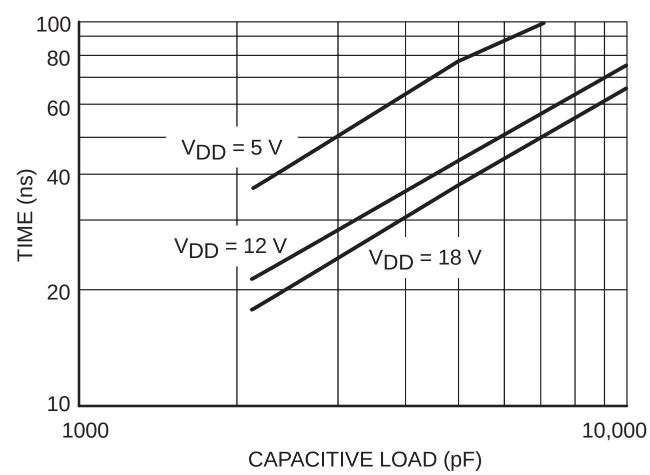


Figure 5. Rise Time vs. Capacitive Load

TYPICAL CHARACTERISTICS

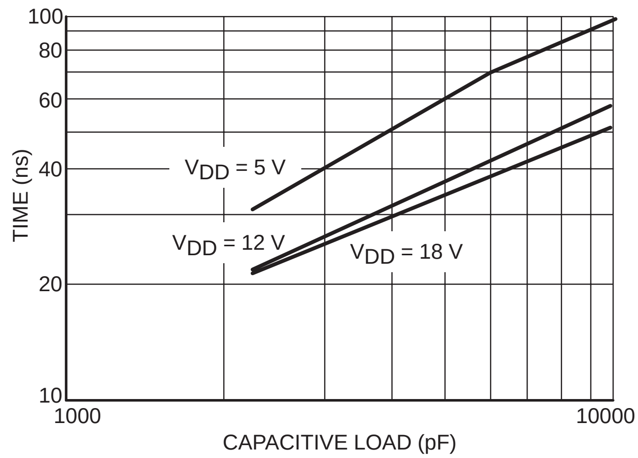


Figure 6. Fall Time vs. Capacitive Load

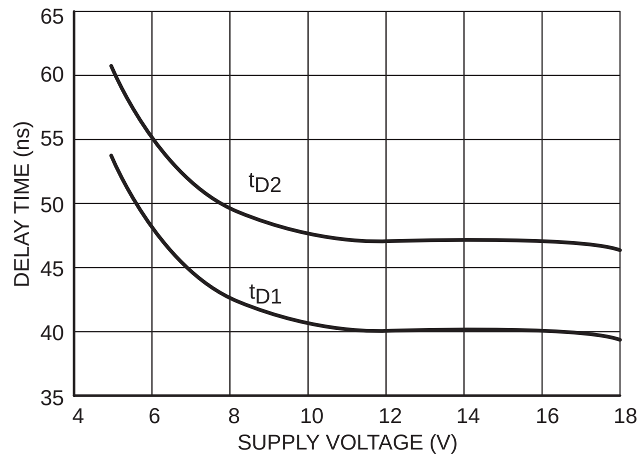


Figure 7. Propagation Delay Time vs.Supply Voltage

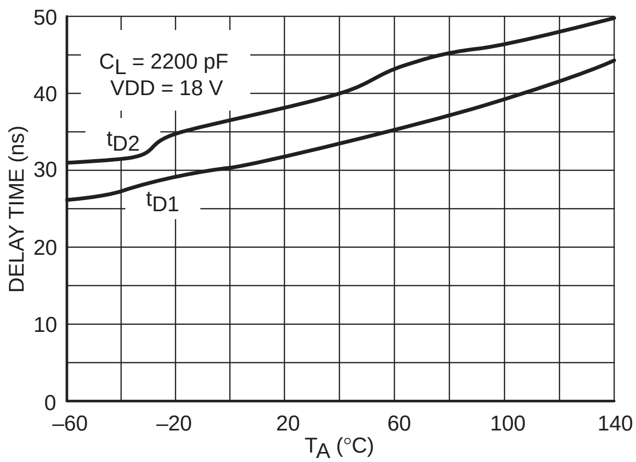


Figure 8. Propagation Delay Time vs. Temperature

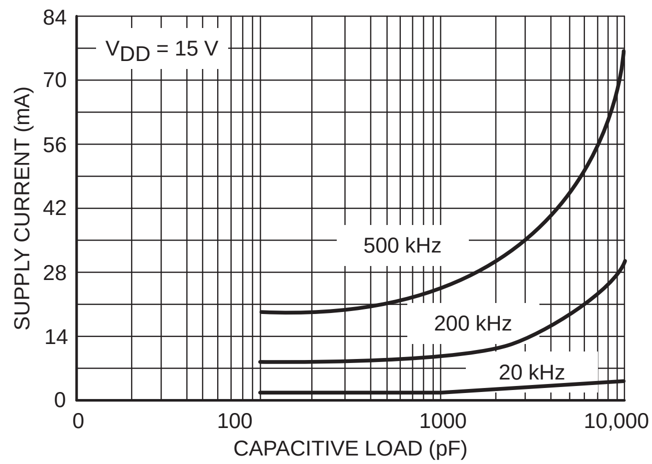


Figure 9. Supply Current vs. Capacitive Load

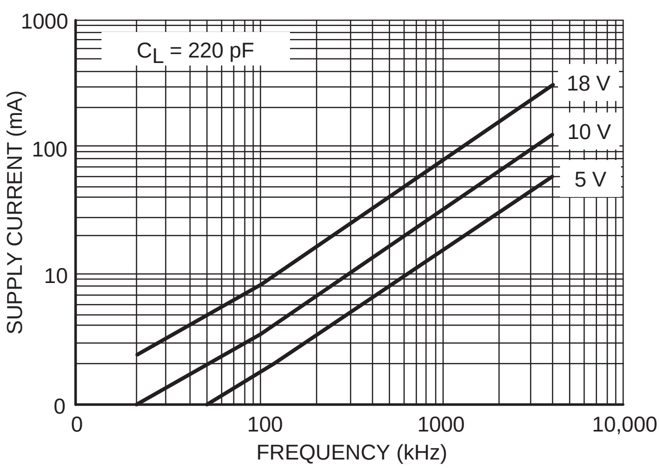


Figure 10. Supply Current vs. Frequency

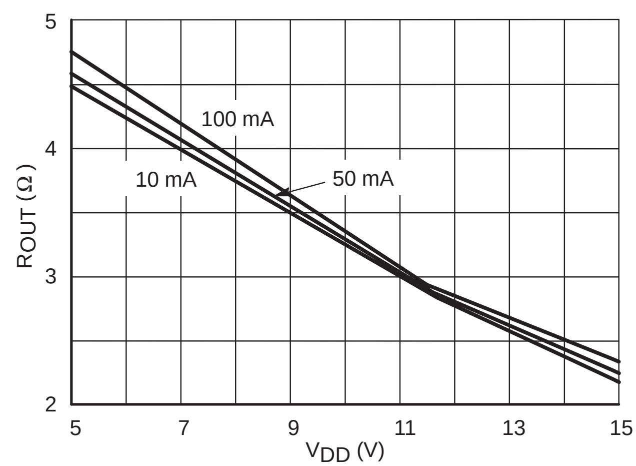


Figure 11. High–State Output Resistance

TYPICAL CHARACTERISTICS

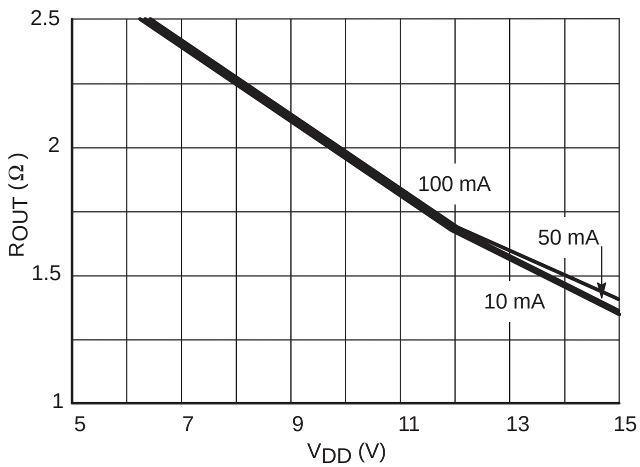


Figure 12. Low–State Output Resistance

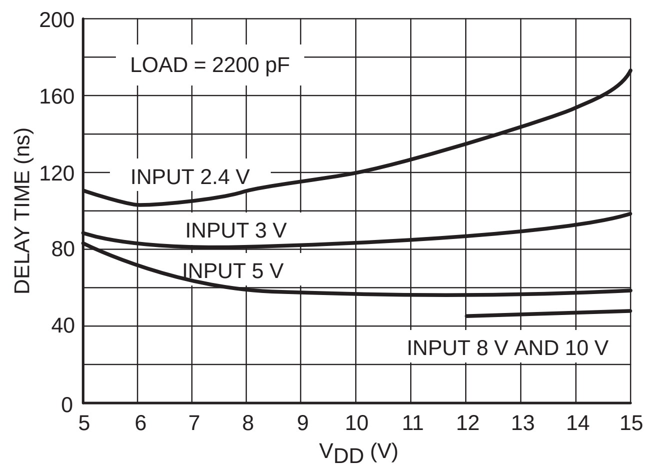


Figure 13. Effect of Input Amplitude on Propagation Delay

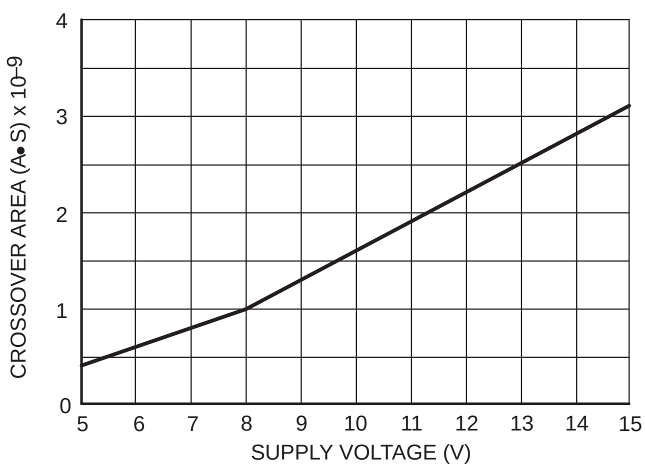
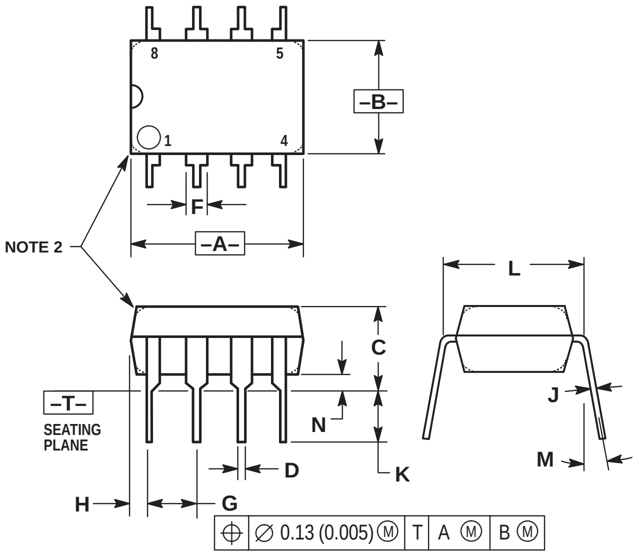


Figure 14. Total nA•S Crossover*

* The values on this graph represent the loss seen by the driver during one complete cycle. For a single transition, divide the value by 2.

PACKAGE DIMENSIONS

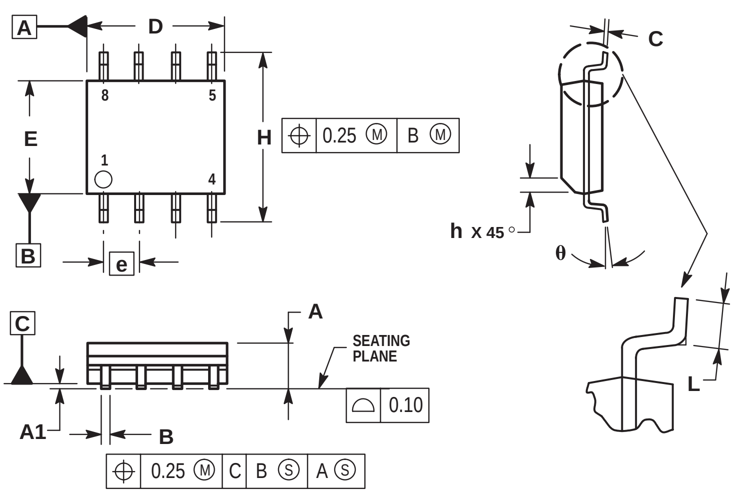
PDIP–8
P SUFFIX
CASE 626–05
ISSUE K



NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	—	10°	—	10°
N	0.76	1.01	0.030	0.040

SO–8
D SUFFIX
CASE 751–06
ISSUE T



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETER.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

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