NCP4423, NCP4424, NCP4425

3 A Dual High-Speed MOSFET Drivers

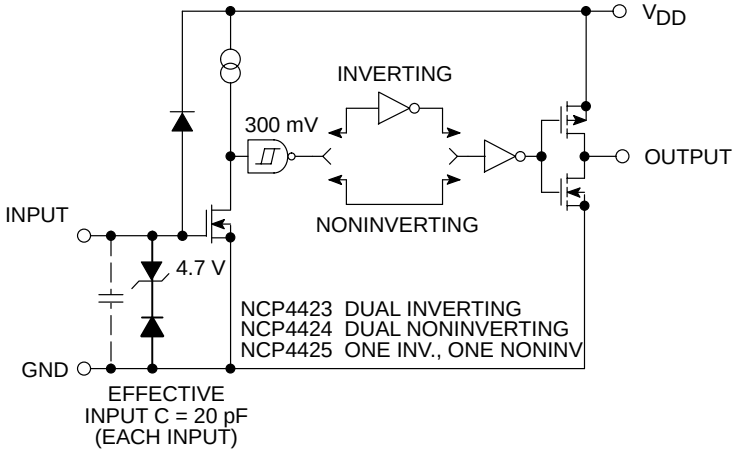
The NCP4423/4424/4425 are MOSFET drivers that are capable of giving reliable service in demanding electrical environments.

Although primarily intended for driving power MOSFETs, these drivers are well–suited for driving other loads (capacitive, resistive, or inductive) which require a low impedance driver capable of high peak currents and fast switching times. Applications such as heavily loaded clock lines, coaxial cables, or piezoelectric transducers can all be driven with the NCP4423/4424/4425. The only known limitation on loading is that the total power dissipated of the driver must be kept within the maximum power dissipation limits of the package.

Features

- High Peak Output Current (3 A)
- Wide Operating Range (4.5 V to 18 V)
- High Capacitive Load Drive Capability (1800 pF in 25 nsec)
- Short Delay Times (< 40 nsec Typ)
- Matched Rise/Fall Times
- Low Supply Current
  With Logic “1’’ Input (3.5 mA)
  With Logic “0’’ Input (350 μA)
- Low Output Impedance (3.5 Ω Typ)
- Latch–Up Protected: Will Withstand 1.5 A Reverse Current
- Logic Input Will Withstand Negative Swing Up to 5 V
- ESD Protected (4 kV)

FUNCTIONAL BLOCK DIAGRAM

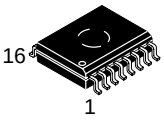


NOTES:
1. NCP4425 has one inverting and one noninverting driver.
2. Ground any unused driver input.

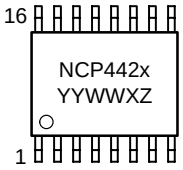
ON Semiconductor

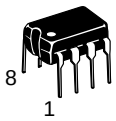
http://onsemi.com

MARKING DIAGRAM

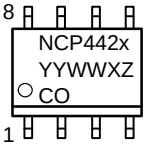


SO–16
DW SUFFIX
CASE 751G





PDIP–8
P SUFFIX
CASE 626

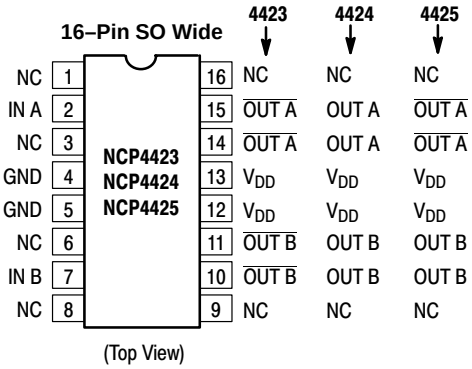


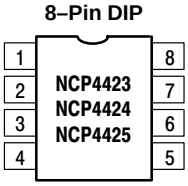
x = Device Number (3, 4, or 5)
YY = Year
WW = Work Week
X = Assembly ID Code
Z = Subcontractor ID Code
CO = Country of Origin

ORDERING INFORMATION

Device	Package	Shipping
NCP4423DWR2	SO–16	1000 Tape & Reel
NCP4424DWR2	SO–16	1000 Tape & Reel
NCP4425DWR2	SO–16	1000 Tape & Reel
NCP4423P	PDIP–8	50 Units/Rail
NCP4424P	PDIP–8	50 Units/Rail
NCP4425P	PDIP–8	50 Units/Rail

PIN CONNECTIONS





NC = NO CONNECTION

NOTE: Duplicate pins must **both** be connected for proper operation.

ABSOLUTE MAXIMUM RATINGS

Rating	Value	Unit
Supply Voltage	+22	V
Input Voltage, IN A or IN B (V_{DD} + 0.3 V to GND – 5.0 V)	–5	V
Maximum Chip Temperature	+150	°C
Storage Temperature Range, T_{stg}	–65 to +150	°C
Lead Temperature (Soldering, 10 sec)	+300	°C
Package Thermal Resistance SOIC, $R_{\theta JA}$ PDIP, $R_{\theta JA}$ PDIP, $R_{\theta JC}$	 155 –125 –45	°C/W
Operating Temperature Range	–40 to +85	°C
Package Power Dissipation ($T_A \leq 70°C$) SOIC PDIP	 470 730	 mW mc

ELECTRICAL CHARACTERISTICS (T_A = +25°C with 4.5 V ≤ V_{DD} ≤ 18 V, unless otherwise specified.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Input						
Logic 1 High Input Voltage	V_{OH}	–	2.4	–	–	V
Logic 0 Low Input Voltage	V_{IL}	–	–	–	0.8	V
Input Current	I_{IN}	0 V ≤ V_{IN} ≤ V_{DD}	–1.0	–	1.0	μA
Output						
High Output Voltage	V_{OH}	–	V_{DD} –0.025	–	–	V
Low Output Voltage	V_{OL}	–	–	–	0.025	V
Output Resistance, High	R_{OH}	I_{OUT} = 10 mA, V_{DD} = 18 V	–	2.8	5.0	Ω
Output Resistance, Low	R_{OL}	I_{OUT} = 10 mA, V_{DD} = 18 V	–	3.5	5.0	Ω
Peak Output Current	I_{PK}	–	–	3.0	–	A
Latch–Up Protection Withstand Reverse Current	I_{REV}	Duty Cycle ≤ 2% t ≤ 300 μs	1.5	–	–	A
Switching Time (Note 1.)						
Rise Time	t_R	Figure 1, C_L = 1800 pF	–	23	35	nsec
Fall Time	t_F	Figure 1, C_L = 1800 pF	–	25	35	nsec
Delay Time 1	t_{D1}	Figure 1, C_L = 1800 pF	–	33	75	nsec
Delay Time 2	t_{D2}	Figure 1, C_L = 1800 pF	–	38	75	nsec
Power Supply						
Power Supply Current	I_S	V_{IN} = 3.0 V (Both Inputs) V_{IN} = 0 V (Both Inputs)	– –	1.5 0.15	2.5 0.25	mA

1. Switching times guaranteed by design.

ELECTRICAL CHARACTERISTICS (Over operating temperature range with 4.5 V ≤ V_{DD} ≤ 18 V, unless otherwise specified.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Input						
Logic 1 High Input Voltage	V_{IH}	–	2.4	–	–	V
Logic 0 Low Input Voltage	V_{IL}	–	–	–	0.8	V
Input Current	I_{IN}	0 V ≤ V_{IN} ≤ V_{DD}	–10	–	10	μA
Output						
High Output Voltage	V_{OH}	–	V_{DD} –0.025	–	–	V
Low Output Voltage	V_{OL}	–	–	–	0.025	V
Output Resistance, High	R_O	I_{OUT} = 10 mA, V_{DD} = 18 V	–	3.7	8.0	Ω
Output Resistance, Low	R_O	I_{OUT} = 10 mA, V_{DD} = 18 V	–	4.3	8.0	Ω
Peak Output Current	I_{PK}	–	–	3.0	–	A
Latch–Up Protection Withstand Reverse Current	I_{REV}	Duty Cycle ≤ 2% t ≤ 300 μsec	1.5	–	–	A
Switching Time (Note 1.)						
Rise Time	t_R	Figure 1, C_L = 1800 pF	–	28	60	nsec
Fall Time	t_F	Figure 1, C_L = 1800 pF	–	32	60	nsec
Delay Time 1	t_{D1}	Figure 1, C_L = 1800 pF	–	32	100	nsec
Delay Time 2	t_{D2}	Figure 1, C_L = 1800 pF	–	38	100	nsec
Power Supply						
Power Supply Current	I_S	V_{IN} = 3.0 V (Both Inputs) V_{IN} = 0 V (Both Inputs)	– –	2.0 0.2	3.5 0.3	mA

1. Switching times guaranteed by design.

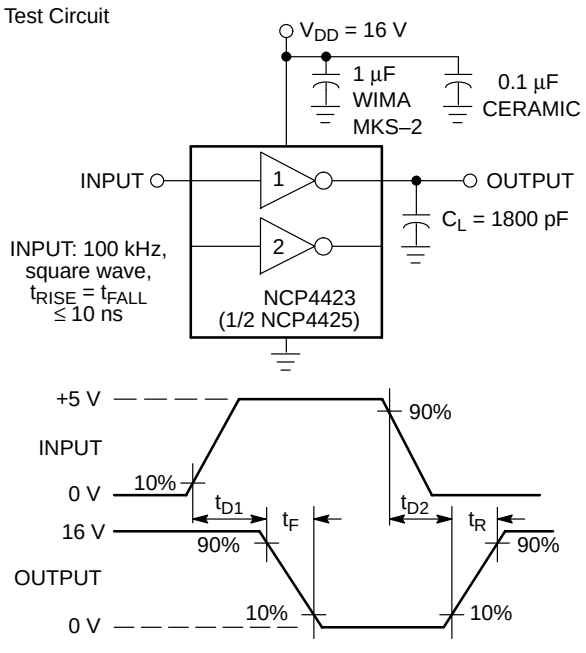


Figure 1. Inverting Driver Switching Time

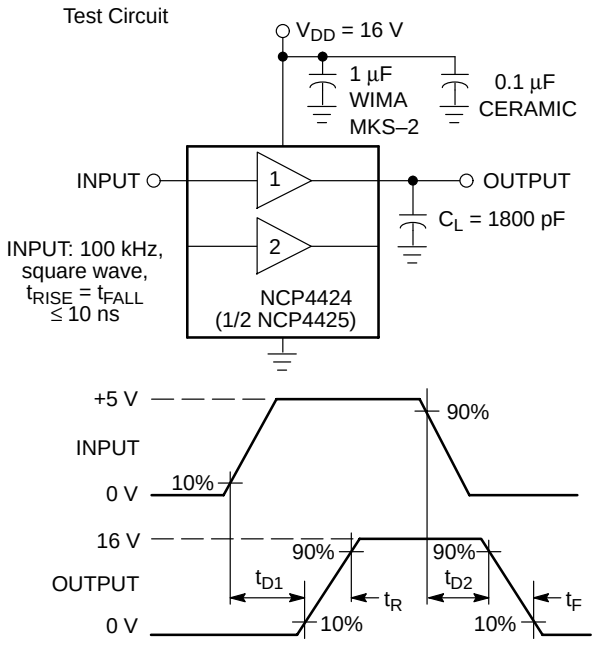


Figure 2. Noninverting Driver Switching Time

TYPICAL ELECTRICAL CHARACTERISTICS

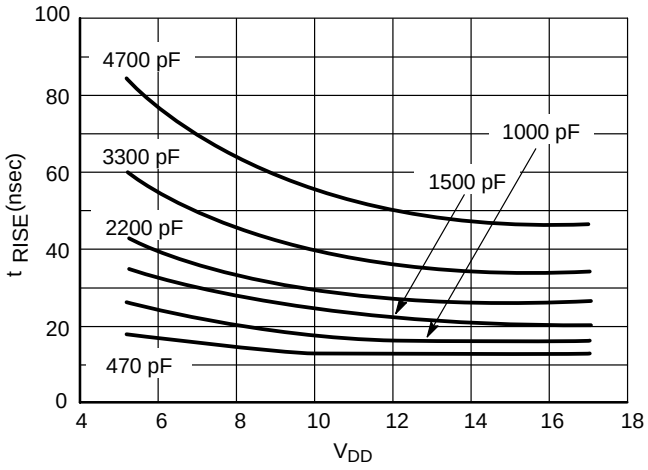


Figure 3. Rise Time vs. Supply Voltage

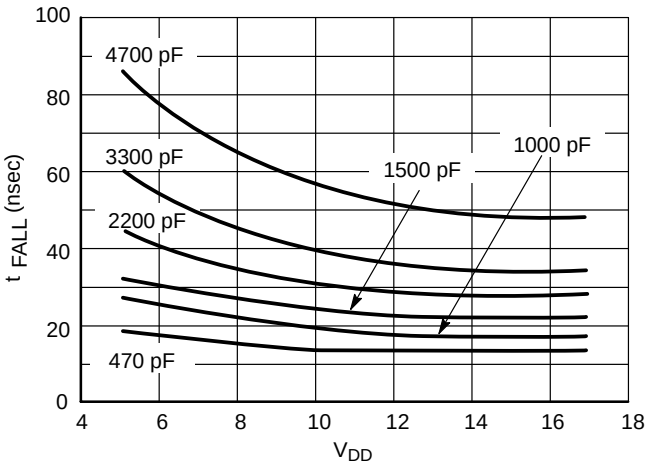


Figure 4. Fall Time vs. Supply Voltage

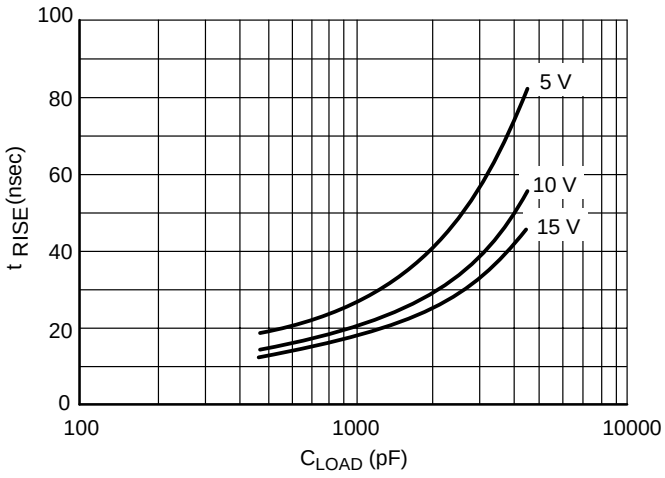


Figure 5. Rise Time vs. Capacitive Load

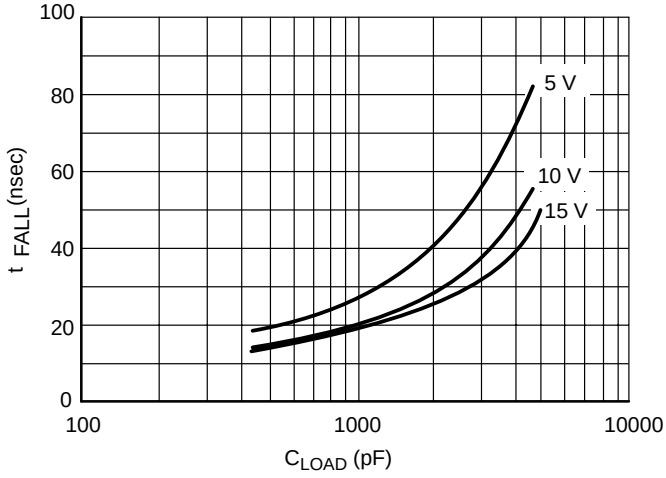


Figure 6. Fall Time vs. Capacitive Load

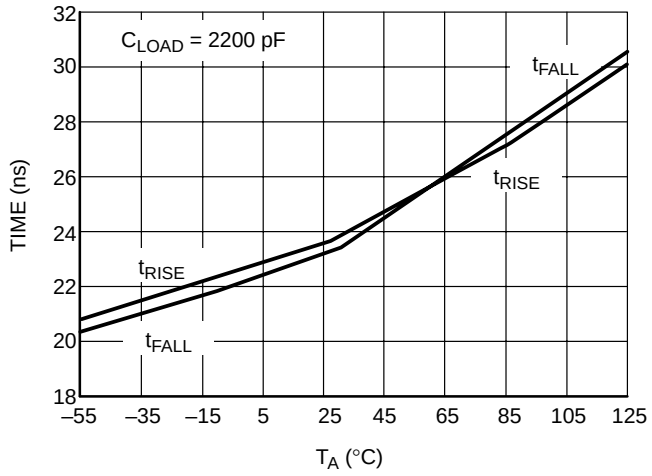


Figure 7. Rise and Fall Times vs. Temperature

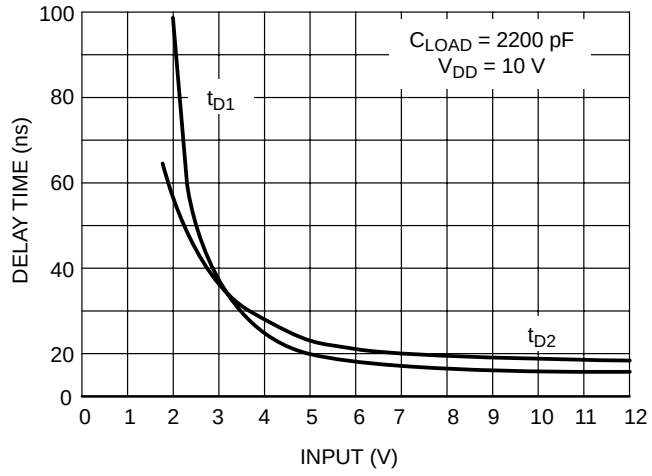


Figure 8. Propagation Delay vs. Input Amplitude

TYPICAL ELECTRICAL CHARACTERISTICS

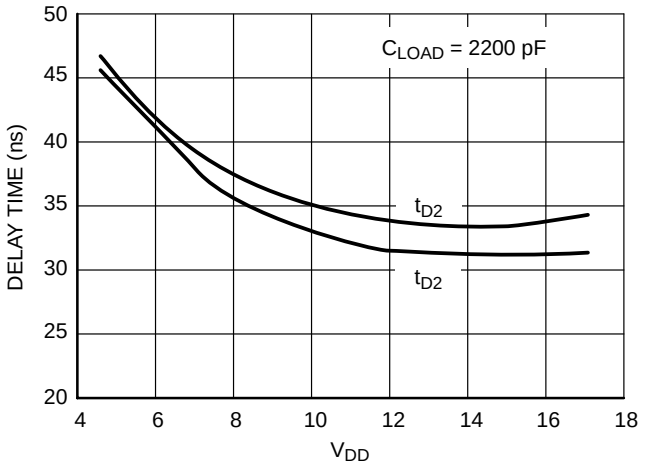


Figure 9. Propagation Delay Time vs. Supply Voltage

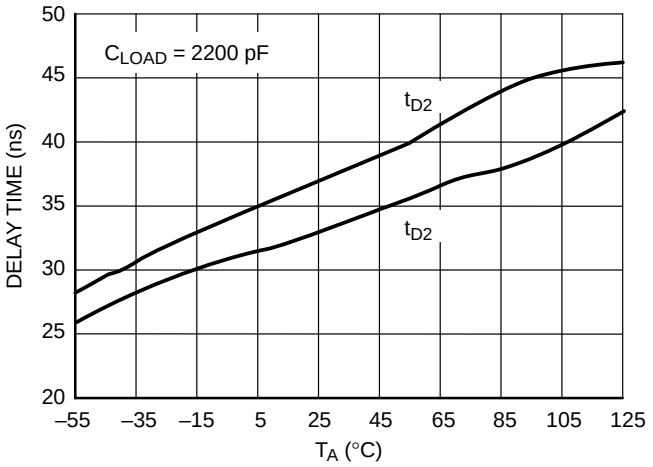


Figure 10. Delay Time vs. Temperature

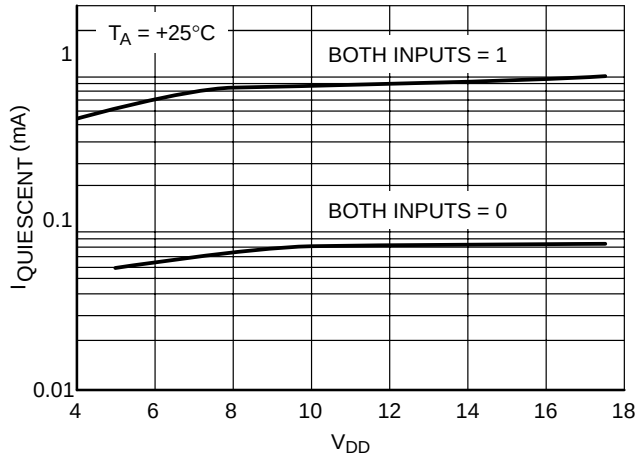


Figure 11. Quiescent Current vs. Supply Voltage

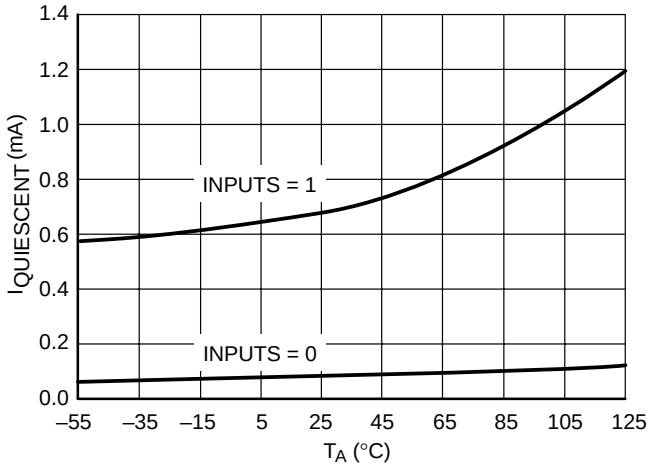


Figure 12. Quiescent Current vs. Temperature

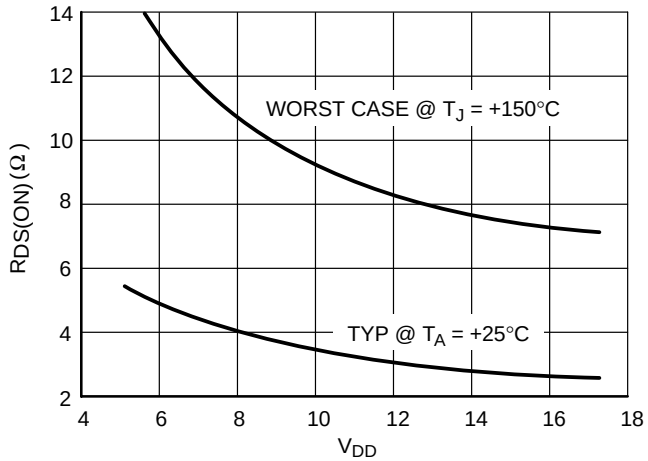


Figure 13. Output Resistance (Output High) vs. Supply Voltage

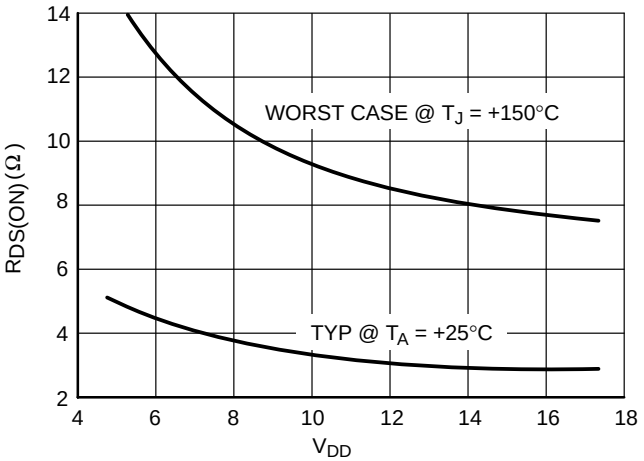


Figure 14. Output Resistance (Output Low) vs. Supply Voltage

TYPICAL ELECTRICAL CHARACTERISTICS

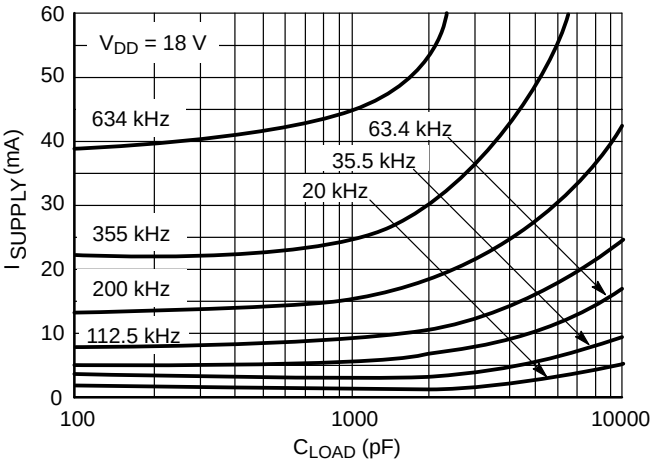


Figure 15. Supply Current vs. Capacitive Load

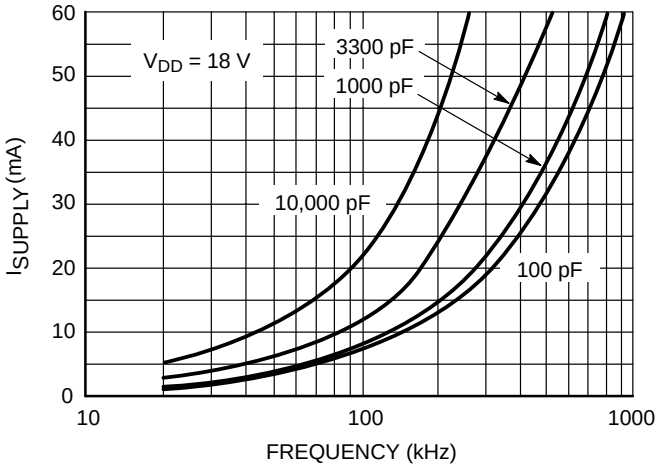


Figure 16. Supply Current vs. Frequency

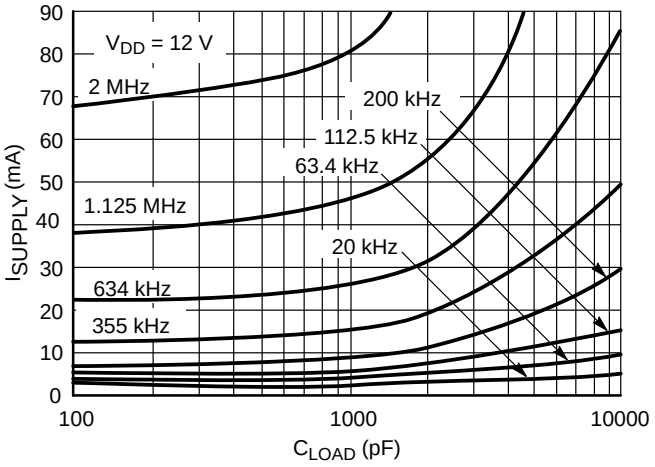


Figure 17. Supply Current vs. Capacitive Load

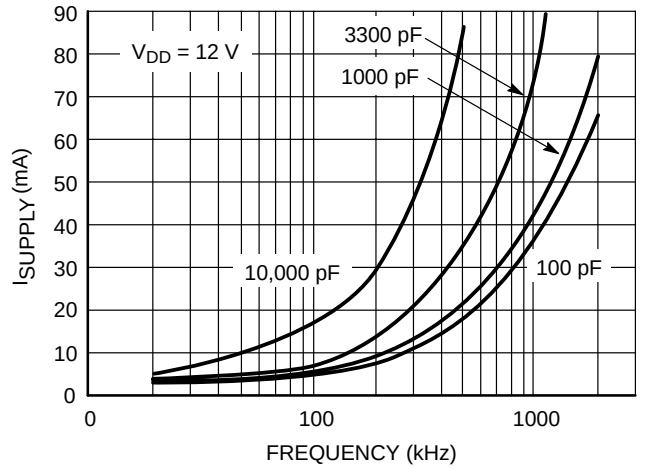


Figure 18. Supply Current vs. Frequency

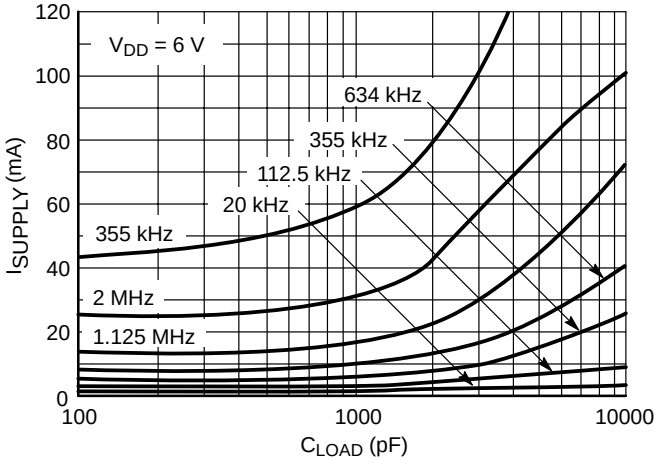


Figure 19. Supply Current vs. Capacitive Load

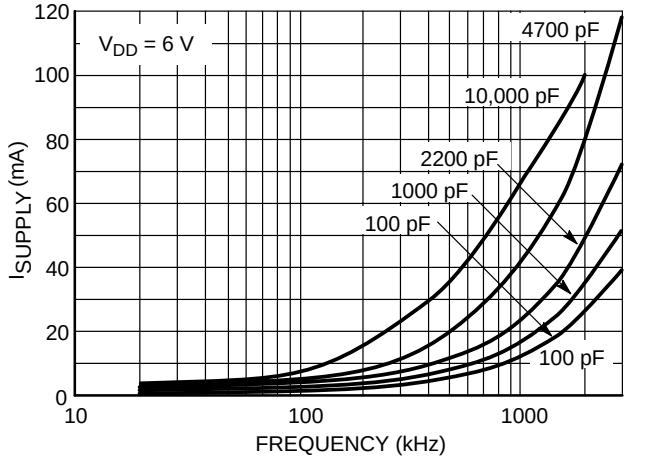


Figure 20. Supply Current vs. Frequency

TYPICAL ELECTRICAL CHARACTERISTICS

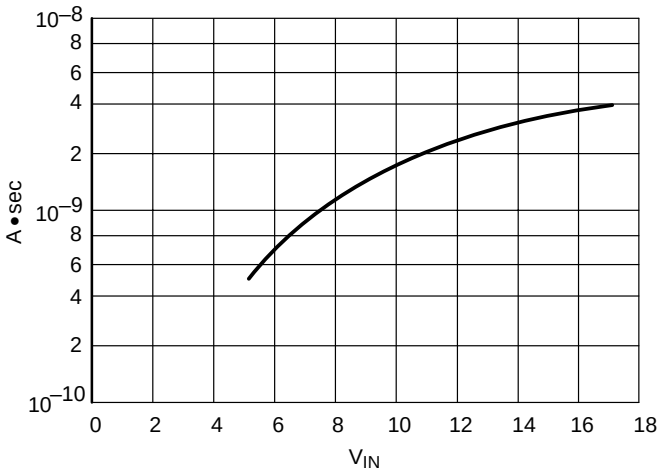


Figure 21. NCP4423 Crossover Energy

NOTE: The values on this graph represent the loss seen by both drivers in a package during one complete cycle. For a single driver, divide the stated values by 2. For a single transition of a single driver, divide the stated value by 4.

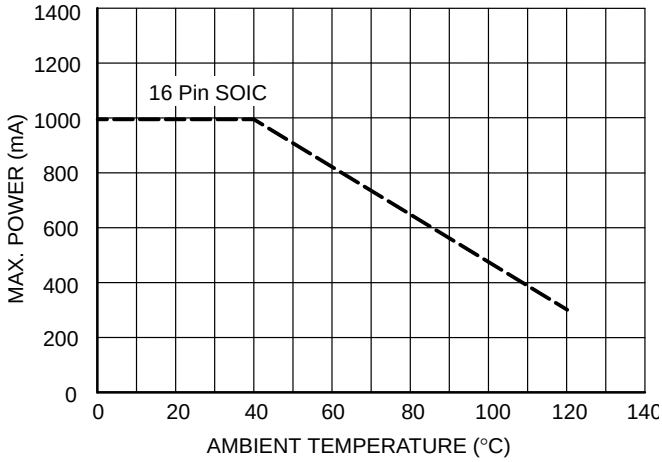
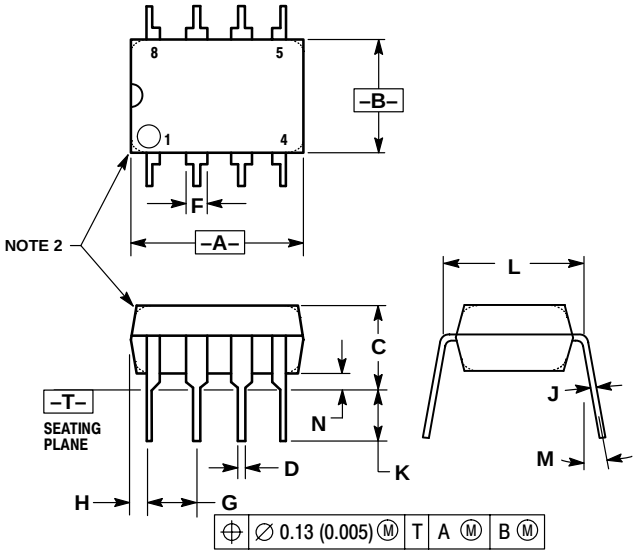


Figure 22. Thermal Derating Curves

Static–sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings (See page 2) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

PACKAGE DIMENSIONS

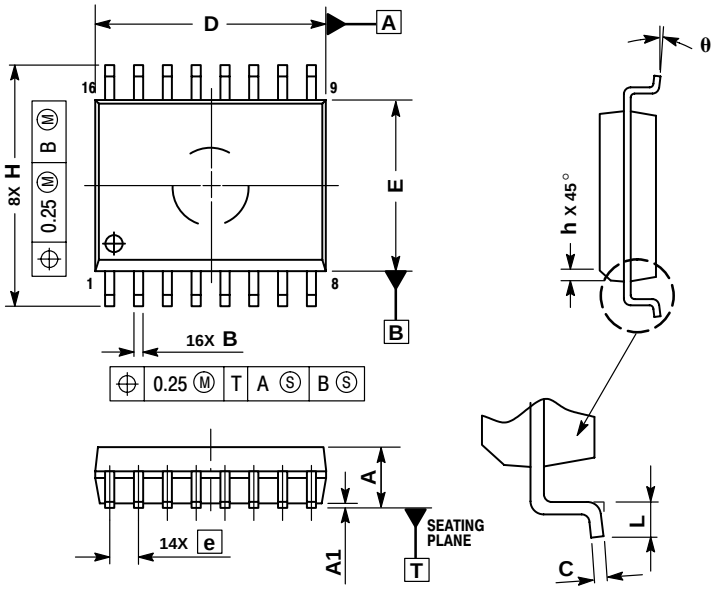
PDIP–8
P SUFFIX
CASE 626–05
ISSUE K



NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	---	10°	---	10°
N	0.76	1.01	0.030	0.040

SO–16
DW SUFFIX
CASE 751G–03
ISSUE B



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INLCUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

Notes

Notes

PUBLICATION ORDERING INFORMATION

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