NCP1509

Advance Information

PWM Buck Converter with a Very Low Iq During Low Load Conditions

The NCP1509 is a tri−mode regulator that operates either as a Synchronized PWM Buck Converter, PWM Buck Converter with internal oscillator or as a Pulsed Switching Regulator. If a synchronization signal is present, the NCP1509 operates as a current mode PWM converter with synchronous rectification. The optional external frequency input signal allows the user to control the location of the spurious frequency noise generated by a PWM converter. The Pulsed Switching Regulator mode is active when the Sync Pin is Low. The Pulsed Mode is an extremely low quiescent current Buck Converter. NCP1509 operates in a PWM mode with an internal oscillator when the Sync Pin is held high. The NCP1509 configuration allows the flexibility of efficient high power operation and low input current during system sleep modes.

Features

- Synchronous Rectification for Higher Efficiency in PWM Mode
- Pulsed Switching Mode Operation for Low Current Consumption at Low Loads
- Output Current of 300 mA in PWM and 30 mA in Pulse Mode
- Integrated MOSFETs and Feedback Circuits
- Cycle−by−Cycle Current Limit
- Switching Between PWM, with External or Internal Oscillator, and Pulsed Mode
- Operating Frequency Range of 450 to 1000 kHz
- Internal 1.0 MHz Oscillator
- Thermal Limit Protection
- Built−in Slope Compensation for Current Mode PWM Converter
- 1.05, 1.35, 1.57, 1.8 Fixed Output Voltages
- Shutdown Current Consumption of 0.2 μA
- Pb−Free Package is Available

Applications

- Cellular Phones and Pagers
- PDA
- Digital Cameras
- Supplies for DSP Cores
- Portable Applications

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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MARKING DIAGRAM

10 PIN DFN
MN SUFFIX
CASE 485C

1509 = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
NCP1509MNR2	10 Pin DFN	3000 Tape & Reel
NCP1509MNR2G	10 Pin DFN (Pb−Free)	3000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

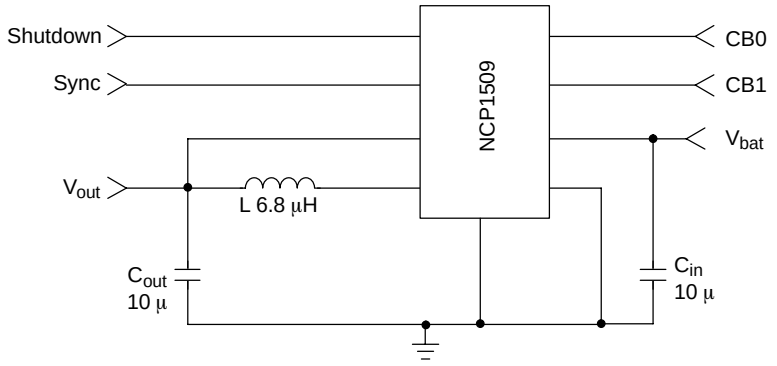


Figure 1. Applications Circuit

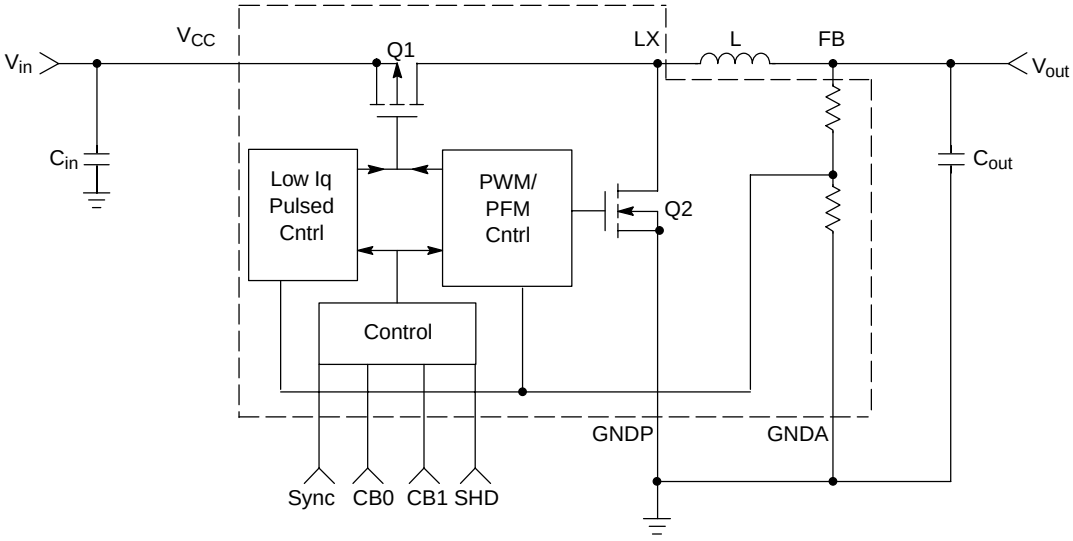


Figure 2. Block Diagram

Bill of Materials

Component	Value	Manufacturer	Part Number	Size (mm)	I_{out} (mA)	ESL (mΩ)
C	10 μF, X5R, 6.3 V	TDK muRata	C2012X5R0J106 GRM21BR60J106	2.0x1.25x1.25	−	−
L	6.8 μH	TDK Coilcraft Coilcraft Sumida	LLF4017−6R8 0805PS−682 LPO4812 CLS4D11	4.1x4.0x1.7 3.4x3.0x1.8 4.8x4.8x1.2 4.9x4.9x1.2	700 200 350 600	146 970 230 220

*Output current calculated from V_{CC} = 4.2 V_{max}, 1.5 V_{out} and Freq = 800 kHz (1.0 MHz − 20 %).

PIN FUNCTION DESCRIPTION

Pin Number	Name	Type	Description
1	GNDA	Analog GND	Ground connection for the Analog Section of the IC. This is the GND for the FB, Sync, CB0, CB1, PG and ENABLE pins.
2	GNDP	Power GND	Ground connection for the NFET Power Stage.
3	LX	Power Output	Connection from Power MOSFETs to the Inductor.
4	VCCP	Power Input	Power Supply Input for the Switching PFET.
5	VCCA	Power Input	Power Supply Input for the Analog Section of the IC.
6	FB	Analog Input	Feedback voltage from the output of the power supply.
7	CB0	Analog Input	V_{out} Selection Pin. This pin contains a pull up resistor.
8	CB1	Analog Input	V_{out} Selection Pin. This pin contains a pull up resistor.
9	SHD	Analog Input	Enable for Switching Regulator. This pin is active high to turn on the NCP1509. This pin contains an internal pull down resistor.
10	SYNC	Analog Input	Synchronization input for the PWM converter. If a clock signal is present, the converter uses the rising edge for the turn on of the PFET. If this pin is low, the converter is in Low Iq Pulse mode. If this pin is high, the converter uses the internal oscillator for the PWM mode. This pin has an internal pull down resistor to force the operation into the Pulse Mode.

MAXIMUM RATINGS (Note 1)

Rating		Symbol	Value	Unit
Maximum Voltage All Pins		V_{max}	5.5	V
Maximum Operating Voltage All Pins		V_{max}	5.2	V
Thermal Resistance, Junction−to−Air		$R_{\theta JA}$	68.5	°C/W
Operating Ambient Temperature Range		T_A	−30 to 85	°C
ESD Withstand Voltage	Human Body Model (Note 1) Machine Model (Note 1)	V_{ESD}	> 2500 > 150	V
Moisture Sensitivity		MSL	Level 1	
Storage Temperature Range		T_{stg}	−55 to 150	°C
Junction Operating Temperature		T_J	−30 to 125	°C

1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model 2,500 V per MIL−STD−883, Method 3015.
   Machine Model Method 150 V.

ELECTRICAL CHARACTERISTICS (V_{in} = 3.6 V, Vo = 1.57 V, T_A = 25°C, Fsyn = 600 kHz 50% Duty Cycle square wave for PWM mode; T_A = –30 to 85°C for Min/Max values, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
VCC Pin					
Quiescent Current of Sync Mode, I_{out} = 0 mA	Iq PWM	−	175	−	μA
Quiescent Current of PWM Mode, I_{out} = 0 mA	Iq PWM	−	185	−	μA
Quiescent Current of Pulsed Mode, I_{out} = 0 mA	Iq Pulsed	−	14	−	μA
Quiescent Current, SHD Low	Iq Off	−	0.1	1.0	μA
Input Voltage Range	Vin	2.5	−	5.2	V
Sync Pin					
Input Voltage	Vsync	−0.3	−	Vcc + 0.3	V
Frequency Operational Range	Fsync	450	600	1000	kHz
Minimum Synchronization Pulse Width	Dcsync Min	−	5.0	−	%
Maximum Synchronization Pulse Width	Dcsync Max	−	95	−	%
SYNC “H” Voltage Threshold	Vsynch	−	920	1200	mV
SYNC “L” Voltage Threshold	Vsyncl	400	830	−	mV
SYNC “H” Input Current, Vsync = 3.6 V	Isynch	−	2.2	−	μA
SYNC “L” Input Current, Vsync = 0 V	Isyncl	−0.5	−	−	μA
Output Level Selection Pins					
Input Voltage	Vcb	−0.3	−	Vcc + 0.3	V
CB0, CB1 “H” Voltage Threshold	Vcb h	−	920	1200	mV
CB0, CB1 “L” Voltage Threshold	Vcb l	400	830	−	mV
CB0 “H” Input Current, CB = 3.6 V	Icb0 h	−	2.2	−	μA
CB0 “L” Input Current, CB = 0 V	Icb0 l	−0.5	−	−	μA
CB1 “H” Input Current, CB = 3.6 V	Icb1 h	−	0.3	1.0	μA
CB1 “L” Input Current, CB = 0 V	Icb1 l	−	−2.2	−	μA
Shutdown Pin					
Input Voltage	Vshd	−0.3	−	Vcc + 0.3	V
SHD “H” Voltage Threshold	Vshd h	−	920	1200	mV
SHD “L” Voltage Threshold	Vshd l	400	830	−	mV
SHD “H” Input Current, SHD = 3.6 V	Ishd h	−	2.2	−	μA
SHD “L” Input Current, SHD = 0 V	Ishd l	−0.5	−	−	μA
Feedback Pin					
Input Voltage	Vfb	−0.3	−	Vcc + 0.3	V
Input Current, Vfb = 1.5 V	Ifb	−	5.0	7.5	μA
Sync PWM Mode Characteristics					
Switching P−FET Current Limit	I lim	−	800	−	mA
Duty Cycle	DC	−	−	100	%
Minimum On Time	Ton min	−	75	−	nsec
Rdson Switching P−FET and N_FET	Rdson	−	0.23	−	Ω
Switching P−FET and N−FET Leakage Current	Ileak	−	0	10	μA
Output Overvoltage Threshold	Vo	−	3.0	−	%
Feedback Voltage Accuracy, V_{out} Set = 1.05 V C_{B0} = L, C_{B1} = L, I_{out} = 300 mA	V_{out}	1.018	1.050	1.082	V

ELECTRICAL CHARACTERISTICS (V_{in} = 3.6 V, Vo = 1.57 V, T_A = 25°C, Fsyn = 600 kHz 50% Duty Cycle square wave for PWM mode; T_A = –30 to 85°C for Min/Max values, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Sync PWM Mode Characteristics (continued)					
Feedback Voltage Accuracy, V_{out} Set = 1.35 V, C_{B0} = L, C_{B1} = H, I_{out} = 300 mA	V_{out}	1.309	1.350	1.391	V
Feedback Voltage Accuracy, V_{out} Set = 1.57 V, C_{B0} = H, C_{B1} = H, I_{out} = 300 mA	V_{out}	1.523	1.570	1.617	V
Feedback Voltage Accuracy, V_{out} Set = 1.8 V, C_{B0} = H, C_{B1} = L, I_{out} = 300 mA	V_{out}	1.746	1.800	1.854	V
Line Regulation, V_{in} = 2.7 V−3.6 V, I_{out} = 100 mA	−	−15	−	+15	mV
Line Regulation, V_{in} = 3.6 V−5.2 V, I_{out} = 100 mA	−	−15	−	+15	mV
Load Regulation, I_{out} = 100 mA−300 mA	−	−15	−	+15	mV
Load Transient Response 10 to 100 mA Load Step	V_{out}	−	−	50	mV
Line Transient Response, I_{out} = 100 mA 3.0 to 3.6 Vin Line Step	V_{out}	−	±5.0	−	mVpp
PWM Mode with Internal Oscillator Characteristics					
Switching P−FET Current Limit	I lim	−	800	−	mA
Duty Cycle	DC	−	−	100	%
Minimum On Time	Ton min	−	75	−	nsec
Internal Oscillator Frequency	Fosc	−	1.0	−	MHz
Rdson Switching P−FET and N_FET	Rdson	−	0.23	−	Ω
Switching P−FET and N−FET Leakage Current	Ileak	−	0	10	μA
Output Overvoltage Threshold	Vo	−	3.0	−	%
Feedback Voltage Accuracy, V_{out} Set = 1.05 V, C_{B0} = L, C_{B1} = L, I_{out} = 300 mA	V_{out}	1.018	1.050	1.082	V
Feedback Voltage Accuracy, V_{out} Set = 1.35 V, C_{B0} = L, C_{B1} = H, I_{out} = 300 mA	V_{out}	1.309	1.350	1.391	V
Feedback Voltage Accuracy, V_{out} Set = 1.57 V, C_{B0} = H, C_{B1} = H, I_{out} = 300 mA	V_{out}	1.523	1.570	1.617	V
Feedback Voltage Accuracy, V_{out} Set = 1.8 V, C_{B0} = H, C_{B1} = L, I_{out} = 300 mA	V_{out}	1.746	1.800	1.854	V
Line Regulation, V_{in} = 2.7 V−3.6 V, I_{out} = 100 mA	−	−15	−	+15	mV
Line Regulation, V_{in} = 3.6 V−5.2 V, I_{out} = 100 mA	−	−15	−	+15	mV
Load Regulation, I_{out} = 100 mA−300 mA	−	−15	−	+15	mV
Load Transient Response 10 to 100 mA Load Step	V_{out}	−	−	50	mV
Line Transient Response, I_{out} = 100 mA 3.0 to 3.6 Vin Line Step	V_{out}	−	±5.0	−	mVpp
Pulsed Mode Characteristics					
On Time	Ton	−	660	−	nsec
Output Current	I_{out}	0.05	−	30	mA
Output Ripple Voltage, I_{out} = 100 μA	V_{out}	−	22	100	mV
Feedback Voltage Accuracy, V_{out} Set = 1.05 V, C_{B0} = L, C_{B1} = L	V_{out}	1.018	1.050	1.082	V
Feedback Voltage Accuracy, V_{out} Set = 1.35 V, C_{B0} = L, C_{B1} = H	V_{out}	1.309	1.350	1.391	V
Feedback Voltage Accuracy, V_{out} Set = 1.57 V, C_{B0} = H, C_{B1} = H	V_{out}	1.523	1.570	1.617	V
Feedback Voltage Accuracy, V_{out} Set = 1.8 V, C_{B0} = H, C_{B1} = L	V_{out}	1.746	1.800	1.854	V

INTRODUCTION

The NCP1509 is a tri−mode regulator intended for use in baseband supplies for portable equipment. Its unique features provide an efficient power supply for a portable device at full operating current, while also providing extremely low standby current for idle mode operation. When the system is idle, the user can activate the pulsed mode function. In this mode, the regulator provides a regulated low current output voltage keeping the system biased. When the device is in its normal operating mode, the regulator synchronizes to the system clock or uses an internal 1.0 MHz clock and turns into a switching regulator. This allows the regulator to provide efficient power to the system. This circuit is patent pending.

Operation Description

The Buck regulator is a synchronous rectifier PWM regulator with integrated MOSFETs. This regulator has a Pulsed function for low power modes to conserve power. The Tri PWM with external or internal oscillator/pulsed mode is an exclusive Patent Pending circuit.

For the PWM Synchronization mode, the operating frequency range for the NCP1509 is 450 to 1000 kHz. The output current of the PWM is optimized for 100 mA with a maximum current supply of over 300 mA for the 2.5 to 5.2 input voltage range.

If the Sync Pin is held low, the NCP1509 changes into the Pulsed mode. The Pulsed function assures the user of an extremely low input current and greatly reduced quiescent current when the users system is in a sleep mode. Internally to the NCP1509, the Synchronization pin has a pull down resistor to force the part into Pulsed mode when a clock signal is not present. The Pulsed mode guarantees an output of 30 mA.

If the Sync Pin is held high, NCP1509 enters a PWM mode with an internal 1.0 MHz oscillator. The PWM mode has the same operational characteristics (current limit, maximum output current, etc.) as the synchronized PWM mode. The Sync Pin threshold is fixed as noted in the Electrical Characteristics table.

Table 1. Sync Pin Input with Corresponding Operational Mode of NCP1509

Sync Pin State	Operational Mode
Low	Low I_q Pulsed Mode Operation
High	PWM Using Internal Oscillator for the Clock
Clock	PWM Using Rising Edge of Clock Signal to Turn On PFET Pass Element

PWM Mode with External Synchronization Signal

During normal operation, a synchronization pulse acts as the clock for the DC/DC controller. The rising edge of the clock pulls the gate of Q1 low allowing the inductor to charge. When the current through Q1 reaches either the current limit or feedback voltage reaches its limit, Q1 will turn off and Q2 will turn on. Q2 replaces the free wheeling diode typically associated with Buck Converters. Q2 will turn off when either a rising edge sync pulse is present or all the stored energy is depleted from the inductor.

The output voltage accuracy in the PWM mode is well within 3% of the nominal set value. An overvoltage protection circuit is present in the PWM mode to limit the positive voltage spike due to fast load transient conditions. If the OVP comparator is activated, the duty cycle will be 0% until the output voltage falls to the nominal level. The PWM also has the ability to go to 100% duty cycle for transient conditions and low input to output voltage differentials.

In PWM mode operates as a forced−PWM converter. Each switching cycle has a typical on−time of 75 nsec. NCP1509 has two protection circuits that can eliminate the minimum on time for the cycle. When tripped, the overvoltage protection or the thermal shutdown overrides the gate drive of the high side MOSFET.

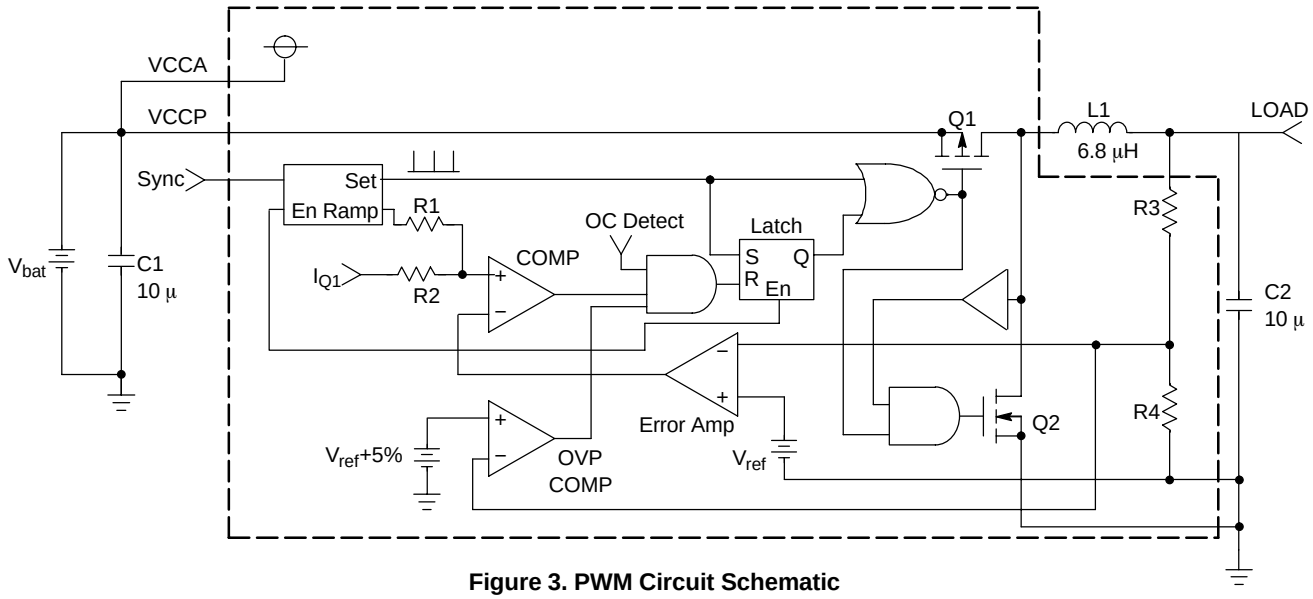


Figure 3. PWM Circuit Schematic

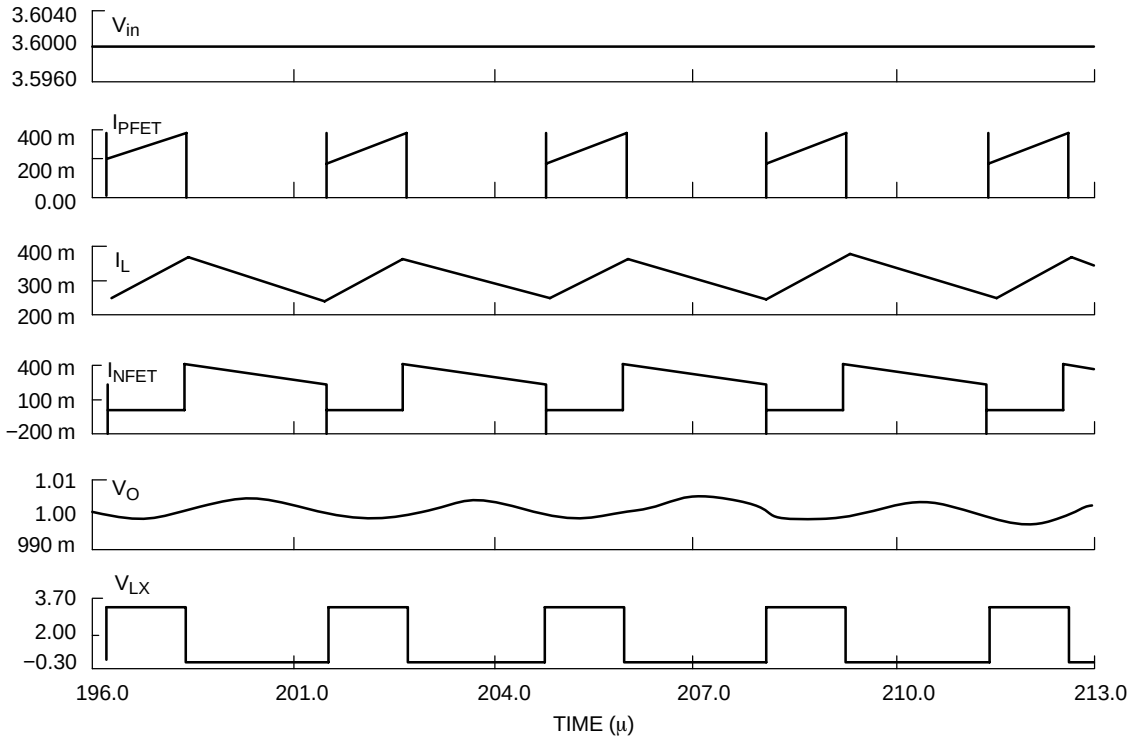


Figure 4. Waveforms During PWM Operation

PWM Mode with Internal Oscillator

If a synchronization signal is not available, the converter has a 1.0 MHz internal oscillator available. The Sync Pin must be held high to enter this mode. The characteristics of the PWM mode with internal oscillator are similar to the Sync PWM Mode.

Pulsed Mode

During low−level current output, NCP1509 can enter a low current consumption mode when the Sync Pin is held low. This mode will typically have a free running frequency and an output voltage ripple similar to a PFM mode. The advantage of the Pulsed mode is much lower Iq (14 μA) and drastically higher efficiency compared with PWM and PFM modes in low output loads.

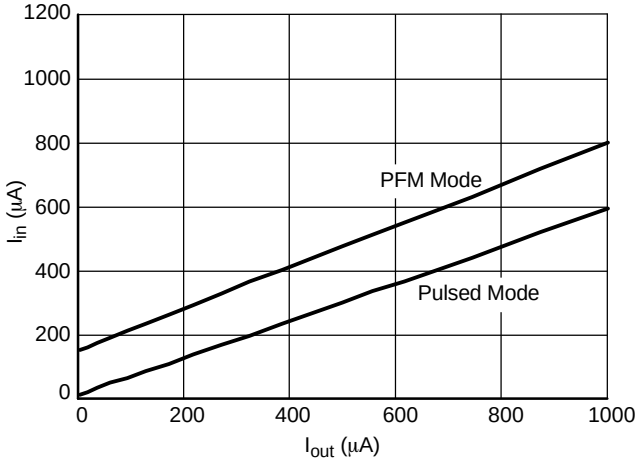


Figure 5. Input Current Comparison for V_{in} = 3.6 V and V_{out} = 1.57 V

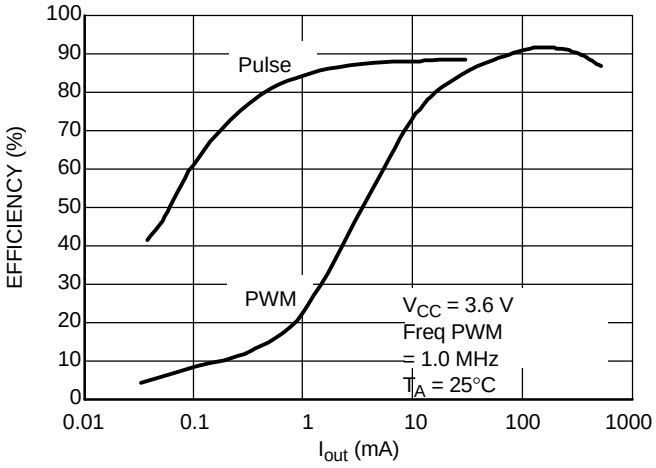


Figure 6. PWM versus Pulse Efficiency Comparison

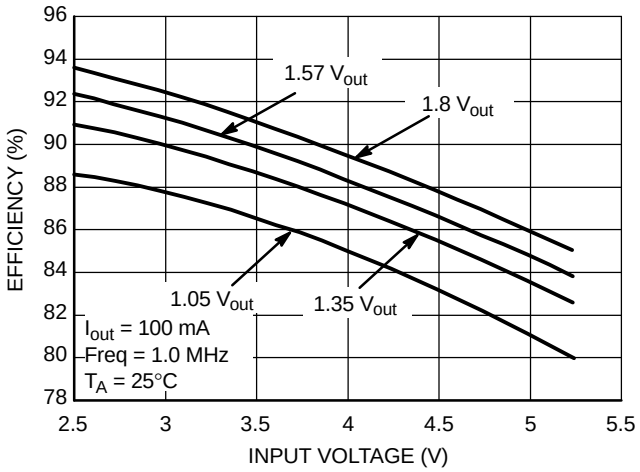


Figure 7. Converter Efficiency versus Input Voltage in PWM Mode

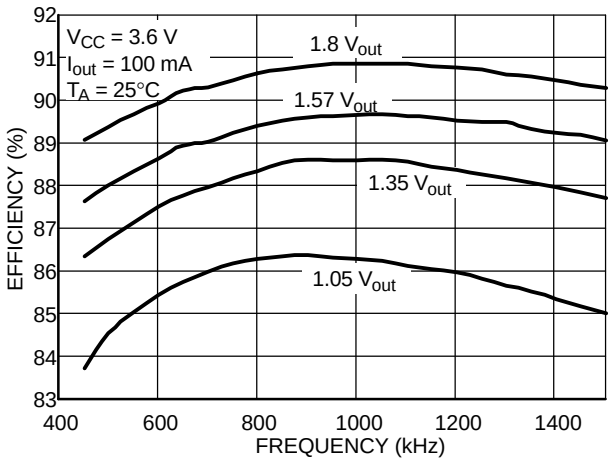


Figure 8. Converter Efficiency versus Operational Frequency in PWM Mode

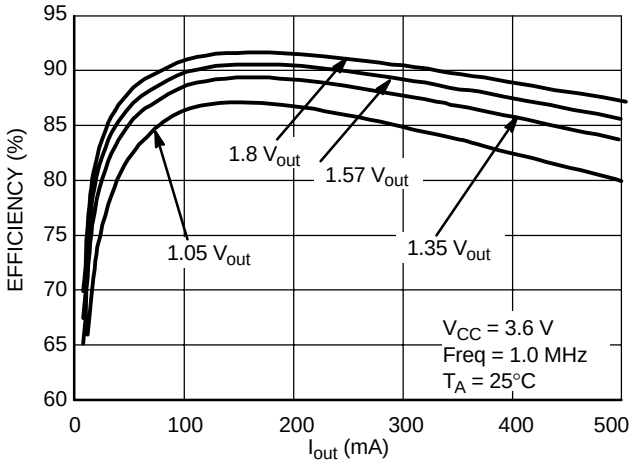


Figure 9. Converter Efficiency versus Output Current in PWM Mode

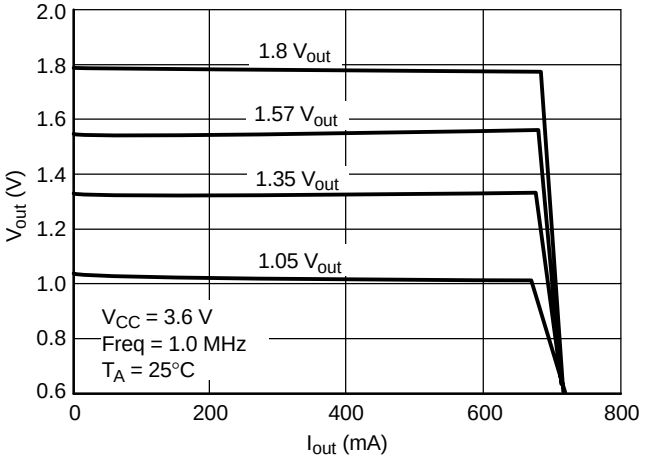


Figure 10. Output Voltage versus Output Current in PWM Mode

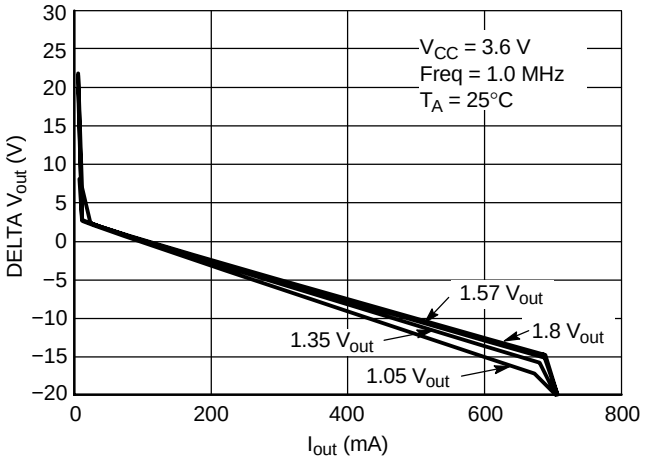


Figure 11. Output Voltage Delta versus Output Current in PWM Mode

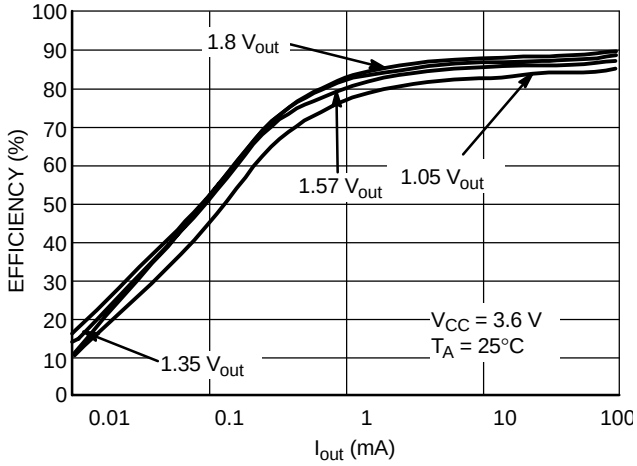


Figure 12. Converter Efficiency versus Input Current in Pulsed Mode

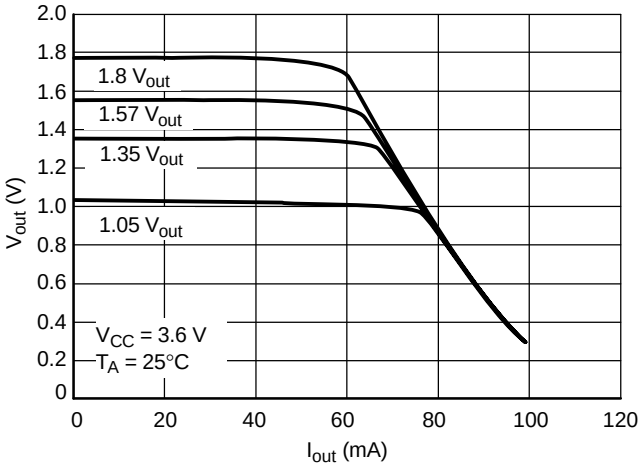


Figure 13. Output Voltage versus Output Current in Pulsed Mode

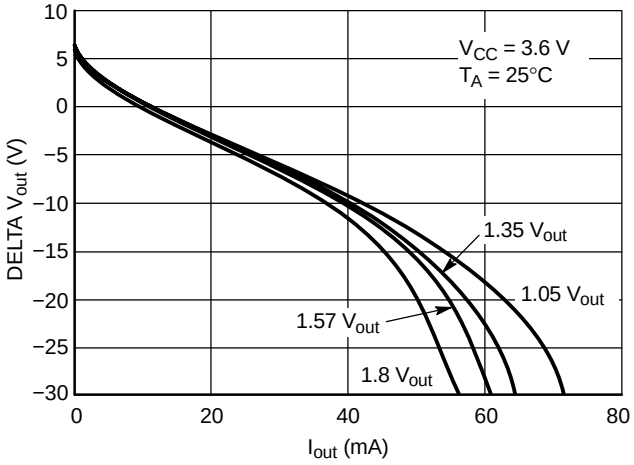


Figure 14. Output Voltage Delta versus Output Current in Pulsed Mode

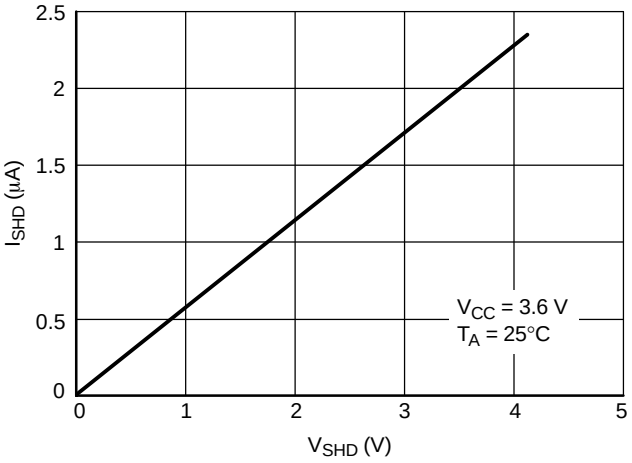


Figure 15. Input Current versus Voltage for the Shutdown Pin

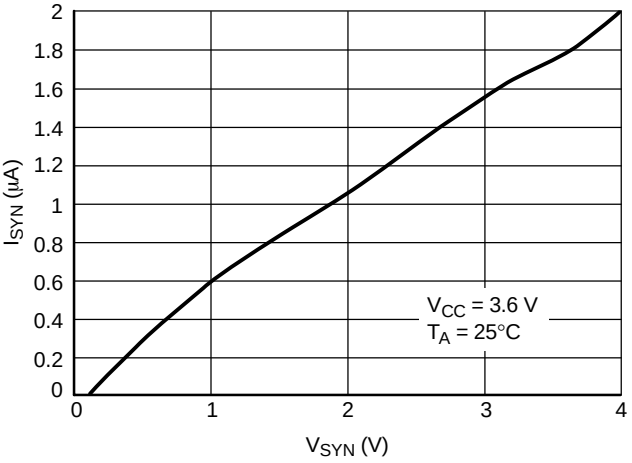


Figure 16. Input Current versus Voltage for the Synchronization Pin

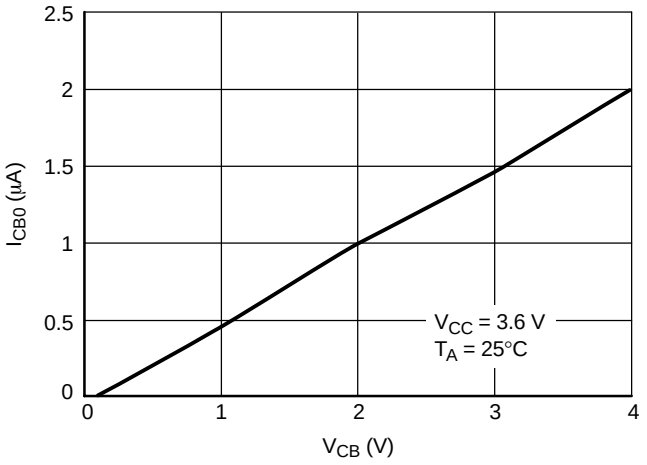


Figure 17. Input Current versus Voltage for CB0

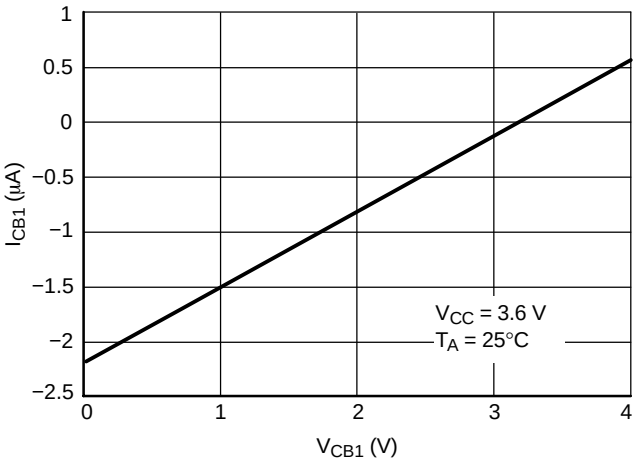


Figure 18. Input Current versus Input Voltage for CB1

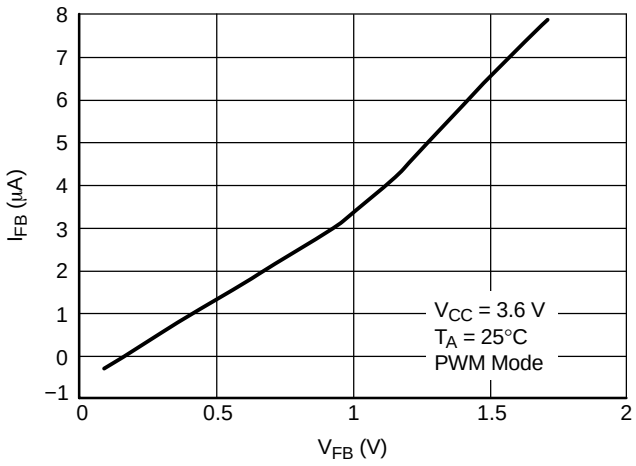


Figure 19. Input Current versus Voltage for the Feedback Pin

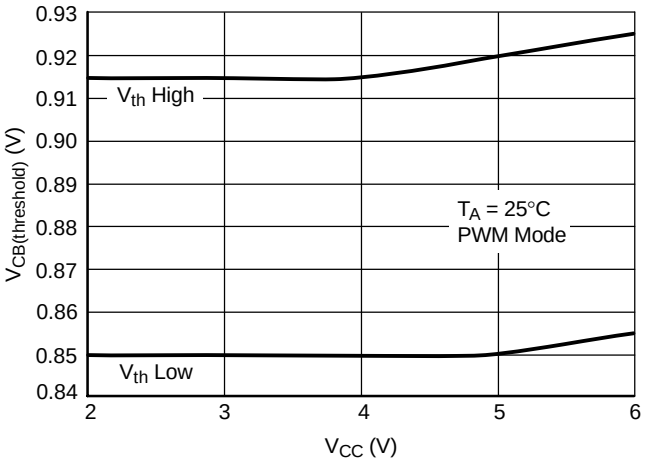


Figure 20. V_{CC} Input Voltage versus CB Threshold

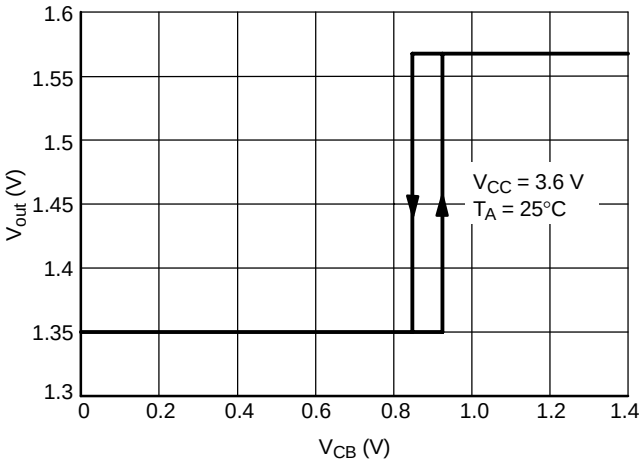


Figure 21. Transition Level of CB Pins

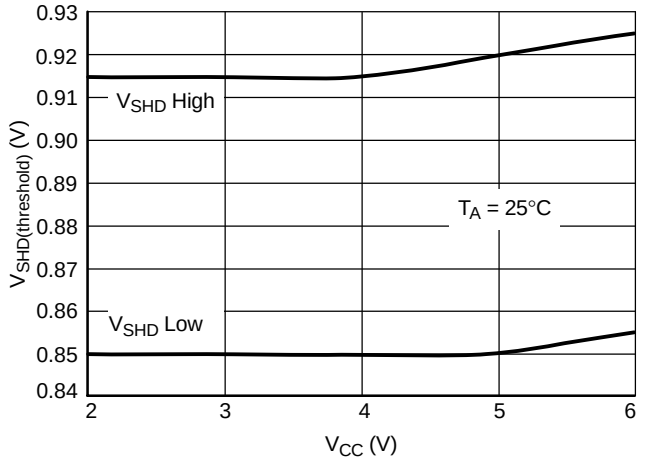


Figure 22. Input Voltage versus Shutdown Voltage

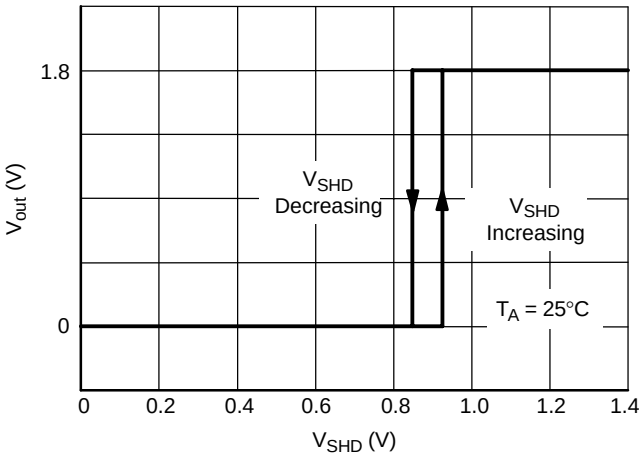
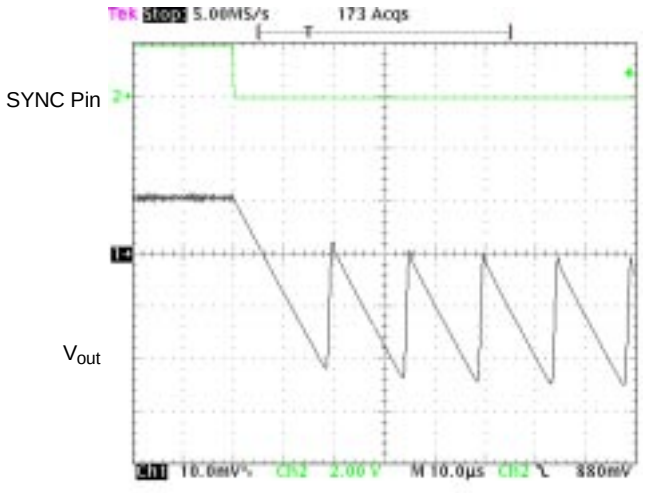
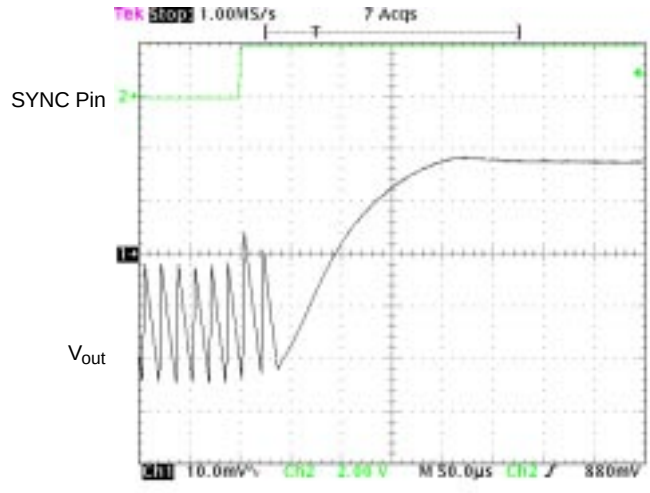


Figure 23. Output Voltage versus Shutdown Pin Voltage



V_{CC} = 3.6 V, I_{out} = 10 mA, T_A = 25°C

Figure 24. PWM Mode to Pulsed Mode Transition



V_{CC} = 3.6 V, I_{out} = 10 mA, T_A = 25°C

Figure 25. Pulsed Mode to PWM Mode Transition

INRUSH CURRENT MEASUREMENTS

CH4: Iin (20 mA/div)

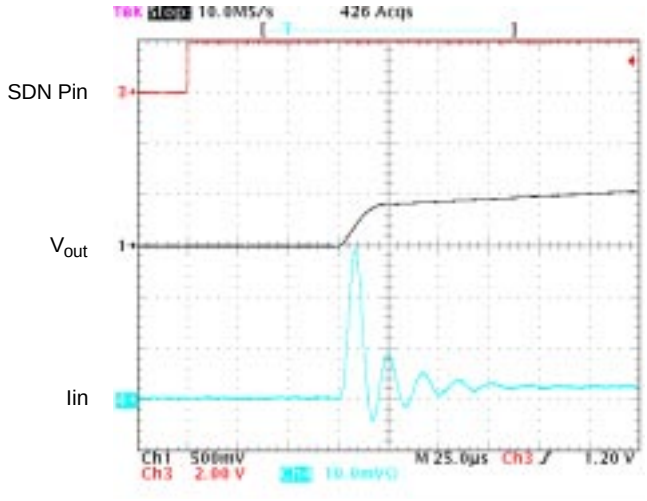


Figure 26. PWM Startup Inrush Current – 400 Ω Load, 1.57 V_{out}

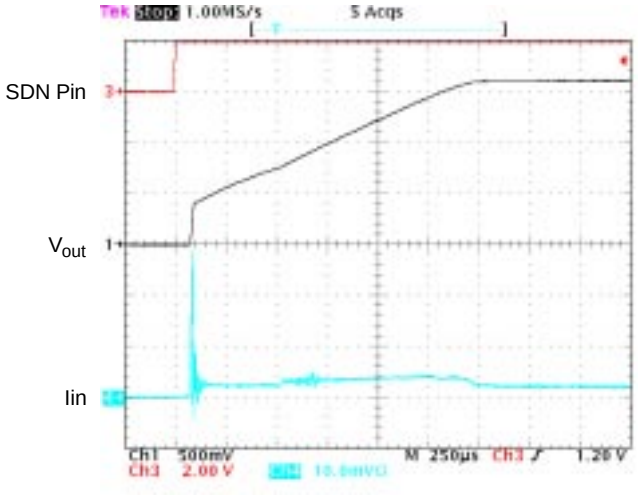


Figure 27. PWM Startup Inrush Current – 400 Ω Load, 1.57 V_{out}

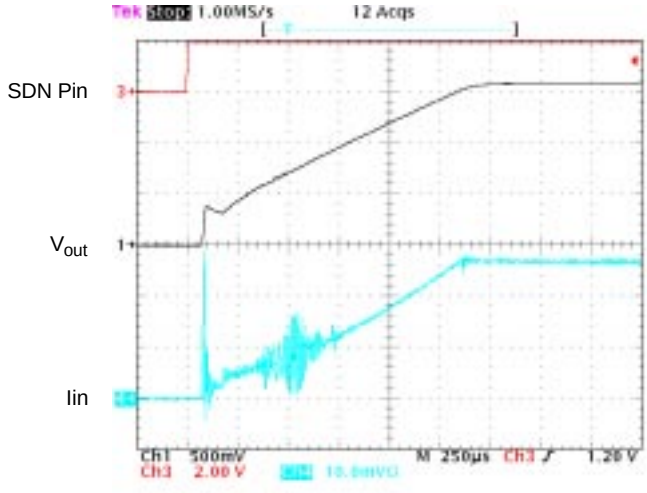


Figure 28. PWM Startup Inrush Current – 10 Ω Load, 1.57 V_{out}

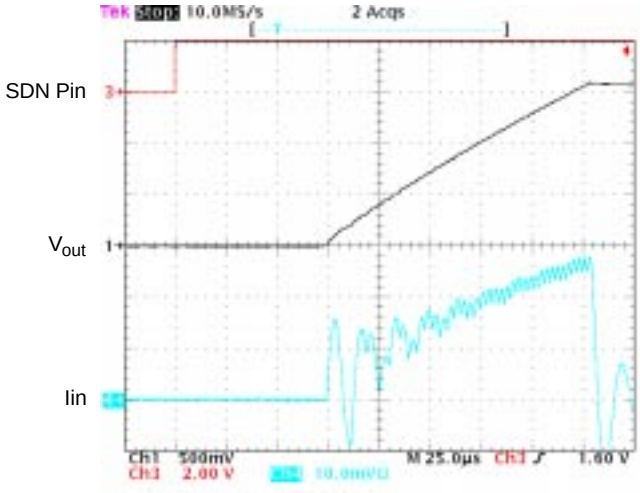


Figure 29. Pulse Startup Inrush Current – 400 Ω Load, 1.57 V_{out}

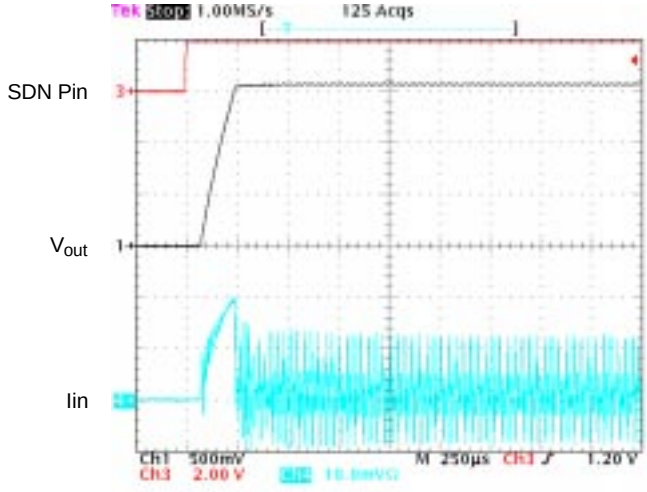


Figure 30. Pulse Startup Inrush Current – 400 Ω Load, 1.57 V_{out}

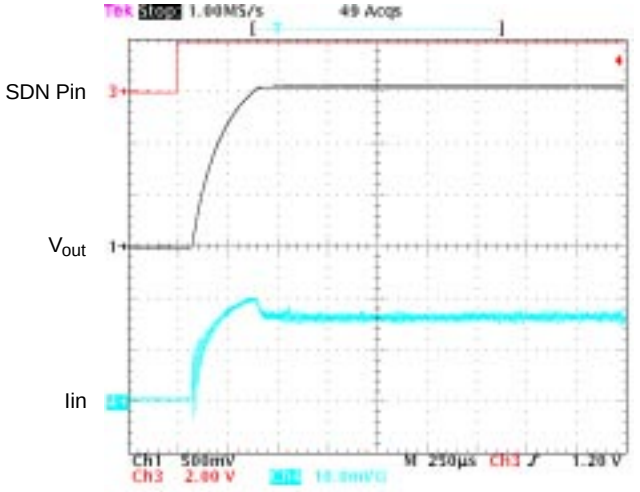


Figure 32. Pulse Startup Inrush Current – 25 Ω Load, 1.57 V_{out}

DYNAMIC VOLTAGE MANAGEMENT

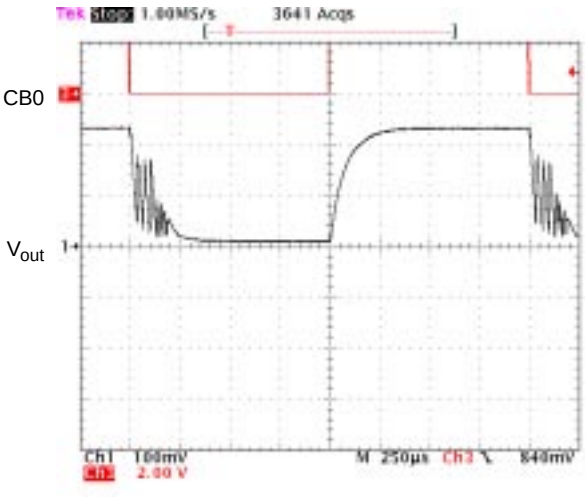


Figure 33. PWM DVM – 30 Ω Load, 1.35 to 1.57 V_{out}

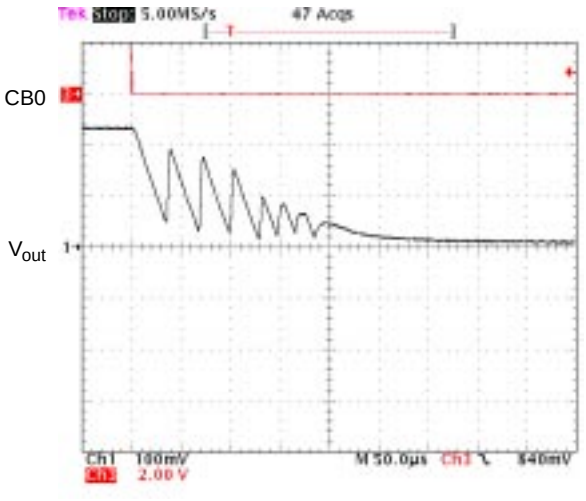


Figure 34. PWM DVM – 30 Ω Load, 1.35 to 1.57 V_{out}

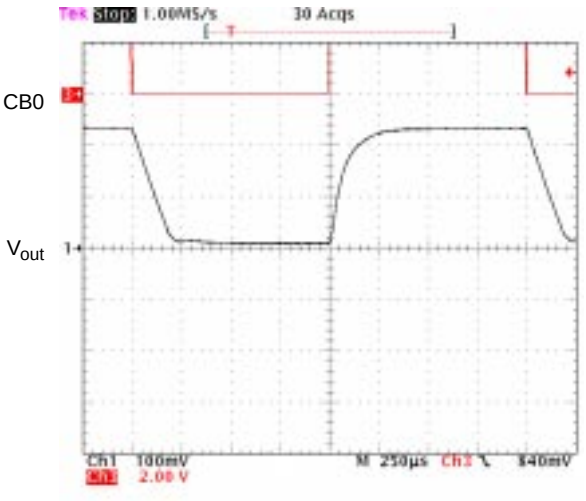


Figure 35. PWM DVM – 150 Ω Load, 1.35 to 1.57 V_{out}

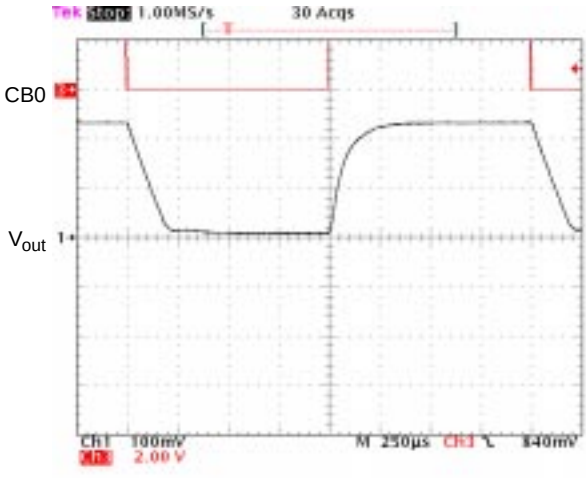


Figure 36. PWM DVM – 150 Ω Load, 1.35 to 1.57 V_{out}

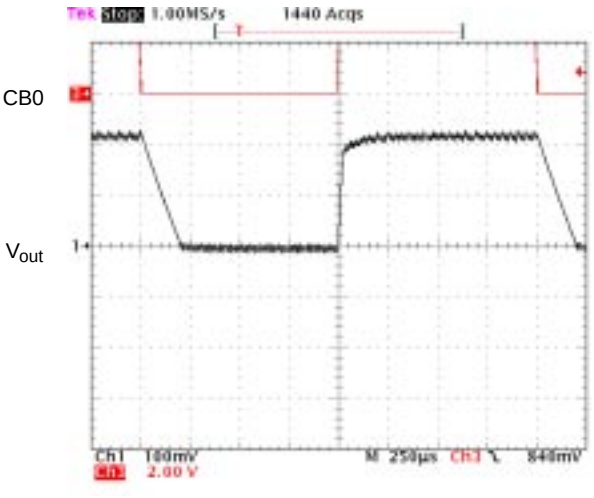


Figure 37. Pulse DVM – 150 Ω Load, 1.35 to 1.57 V_{out}

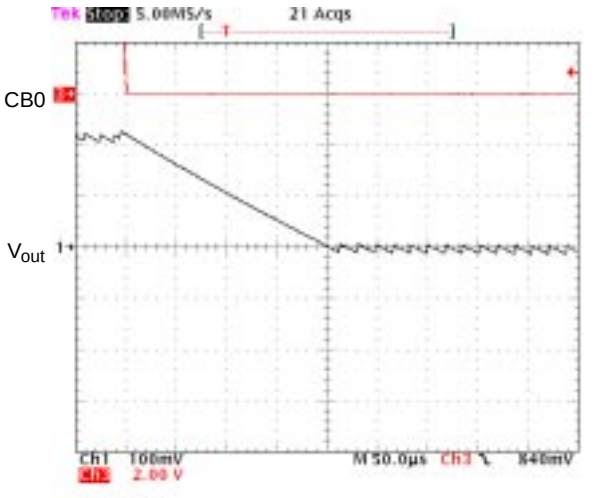


Figure 38. Pulse DVM – 150 Ω Load, 1.35 to 1.57 V_{out}

Voltage Output Selection

The CB1 and CB0 pins control the output voltage selection. The output voltages are listed in Table 2. The CB pins contain internal resistors to force the NCP1509 to 1.35 V_{out} if they are not connected to an external circuit. The CB0 has a pull down resistor and the CB1 has a pull up resistor. The CB Pin thresholds are fixed as noted in the Electrical Characteristics table.

Shutdown Pin

The Shutdown Pin enables the operation of the device. The Shutdown Pin has an internal pull down resistor to force the NCP1509 into the off mode if this pin is floating due to the external circuit. The Shutdown Pin threshold is fixed as noted in the Electrical Characteristics table. During Start−up, the NCP1509 has a soft start function to limit fast dV/dt and eliminate overshoot on the output.

Thermal Shutdown

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event at the maximum junction temperature is exceeded. When activated, typically at 160°C, the PWM latch is reset and the linear regulator control circuitry is disabled. The thermal shutdown circuit is designed with 25°C of hysteresis. This means that the PWM latch and the regulator control circuitry cannot be re−enabled until the die temperature drops by this amount. This feature is provided to prevent catastrophic failures from accidental device overheating. **It is not intended as a substitute for proper heat−sinking.**

Table 2. Truth Table for CB0 and CB1 with the Corresponding Output Voltage

CB0	CB1	V_{out} (V)
0	0	1.05
0	1	1.35
1	1	1.57
1	0	1.8

Design Example

First, determine the normal operating conditions of the NCP1509. If one assumes that the NCP1509 is used in a single lithium−ion battery application, the input voltage, V_{in}, is 3.0 V to 4.2 V. Next determine which output voltage is required. Output conditions for this example will be V_{out} at 1.8 V with a typical load current of 120 mA and a maximum of 300 mA.

Since the compensation is fixed internally in the IC, the inductance as well as the input and output capacitors have a predetermined value. The input and output capacitors are 10 μF. The ESR of the capacitors needs to be as low as possible, therefore, it is recommended that one uses a ceramic capacitor. The inductor must be 6.8 μH. The series resistance of the inductor only factors into the overall efficiency of the converter. The inductor needs to be selected by the peak current required.

Equation 1 is the basic equation for an inductor and can derive Equations 2 and 3. The equation describes the voltage across the inductor and the inductance value determines the slope of the current of the inductor.

$$\frac{V}{L} = \frac{di}{dt} \qquad \text{(eq. 1)}$$

Equation 1 is rearranged to solve for the change in current for the on−time of the converter in Continuous Conduction Mode.

$$i_{Lpk-pk} = \frac{(V_{in} - V_{out})}{L} * t_{on} \qquad \text{(eq. 2)}$$

The only unknown of Equation 2 is the on−time. For a steady state condition at maximum load, the di and L are equal during the on−time and off−time. Manipulating Equation 1 yields the following.

$$t_{on} = \frac{V_{in}}{V_{out}} * \frac{1}{f} \qquad \text{(eq. 3)}$$

Utilizing Equations 2 and 3, the peak inductor current is calculated. The following worst case conditions are used for the calculations.

$$V_{IN\ MAX} = 4.2\ V$$
$$V_{OUT} = 1.8\ V$$
$$Freq = 1.0\ MHz - 20\%$$
$$L = 6.8\ \mu H - 10\%$$

These values result in the following.

$$t_{on} = 536\ nsec$$
$$i_{Lpk-pk} = 211\ mA$$

The maximum current in the inductor is half of the peak to peak value plus the maximum DC current in the load. The inductor must have a maximum current exceeding 405 mA.

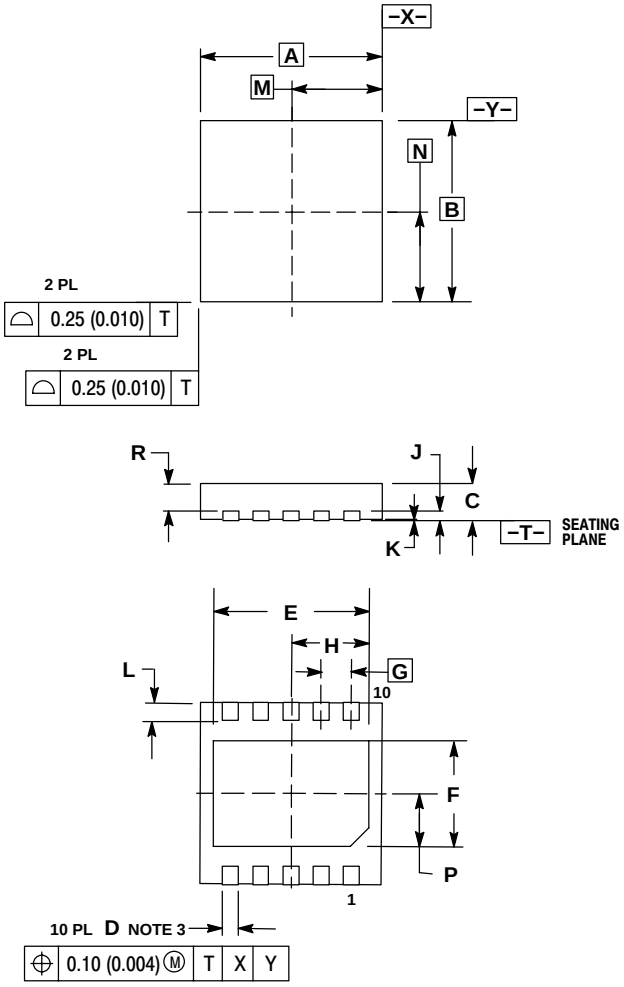
PC Board Layout Criteria

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the NCP1509.

1. Place C_{in} as close as possible to the V_{CC} and GND pins. This will minimize the AC noise into the Reference and Analog Circuitry of the IC generated by the switching in the MOSFETs.
2. Keep the GND connections of the capacitors as close as possible.
3. The power traces should be short and wide as possible.

PACKAGE DIMENSIONS

10 PIN DFN
MN SUFFIX
CASE 485C−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION D APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	3.00 BSC		0.118 BSC	
B	3.00 BSC		0.118 BSC	
C	0.80	1.00	0.031	0.039
D	0.20	0.30	0.008	0.012
E	2.45	2.55	0.096	0.100
F	1.75	1.85	0.069	0.073
G	0.50 BSC		0.020 BSC	
H	1.23	1.28	0.048	0.050
J	0.20 REF		0.008 REF	
K	0.00	0.05	0.000	0.002
L	0.35	0.45	0.014	0.018
M	1.50 BSC		0.059 BSC	
N	1.50 BSC		0.059 BSC	
P	0.88	0.93	0.035	0.037
R	0.60	0.80	0.024	0.031

For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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NCP1509/D