74VCX162240

Low-Voltage 1.8/2.5/3.3V 16-Bit Buffer

With 26 Ω Series Resistors 3.6 V–Tolerant Inputs and Outputs (3–State, Inverting)

The 74VCX162240 is an advanced performance, inverting 16–bit buffer. It is designed for very high–speed, very low–power operation in 1.8 V, 2.5 V or 3.3 V systems.

When operating at 2.5 V (or 1.8 V) the part is designed to tolerate voltages it may encounter on either inputs or outputs when interfacing to 3.3 V busses. It is guaranteed to be over–voltage tolerant to 3.6 V.

The 74VCX162240 is nibble controlled with each nibble functioning identically, but independently. It is designed with 26 Ω series resistors in each of the outputs to reduce noise. The control pins may be tied together to obtain full 16–bit operation. The 3–state outputs are controlled by an Output Enable ($\overline{OEn}$) input for each nibble. When $\overline{OEn}$ is LOW, the outputs are on. When $\overline{OEn}$ is HIGH, the outputs are in the high impedance state.

- Designed for Low Voltage Operation: $V_{CC} = 1.65$–3.6 V
- 3.6 V Tolerant Inputs and Outputs
- High Speed Operation: 3.3 ns max for 3.0 to 3.6 V
  3.8 ns max for 2.3 to 2.7 V
  7.6 ns max for 1.65 to 1.95 V
- Static Drive: ±12 mA Drive at 3.0 V
  ±8 mA Drive at 2.3 V
  ±3 mA Drive at 1.65 V
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When $V_{CC} = 0$ V
- Near Zero Static Supply Current in All Three Logic States (20 μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds ±300 mA @ 125°C
- ESD Performance: Human Body Model >2000 V; Machine Model >200 V

ON Semiconductor
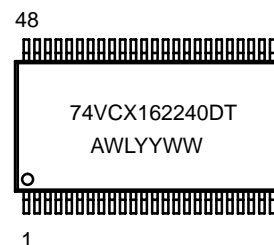
MARKING DIAGRAM

48
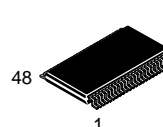
**TSSOP–48
DT SUFFIX
CASE 1201**

48

74VCX162240DT
AWLYYWW

1

A   = Assembly Location
WL = Wafer Lot
YY   = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
74VCX162240DT	TSSOP	39 / Rail
74VCX162240DTR	TSSOP	2500 / Reel

74VCX162240
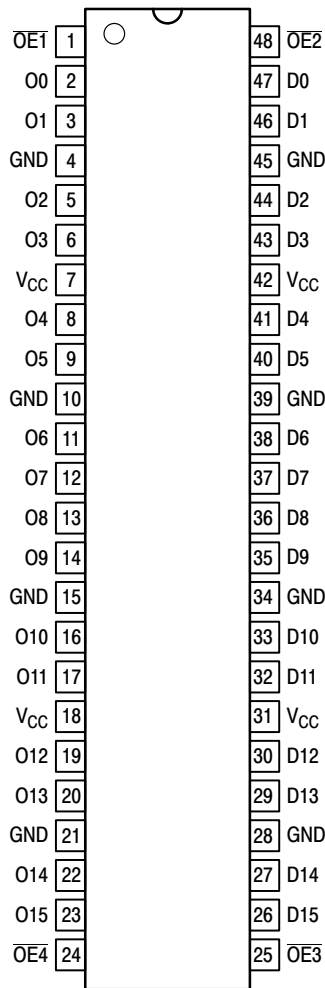
Figure 1. 48–Lead Pinout
(Top View)

Figure 2. Logic Diagram

PIN NAMES

Pins	Function
$\overline{OEn}$ D0–D15 O0–O15	Output Enable Inputs Inputs Outputs
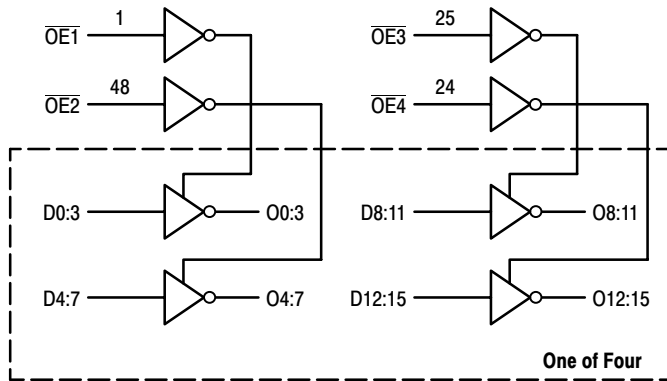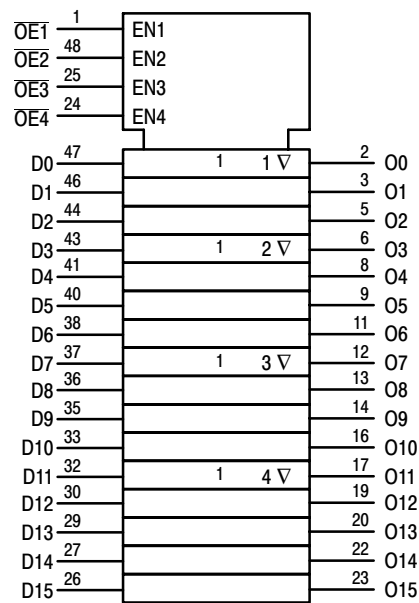
$\overline{OE1}$	D0:3	O0:3	$\overline{OE2}$	D4:7	O4:7	$\overline{OE3}$	D8:11	O8:11	$\overline{OE4}$	D12:15	O12:15
L	L	L	L	L	L	L	L	L	L	L	L
L	H	H	L	H	H	L	H	H	L	H	H
H	X	Z	H	X	Z	H	X	Z	H	X	Z

H = High Voltage Level; L = Low Voltage Level; Z = High Impedance State; X = High or Low Voltage Level and Transitions Are Acceptable, for I_{CC} reasons, DO NOT FLOAT Inputs

74VCX162240

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	−0.5 to +4.6		V
V_I	DC Input Voltage	$−0.5 \le V_I \le +4.6$		V
V_O	DC Output Voltage	$−0.5 \le V_O \le +4.6$	Output in 3–State	V
		$−0.5 \le V_O \le V_{CC} + 0.5$	Note 1.; Outputs Active	V
I_{IK}	DC Input Diode Current	−50	$V_I < GND$	mA
I_{OK}	DC Output Diode Current	−50	$V_O < GND$	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current Per Supply Pin	±100		mA
I_{GND}	DC Ground Current Per Ground Pin	±100		mA
T_{STG}	Storage Temperature Range	−65 to +150		°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

1. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	Operating Data Retention Only	1.65 1.2	3.3	3.6 3.6	V
V_I	Input Voltage		−0.3		3.6	V
V_O	Output Voltage	(Active State) (3–State)	0 0		V_{CC} 3.6	V
I_{OH}	HIGH Level Output Current, V_{CC} = 3.0V – 3.6V				−12	mA
I_{OL}	LOW Level Output Current, V_{CC} = 3.0V – 3.6V				12	mA
I_{OH}	HIGH Level Output Current, V_{CC} = 2.3V – 2.7V				−8	mA
I_{OL}	LOW Level Output Current, V_{CC} = 2.3V – 2.7V				8	mA
I_{OH}	HIGH Level Output Current, V_{CC} = 1.65V – 1.95V				−3	mA
I_{OL}	LOW Level Output Current, V_{CC} = 1.65V – 1.95V				3	mA
T_A	Operating Free–Air Temperature		−40		+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8V to 2.0V, V_{CC} = 3.0V		0		10	ns/V

74VCX162240

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	$T_A = -40°C$ to $+85°C$ Min	$T_A = -40°C$ to $+85°C$ Max	Unit
V_{IH}	HIGH Level Input Voltage (Note 2.)	$1.65V \leq V_{CC} < 2.3V$	$0.65 \times V_{CC}$		V
		$2.3V \leq V_{CC} \leq 2.7V$	1.6		
		$2.7V < V_{CC} \leq 3.6V$	2.0		
V_{IL}	LOW Level Input Voltage (Note 2.)	$1.65V \leq V_{CC} < 2.3V$		$0.35 \times V_{CC}$	V
		$2.3V \leq V_{CC} \leq 2.7V$		0.7	
		$2.7V < V_{CC} \leq 3.6V$		0.8	
V_{OH}	HIGH Level Output Voltage	$1.65V \leq V_{CC} \leq 3.6V; I_{OH} = -100µA$	$V_{CC} - 0.2$		V
		$V_{CC} = 1.65V; I_{OH} = -3mA$	1.25		
		$V_{CC} = 2.3V; I_{OH} = -4mA$	2.0		
		$V_{CC} = 2.3V; I_{OH} = -6mA$	1.8		
		$V_{CC} = 2.3V; I_{OH} = -8mA$	1.7		
		$V_{CC} = 2.7V; I_{OH} = -6mA$	2.2		
		$V_{CC} = 3.0V; I_{OH} = -8mA$	2.4		
		$V_{CC} = 3.0V; I_{OH} = -12mA$	2.2		
V_{OL}	LOW Level Output Voltage	$1.65V \leq V_{CC} \leq 3.6V; I_{OL} = 100µA$		0.2	V
		$V_{CC} = 1.65V; I_{OL} = 3mA$		0.3	
		$V_{CC} = 2.3V; I_{OL} = 6mA$		0.4	
		$V_{CC} = 2.3V; I_{OL} = 8mA$		0.6	
		$V_{CC} = 2.7V; I_{OL} = 6mA$		0.4	
		$V_{CC} = 3.0V; I_{OL} = 8mA$		0.55	
		$V_{CC} = 3.0V; I_{OL} = 12mA$		0.8	
I_I	Input Leakage Current	$1.65V \leq V_{CC} \leq 3.6V; 0V \leq V_I \leq 3.6V$		±5.0	µA
I_{OZ}	3–State Output Current	$1.65V \leq V_{CC} \leq 3.6V; 0V \leq V_O \leq 3.6V;$ $V_I = V_{IH}$ or V_{IL}		±10	µA
I_{OFF}	Power–Off Leakage Current	$V_{CC} = 0V; V_I$ or $V_O = 3.6V$		10	µA
I_{CC}	Quiescent Supply Current (Note 3.)	$1.65V \leq V_{CC} \leq 3.6V; V_I = GND$ or V_{CC}		20	µA
		$1.65V \leq V_{CC} \leq 3.6V; 3.6V \leq V_I, V_O \leq 3.6V$		±20	µA
ΔI_{CC}	Increase in I_{CC} per Input	$2.7V < V_{CC} \leq 3.6V; V_{IH} = V_{CC} - 0.6V$		750	µA

2. These values of V_I are used to test DC electrical characteristics only.
3. Outputs disabled or 3–state only.

AC CHARACTERISTICS (Note 4.; $t_R = t_F = 2.0ns$; $C_L = 30pF$; $R_L = 500Ω$)

Symbol	Parameter	Waveform	$V_{CC} = 3.0V$ to $3.6V$ Min	$V_{CC} = 3.0V$ to $3.6V$ Max	$V_{CC} = 2.3V$ to $2.7V$ Min	$V_{CC} = 2.3V$ to $2.7V$ Max	$V_{CC} = 1.65$ to $1.95V$ Min	$V_{CC} = 1.65$ to $1.95V$ Max	Unit
t_{PLH} t_{PHL}	Propagation Delay Input to Output	1	0.8 0.8	3.3 3.3	1.0 1.0	3.8 3.8	1.5 1.5	7.6 7.6	ns
t_{PZH} t_{PZL}	Output Enable Time to High and Low Level	2	0.8 0.8	3.8 3.8	1.0 1.0	5.1 5.1	1.5 1.5	9.8 9.8	ns
t_{PHZ} t_{PLZ}	Output Disable Time From High and Low Level	2	0.8 0.8	3.6 3.6	1.0 1.0	4.0 4.0	1.5 1.5	7.2 7.2	ns
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 5.)			0.5 0.5		0.5 0.5		0.75 0.75	ns

Limits / $T_A = -40°C$ to $+85°C$

4. For $C_L = 50pF$, add approximately 300ps to the AC maximum specification.
5. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

74VCX162240

DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = +25°C Typ	Unit
V_{OLP}	Dynamic LOW Peak Voltage (Note 6.)	V_{CC} = 1.8V, C_L = 30pF, V_{IH} = V_{CC}, V_{IL} = 0V	0.15	V
		V_{CC} = 2.5V, C_L = 30pF, V_{IH} = V_{CC}, V_{IL} = 0V	0.25	
		V_{CC} = 3.3V, C_L = 30pF, V_{IH} = V_{CC}, V_{IL} = 0V	0.35	
V_{OLV}	Dynamic LOW Valley Voltage (Note 6.)	V_{CC} = 1.8V, C_L = 30pF, V_{IH} = V_{CC}, V_{IL} = 0V	−0.15	V
		V_{CC} = 2.5V, C_L = 30pF, V_{IH} = V_{CC}, V_{IL} = 0V	−0.25	
		V_{CC} = 3.3V, C_L = 30pF, V_{IH} = V_{CC}, V_{IL} = 0V	−0.35	
V_{OHV}	Dynamic HIGH Valley Voltage (Note 7.)	V_{CC} = 1.8V, C_L = 30pF, V_{IH} = V_{CC}, V_{IL} = 0V	1.55	V
		V_{CC} = 2.5V, C_L = 30pF, V_{IH} = V_{CC}, V_{IL} = 0V	2.05	
		V_{CC} = 3.3V, C_L = 30pF, V_{IH} = V_{CC}, V_{IL} = 0V	2.65	

6. Number of outputs defined as "n". Measured with "n–1" outputs switching from HIGH–to–LOW or LOW–to–HIGH. The remaining output is measured in the LOW state.
7. Number of outputs defined as "n". Measured with "n–1" outputs switching from HIGH–to–LOW or LOW–to–HIGH. The remaining output is measured in the HIGH state.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{IN}	Input Capacitance	Note 8.	6	pF
C_{OUT}	Output Capacitance	Note 8.	7	pF
C_{PD}	Power Dissipation Capacitance	Note 8., 10MHz	20	pF

8. V_{CC} = 1.8, 2.5 or 3.3V; V_I = 0V or V_{CC}.

74VCX162240
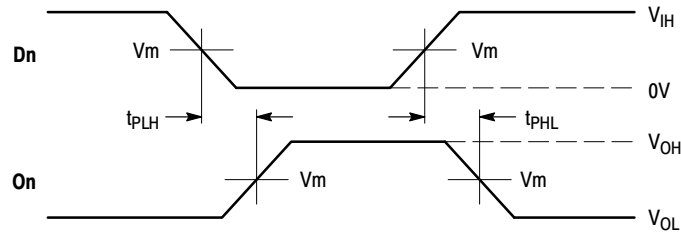
WAVEFORM 1 – PROPAGATION DELAYS
$t_R = t_F = 2.0ns$, 10% to 90%; f = 1MHz; $t_W = 500ns$
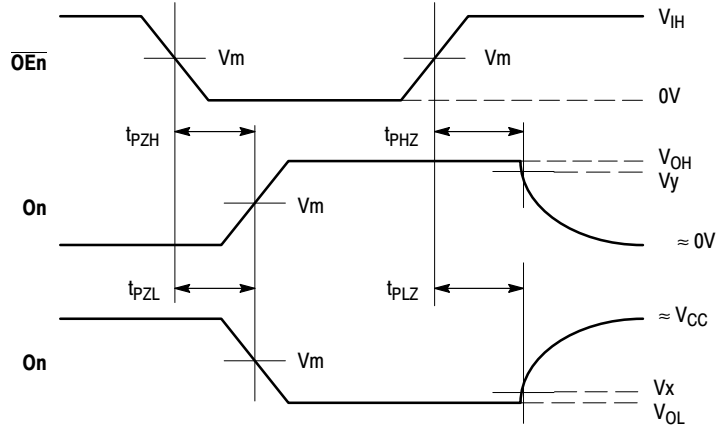
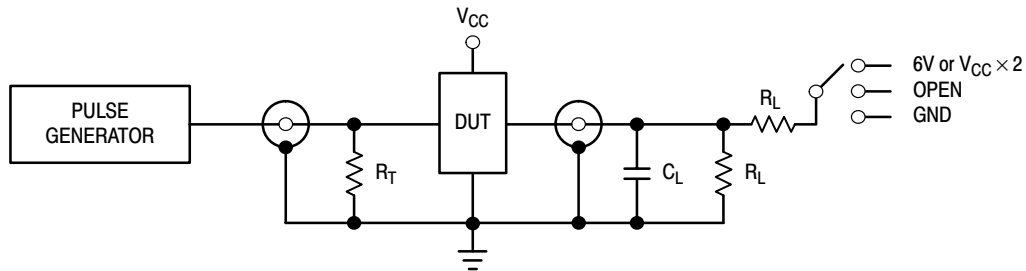**WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES**
$t_R = t_F = 2.0ns$, 10% to 90%; f = 1MHz; $t_W = 500ns$

Figure 3. AC Waveforms

Symbol	V_{CC}		
	3.3V ±0.3V	2.5V ±0.2V	1.8V ±0.15V
V_{IH}	2.7V	V_{CC}	V_{CC}
V_m	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_x	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$	$V_{OL} + 0.15V$
V_y	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$	$V_{OH} - 0.15V$

TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at V_{CC} = 3.3 ±0.3V; $V_{CC} \times 2$ at V_{CC} = 2.5 ±0.2V; 1.8 ±0.15V
t_{PZH}, t_{PHZ}	GND

C_L = 30pF or equivalent (Includes jig and probe capacitance)
R_L = 500Ω or equivalent
R_T = Z_{OUT} of pulse generator (typically 50Ω)

Figure 4. Test Circuit

74VCX162240
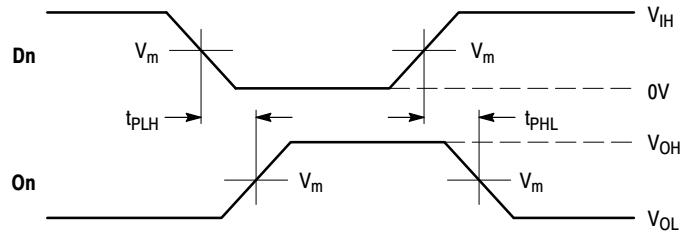
WAVEFORM 3 – PROPAGATION DELAYS
$t_R = t_F = 2.0ns$, 10% to 90%; f = 1MHz; $t_W = 500ns$
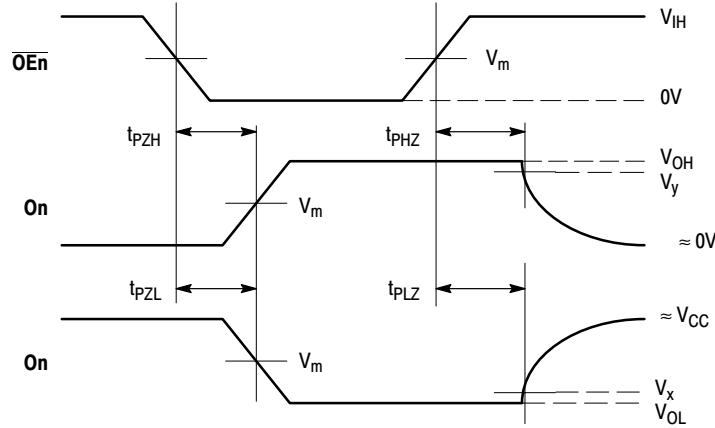
WAVEFORM 4 – OUTPUT ENABLE AND DISABLE TIMES
$t_R = t_F = 2.0ns$, 10% to 90%; f = 1MHz; $t_W = 500ns$

Figure 5. AC Waveforms

Symbol	V_{CC}	
	3.3V ±0.3V	**2.7V**
V_{IH}	2.7V	2.7V
V_m	1.5V	1.5V
V_x	$V_{OL} + 0.3V$	$V_{OL} + 0.3V$
V_y	$V_{OH} - 0.3V$	$V_{OH} - 0.3V$

TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at V_{CC} = 3.3 ±0.3V; $V_{CC} \times 2$ at V_{CC} = 2.5 ±0.2V; 1.8 ±0.15V
t_{PZH}, t_{PHZ}	GND

C_L = 50pF or equivalent (Includes jig and probe capacitance)
R_L = 500Ω or equivalent
R_T = Z_{OUT} of pulse generator (typically 50Ω)

Figure 6. Test Circuit

74VCX162240

AC CHARACTERISTICS ($t_R = t_F = 2.0ns$; $C_L = 50pF$; $R_L = 500\Omega$)

Symbol	Parameter	Waveform	Limits $T_A = -40°C$ to $+85°C$ $V_{CC} = 3.0V$ to $3.6V$		$V_{CC} = 2.7V$		Unit
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay Input to Output	3	1.0 1.0	4.2 4.2		4.7 4.7	ns
t_{PZH} t_{PZL}	Output Enable Time to High and Low Level	4	1.0 1.0	5.6 5.6		6.7 6.7	ns
t_{PHZ} t_{PLZ}	Output Disable Time From High and Low Level	4	1.0 1.0	5.5 5.5		5.7 5.7	ns
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 9.)			0.5 0.5		0.5 0.5	ns

9. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

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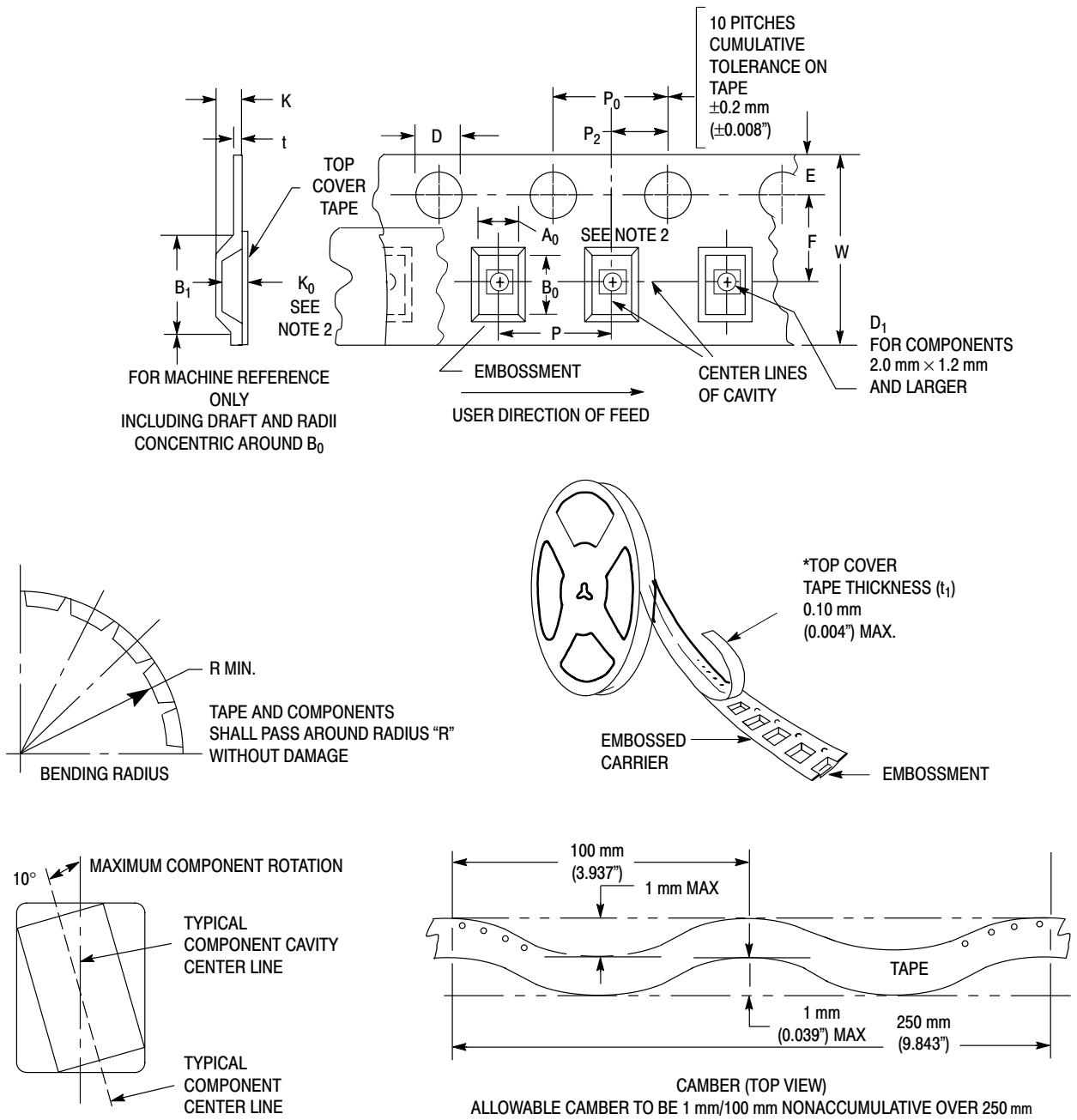
Figure 7. Carrier Tape Specifications

EMBOSSED CARRIER DIMENSIONS (See Notes 1 and 2)

Tape Size	B₁ Max	D	D₁	E	F	K	P	P₀	P₂	R	T	W
24mm	20.1mm (0.791")	1.5 + 0.1mm −0.0 (0.059 +0.004" −0.0)	1.5mm Min (0.060")	1.75 ±0.1 mm (0.069 ±0.004")	11.5 ±0.10 mm (0.453 ±0.004")	11.9 mm Max (0.468")	16.0 ±0.1 mm (0.63 ±0.004")	4.0 ±0.1 mm (0.157 ±0.004")	2.0 ±0.1 mm (0.079 ±0.004")	30 mm (1.18")	0.6 mm (0.024")	24.3 mm (0.957")

1. Metric Dimensions Govern–English are in parentheses for reference only.
2. A_0, B_0, and K_0 are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min to 0.50 mm max. The component cannot rotate more than 10° within the determined cavity
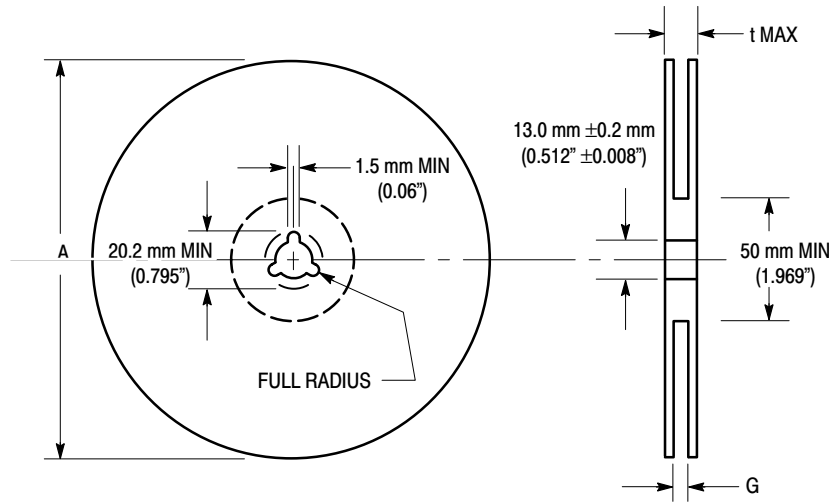
Figure 8. Reel Dimensions

REEL DIMENSIONS

Tape Size	A Max	G	t Max
24 mm	360 mm (14.173")	24.4 mm + 2.0 mm, −0.0 (0.961" + 0.078", −0.00)	30.4 mm (1.197")

DIRECTION OF FEED

BARCODE LABEL

POCKET   HOLE
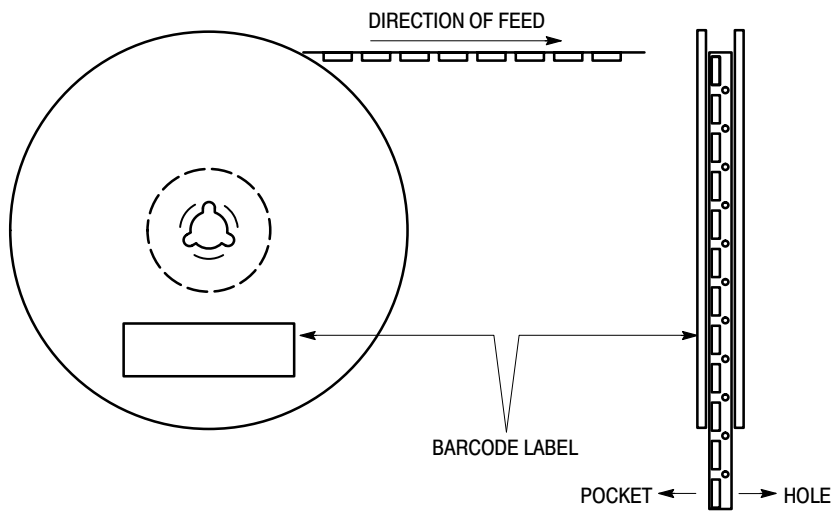
Figure 9. Reel Winding Direction

74VCX162240
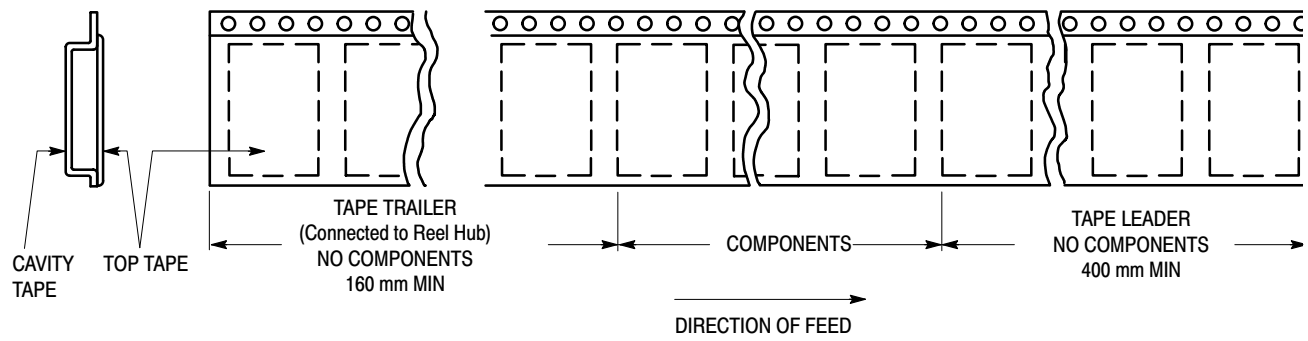
Figure 10. Tape Ends for Finished Goods

User Direction of Feed
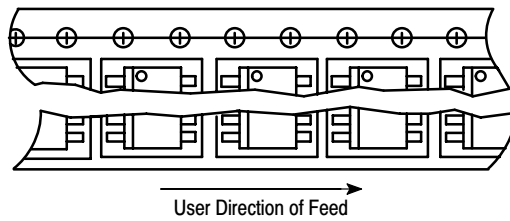
Figure 11. Reel Configuration

48 Leads

Package Footprint

74VCX162240
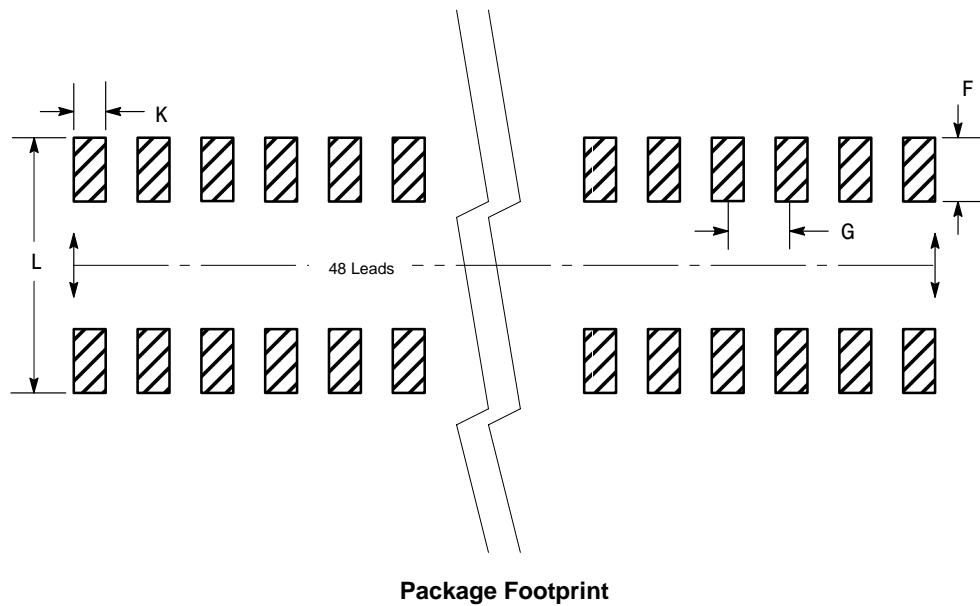
PACKAGE DIMENSIONS

TSSOP
DT SUFFIX
CASE 1201–01
ISSUE A
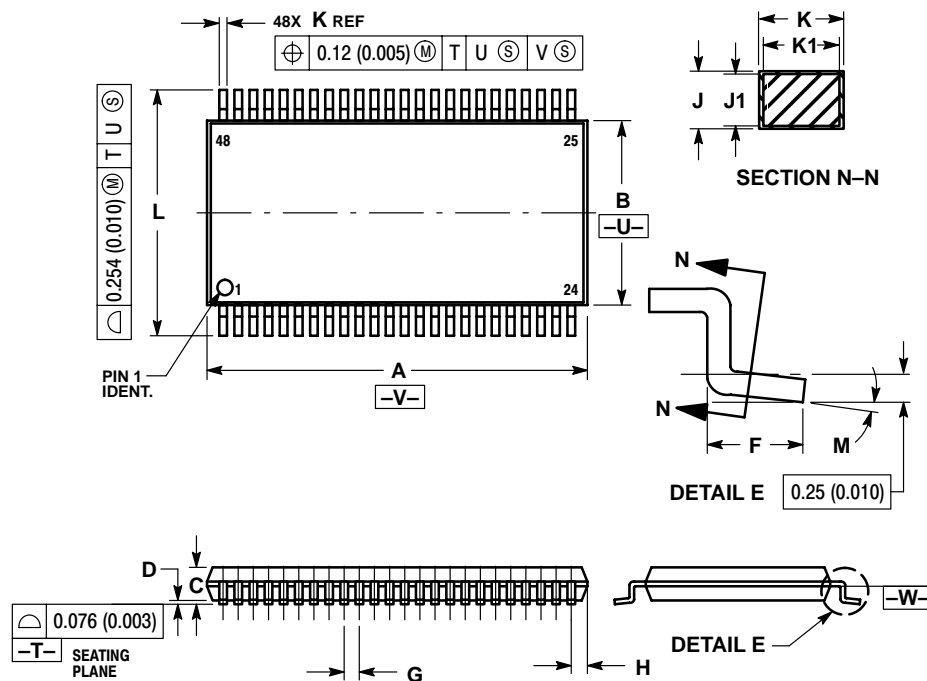
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.40	12.60	0.488	0.496
B	6.00	6.20	0.236	0.244
C	---	1.10	---	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.50 BSC		0.0197 BSC	
H	0.37	---	0.015	---
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.17	0.27	0.007	0.011
K1	0.17	0.23	0.007	0.009
L	7.95	8.25	0.313	0.325
M	0 °	8 °	0 °	8 °