

74VCX162373

Low-Voltage 1.8/2.5/3.3V 16-Bit Transparent Latch

With 26Ω Series Resistors and
3.6V-Tolerant Inputs and Outputs
(3-State, Non-Inverting)

The 74VCX162373 is an advanced performance, non-inverting 16-bit transparent latch. It is designed for very high-speed, very low-power operation in 1.8 V, 2.5 V or 3.3 V systems. The VCX162373 is byte controlled, with each byte functioning identically, but independently. Each byte has separate Output Enable and Latch Enable inputs. These control pins can be tied together for full 16-bit operation.

When operating at 2.5 V (or 1.8 V) the part is designed to tolerate voltages it may encounter on either inputs or outputs when interfacing to 3.3 V busses. It is guaranteed to be over-voltage tolerant to 3.6 V.

The 74VCX162373 contains 16 D-type latches with 3-state 3.6 V-tolerant outputs. It is designed with 26Ω series resistors in each of the outputs to reduce noise. When the Latch Enable (LEn) inputs are HIGH, data on the Dn inputs enters the latches. In this condition, the latches are transparent, (a latch output will change state each time its D input changes). When LE is LOW, the latch stores the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-state outputs are controlled by the Output Enable (OEn) inputs. When OE is LOW, the outputs are enabled. When OE is HIGH, the standard outputs are in the high impedance state, but this does not interfere with new data entering into the latches.

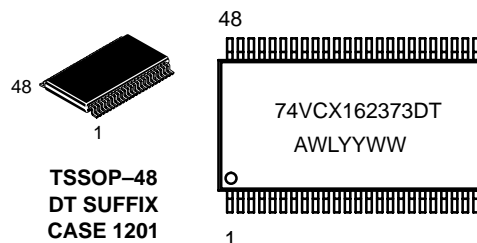
- Designed for Low Voltage Operation: $V_{CC} = 1.65\text{--}3.6\text{ V}$
- 3.6 V Tolerant Inputs and Outputs
- High Speed Operation: 3.3 ns max for 3.0 to 3.6 V
4.5 ns max for 2.3 to 2.7 V
9.0 ns max for 1.65 to 1.95 V
- Static Drive: ±12 mA Drive at 3.0 V
±8 mA Drive at 2.3 V
±3 mA Drive at 1.65 V
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When $V_{CC} = 0\text{ V}$
- Near Zero Static Supply Current in All Three Logic States (20 μA)
Substantially Reduces System Power Requirements
- Latchup Performance Exceeds ±300 mA @ 125°C
- ESD Performance: Human Body Model >2000 V; Machine Model >200 V



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MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
74VCX162373DT	TSSOP	39 / Rail
74VCX162373DTR	TSSOP	2500 / Reel

74VCX162373

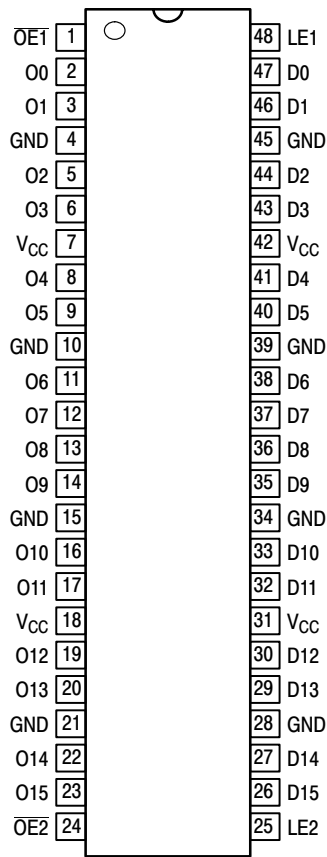


Figure 1. 48-Lead Pinout
(Top View)

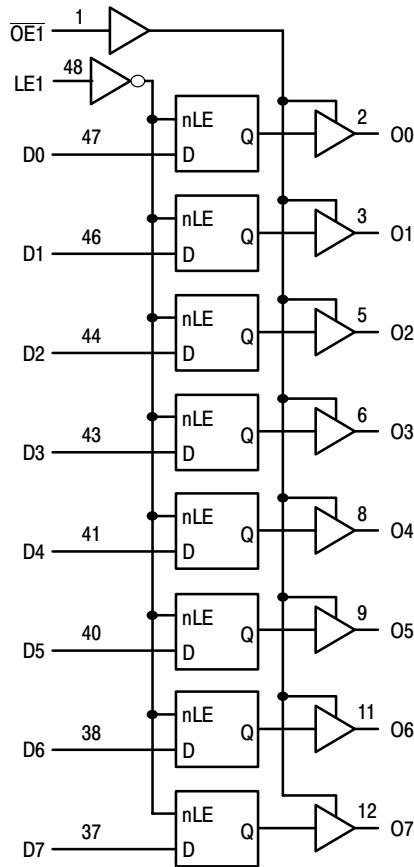
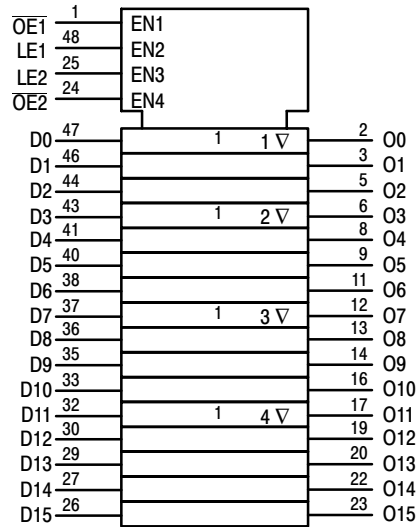


Figure 2. Logic Diagram

PIN NAMES

Pins	Function
OE _n	Output Enable Inputs
LE _n	Latch Enable Inputs
D0–D15	Inputs
O0–O15	Outputs



Inputs			Outputs		Inputs			Outputs	
LE1	OE1	D0:7	O0:7		LE2	OE2	D8:15	O8:15	
X	H	X	Z		X	H	X	Z	
H	L	L	L		H	L	L	L	
H	L	H	H		H	L	H	H	
L	L	X	O0		L	L	X	O0	

H = High Voltage Level; L = Low Voltage Level; Z = High Impedance State; X = High or Low Voltage Level and Transitions Are Acceptable, for I_{CC} reasons, DO NOT FLOAT Inputs. O0 = No Change.

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	-0.5 to +4.6		V
V_I	DC Input Voltage	$-0.5 \leq V_I \leq +4.6$		V
V_O	DC Output Voltage	$-0.5 \leq V_O \leq +4.6$	Output in 3-State	V
		$-0.5 \leq V_O \leq V_{CC} + 0.5$	Note 1.; Outputs Active	V
I_{IK}	DC Input Diode Current	-50	$V_I < GND$	mA
I_{OK}	DC Output Diode Current	-50	$V_O < GND$	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	± 50		mA
I_{CC}	DC Supply Current Per Supply Pin	± 100		mA
I_{GND}	DC Ground Current Per Ground Pin	± 100		mA
T_{STG}	Storage Temperature Range	-65 to +150		°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

1. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	1.65	3.3	3.6	V
		1.2	3.3	3.6	
V_I	Input Voltage	-0.3		3.6	V
V_O	Output Voltage	0		V_{CC}	V
		0		3.6	
I_{OH}	HIGH Level Output Current, $V_{CC} = 3.0V - 3.6V$			-12	mA
I_{OL}	LOW Level Output Current, $V_{CC} = 3.0V - 3.6V$			12	mA
I_{OH}	HIGH Level Output Current, $V_{CC} = 2.3V - 2.7V$			-8	mA
I_{OL}	LOW Level Output Current, $V_{CC} = 2.3V - 2.7V$			8	mA
I_{OH}	HIGH Level Output Current, $V_{CC} = 1.65 - 1.95V$			-3	mA
I_{OL}	LOW Level Output Current, $V_{CC} = 1.65 - 1.95V$			3	mA
T_A	Operating Free-Air Temperature	-40		+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8V to 2.0V, $V_{CC} = 3.0V$	0		10	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$		Unit
			Min	Max	
V_{IH}	HIGH Level Input Voltage (Note 2.)	$1.65\text{V} \leq V_{CC} < 2.3\text{V}$	$0.65 \times V_{CC}$		V
		$2.3\text{V} \leq V_{CC} \leq 2.7\text{V}$	1.6		
		$2.7\text{V} < V_{CC} \leq 3.6\text{V}$	2.0		
V_{IL}	LOW Level Input Voltage (Note 2.)	$1.65\text{V} \leq V_{CC} < 2.3\text{V}$		$0.35 \times V_{CC}$	V
		$2.3\text{V} \leq V_{CC} \leq 2.7\text{V}$		0.7	
		$2.7\text{V} < V_{CC} \leq 3.6\text{V}$		0.8	
V_{OH}	HIGH Level Output Voltage	$1.65\text{V} \leq V_{CC} \leq 3.6\text{V}; I_{OH} = -100\mu\text{A}$	$V_{CC} - 0.2$		V
		$V_{CC} = 1.65\text{V}; I_{OH} = -3\text{mA}$	1.25		
		$V_{CC} = 2.3\text{V}; I_{OH} = -4\text{mA}$	2.0		
		$V_{CC} = 2.3\text{V}; I_{OH} = -6\text{mA}$	1.8		
		$V_{CC} = 2.3\text{V}; I_{OH} = -8\text{mA}$	1.7		
		$V_{CC} = 2.7\text{V}; I_{OH} = -6\text{mA}$	2.2		
		$V_{CC} = 3.0\text{V}; I_{OH} = -8\text{mA}$	2.4		
		$V_{CC} = 3.0\text{V}; I_{OH} = -12\text{mA}$	2.2		
V_{OL}	LOW Level Output Voltage	$1.65\text{V} \leq V_{CC} \leq 3.6\text{V}; I_{OL} = 100\mu\text{A}$		0.2	V
		$V_{CC} = 1.65\text{V}; I_{OL} = 3\text{mA}$		0.3	
		$V_{CC} = 2.3\text{V}; I_{OL} = 6\text{mA}$		0.4	
		$V_{CC} = 2.3\text{V}; I_{OL} = 8\text{mA}$		0.6	
		$V_{CC} = 2.7\text{V}; I_{OL} = 6\text{mA}$		0.4	
		$V_{CC} = 3.0\text{V}; I_{OL} = 8\text{mA}$		0.55	
		$V_{CC} = 3.0\text{V}; I_{OL} = 12\text{mA}$		0.8	
I_I	Input Leakage Current	$1.65\text{V} \leq V_{CC} \leq 3.6\text{V}; 0\text{V} \leq V_I \leq 3.6\text{V}$		± 5.0	μA
I_{OZ}	3-State Output Current	$1.65\text{V} \leq V_{CC} \leq 3.6\text{V}; 0\text{V} \leq V_O \leq 3.6\text{V}; V_I = V_{IH} \text{ or } V_{IL}$		± 10	μA
I_{OFF}	Power-Off Leakage Current	$V_{CC} = 0\text{V}; V_I \text{ or } V_O = 3.6\text{V}$		10	μA
I_{CC}	Quiescent Supply Current (Note 3.)	$1.65\text{V} \leq V_{CC} \leq 3.6\text{V}; V_I = \text{GND or } V_{CC}$		20	μA
		$1.65\text{V} \leq V_{CC} \leq 3.6\text{V}; 3.6\text{V} \leq V_I, V_O \leq 3.6\text{V}$		± 20	μA
ΔI_{CC}	Increase in I_{CC} per Input	$2.7\text{V} < V_{CC} \leq 3.6\text{V}; V_{IH} = V_{CC} - 0.6\text{V}$		750	μA

2. These values of V_I are used to test DC electrical characteristics only.

3. Outputs disabled or 3-state only.

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AC CHARACTERISTICS (Note 4.; $t_R = t_F = 2.0\text{ns}$; $C_L = 30\text{pF}$; $R_L = 500\Omega$)

Symbol	Parameter	Waveform	Limits						Unit
			T _A = −40°C to +85°C						
			V _{CC} = 3.0V to 3.6V		V _{CC} = 2.3V to 2.7V		V _{CC} = 1.65 to 1.95V		
			Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay Dn to On	1	0.8 0.8	3.3 3.3	1.0 1.0	4.5 4.5	1.5 1.5	9.0 9.0	ns
t _{PLH} t _{PHL}	Propagation Delay LE to On	1	0.8 0.8	3.6 3.6	1.0 1.0	4.9 4.9	1.5 1.5	9.8 9.8	ns
t _{PZH} t _{PZL}	Output Enable Time to High and Low Level	2	0.8 0.8	3.9 3.9	1.0 1.0	5.4 5.4	1.5 1.5	9.8 9.8	ns
t _{PHZ} t _{PLZ}	Output Disable Time From High and Low Level	2	0.8 0.8	4.0 4.0	1.0 1.0	4.4 4.4	1.5 1.5	7.9 7.9	ns
t _s	Setup Time, High or Low Dn to LE	3	1.5		1.5		2.5		ns
t _h	Hold Time, High or Low Dn to LE	3	1.0		1.0		1.0		ns
t _w	LE Pulse Width, High	3	1.5		1.5		4.0		ns
t _{OSHL} t _{OSLH}	Output-to-Output Skew (Note 5.)			0.5 0.5		0.5 0.5		0.75 0.75	ns

4. For $C_L = 50\text{pF}$, add approximately 300ps to the AC maximum specification.

5. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	$T_A = +25^\circ\text{C}$	Unit
			Typ	
V_{OLP}	Dynamic LOW Peak Voltage (Note 6.)	$V_{CC} = 1.8\text{V}, C_L = 30\text{pF}, V_{IH} = V_{CC}, V_{IL} = 0\text{V}$	0.15	V
		$V_{CC} = 2.5\text{V}, C_L = 30\text{pF}, V_{IH} = V_{CC}, V_{IL} = 0\text{V}$	0.25	
		$V_{CC} = 3.3\text{V}, C_L = 30\text{pF}, V_{IH} = V_{CC}, V_{IL} = 0\text{V}$	0.35	
V_{OLV}	Dynamic LOW Valley Voltage (Note 6.)	$V_{CC} = 1.8\text{V}, C_L = 30\text{pF}, V_{IH} = V_{CC}, V_{IL} = 0\text{V}$	-0.15	V
		$V_{CC} = 2.5\text{V}, C_L = 30\text{pF}, V_{IH} = V_{CC}, V_{IL} = 0\text{V}$	-0.25	
		$V_{CC} = 3.3\text{V}, C_L = 30\text{pF}, V_{IH} = V_{CC}, V_{IL} = 0\text{V}$	-0.35	
V_{OHV}	Dynamic HIGH Valley Voltage (Note 7.)	$V_{CC} = 1.8\text{V}, C_L = 30\text{pF}, V_{IH} = V_{CC}, V_{IL} = 0\text{V}$	1.55	V
		$V_{CC} = 2.5\text{V}, C_L = 30\text{pF}, V_{IH} = V_{CC}, V_{IL} = 0\text{V}$	2.05	
		$V_{CC} = 3.3\text{V}, C_L = 30\text{pF}, V_{IH} = V_{CC}, V_{IL} = 0\text{V}$	2.65	

6. Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

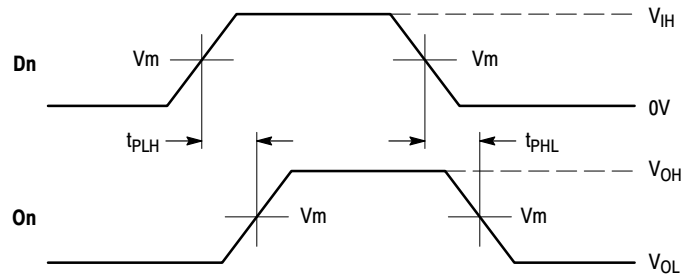
7. Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the HIGH state.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{IN}	Input Capacitance	Note 8.	6	pF
C_{OUT}	Output Capacitance	Note 8.	7	pF
C_{PD}	Power Dissipation Capacitance	Note 8., 10MHz	20	pF

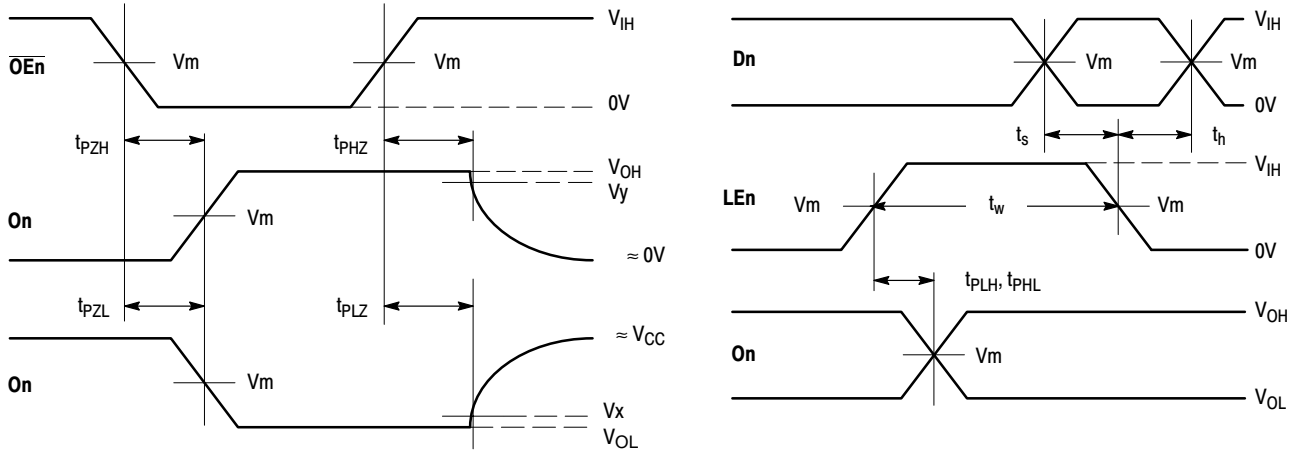
8. $V_{CC} = 1.8, 2.5$ or 3.3V ; $V_I = 0\text{V}$ or V_{CC} .

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WAVEFORM 1 - PROPAGATION DELAYS
 $t_R = t_F = 2.0\text{ns}$, 10% to 90%; $f = 1\text{MHz}$; $t_W = 500\text{ns}$

Figure 3. AC Waveforms

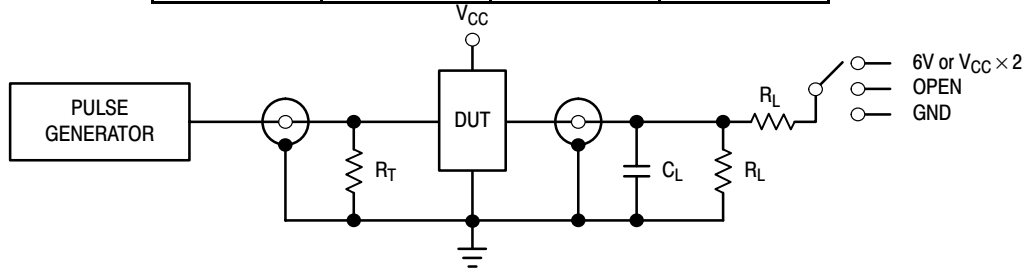


WAVEFORM 2 - OUTPUT ENABLE AND DISABLE TIMES
 $t_R = t_F = 2.0\text{ns}$, 10% to 90%; $f = 1\text{MHz}$; $t_W = 500\text{ns}$

WAVEFORM 3 - LE to On PROPAGATION DELAYS, LE MINIMUM PULSE WIDTH, Dn to LE SETUP AND HOLD TIMES
 $t_R = t_F = 2.0\text{ns}$, 10% to 90%; $f = 1\text{MHz}$; $t_W = 500\text{ns}$ except when noted

Figure 4. AC Waveforms

Symbol	V_{CC}		
	$3.3\text{V} \pm 0.3\text{V}$	$2.5\text{V} \pm 0.2\text{V}$	$1.8\text{V} \pm 0.15\text{V}$
V_{IH}	2.7V	V_{CC}	V_{CC}
V_m	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_x	$V_{OL} + 0.3\text{V}$	$V_{OL} + 0.15\text{V}$	$V_{OL} + 0.15\text{V}$
V_y	$V_{OH} - 0.3\text{V}$	$V_{OH} - 0.15\text{V}$	$V_{OH} - 0.15\text{V}$

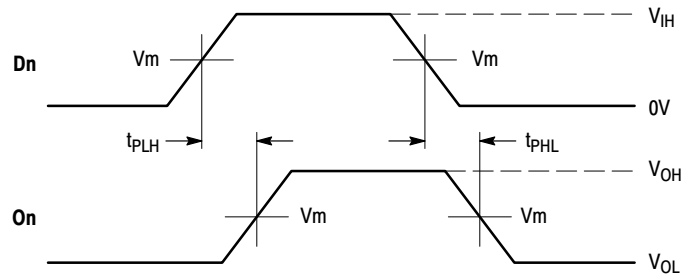


TEST	SWITCH
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PLZ}	6V at $V_{CC} = 3.3 \pm 0.3\text{V}$; $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2\text{V}$; $1.8\text{V} \pm 0.15\text{V}$
t_{PZH} , t_{PHZ}	GND

$C_L = 30\text{pF}$ or equivalent (Includes jig and probe capacitance)
 $R_L = 500\Omega$ or equivalent
 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

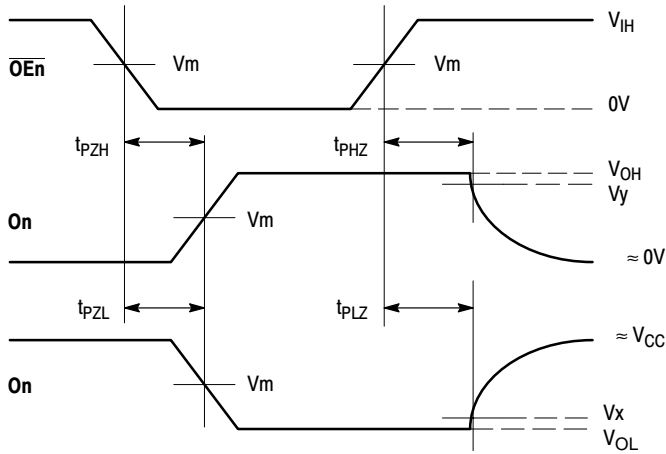
Figure 5. Test Circuit

74VCX162373

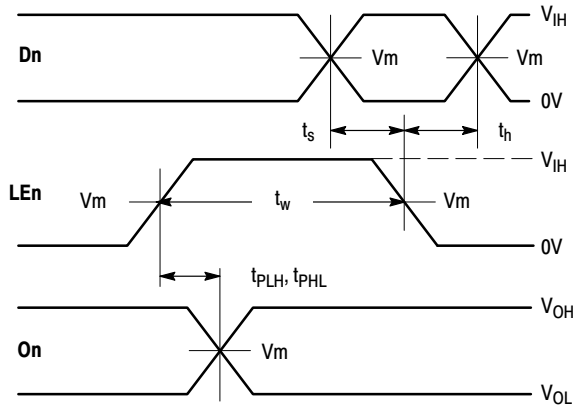


WAVEFORM 4 - PROPAGATION DELAYS
 $t_R = t_F = 2.0\text{ns}$, 10% to 90%; $f = 1\text{MHz}$; $t_W = 500\text{ns}$

Figure 6. AC Waveforms



WAVEFORM 5 - OUTPUT ENABLE AND DISABLE TIMES
 $t_R = t_F = 2.0\text{ns}$, 10% to 90%; $f = 1\text{MHz}$; $t_W = 500\text{ns}$



WAVEFORM 6 - LE to On PROPAGATION DELAYS, LE MINIMUM PULSE WIDTH, Dn to LE SETUP AND HOLD TIMES
 $t_R = t_F = 2.0\text{ns}$, 10% to 90%; $f = 1\text{MHz}$; $t_W = 500\text{ns}$ except when noted

Figure 7. AC Waveforms

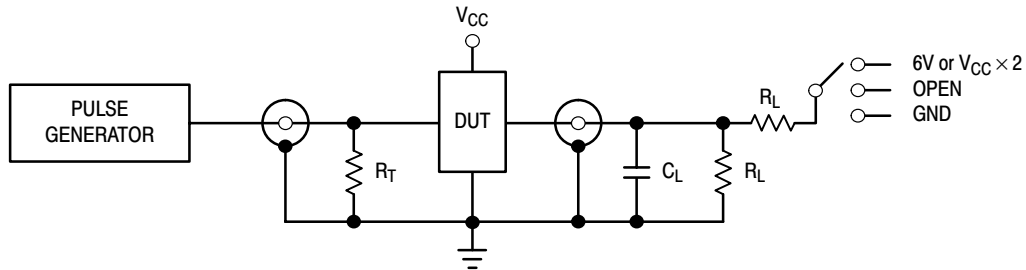
Symbol	V_{CC}	
	$3.3\text{V} \pm 0.3\text{V}$	2.7V
V_{IH}	2.7V	2.7V
V_m	1.5V	1.5V
V_x	$V_{OL} + 0.3\text{V}$	$V_{OL} + 0.3\text{V}$
V_y	$V_{OH} - 0.3\text{V}$	$V_{OH} - 0.3\text{V}$

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AC CHARACTERISTICS ($t_R = t_F = 2.0\text{ns}$; $C_L = 50\text{pF}$; $R_L = 500\Omega$)

Symbol	Parameter	Waveform	Limits				Unit
			T _A = −40°C to +85°C				
			V _{CC} = 3.0V to 3.6V		V _{CC} = 2.7V		
			Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay Dn to On	4	1.0 1.0	4.0 4.0		4.5 4.5	ns
t _{PLH} t _{PHL}	Propagation Delay LE to On	4	1.0 1.0	4.0 4.0		5.0 5.0	ns
t _{PZH} t _{PZL}	Output Enable Time to High and Low Level	5	1.0 1.0	5.0 5.0		6.0 6.0	ns
t _{PHZ} t _{PLZ}	Output Disable Time From High and Low Level	5	1.0 1.0	4.5 4.5		5.5 5.5	ns
t _{OSHL} t _{OSLH}	Output-to-Output Skew (Note 9.)			0.5 0.5		0.5 0.5	ns

9. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.



TEST	SWITCH
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PLZ}	6V at $V_{CC} = 3.3 \pm 0.3\text{V}$; $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2\text{V}$; $1.8\text{V} \pm 0.15\text{V}$
t_{PZH} , t_{PHZ}	GND

$C_L = 50\text{pF}$ or equivalent (Includes jig and probe capacitance)
 $R_L = 500\Omega$ or equivalent
 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 8. Test Circuit

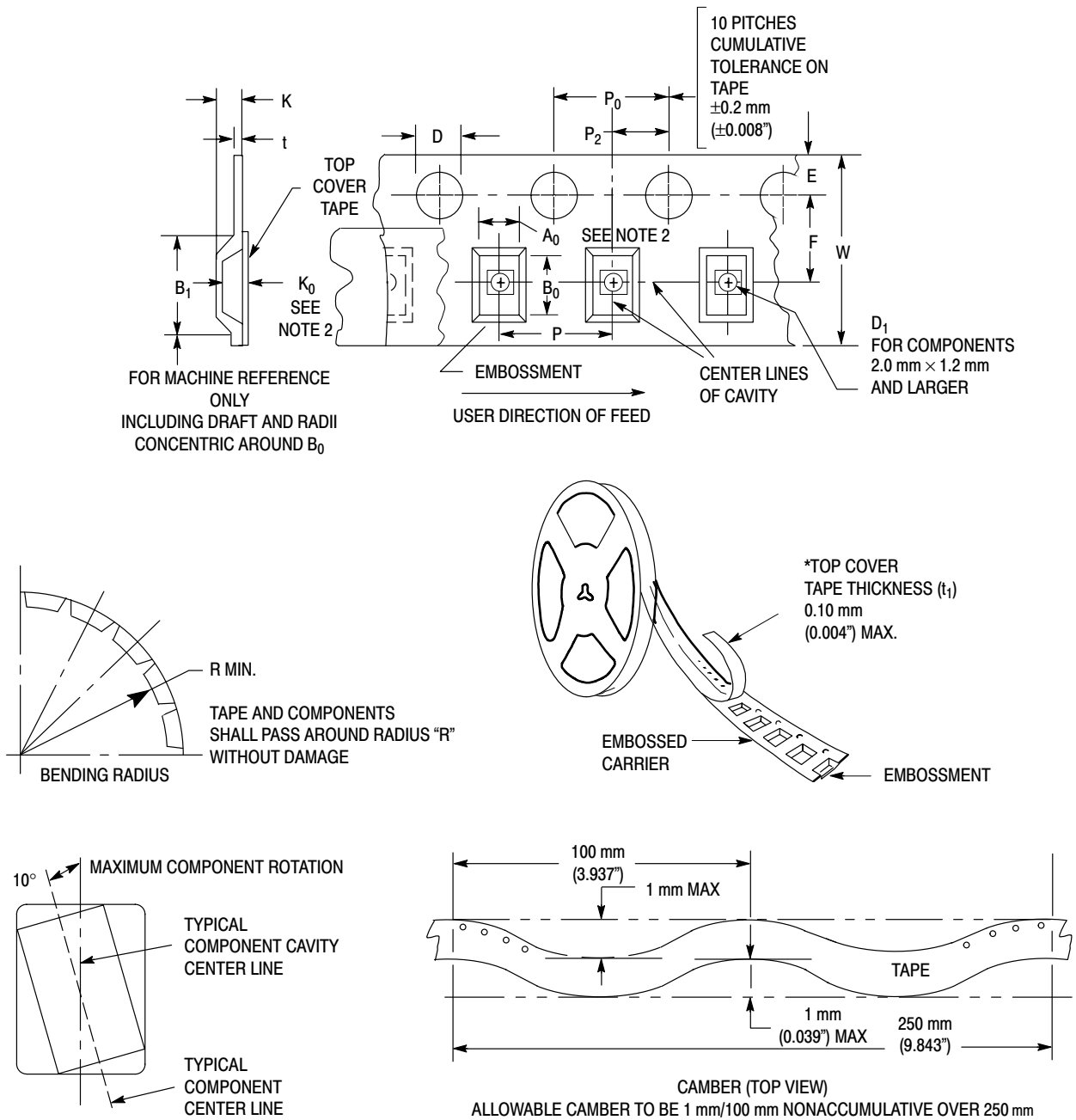


Figure 9. Carrier Tape Specifications

EMBOSSED CARRIER DIMENSIONS (See Notes 1 and 2)

Tape Size	B_1 Max	D	D_1	E	F	K	P	P_0	P_2	R	T	W
24mm	20.1mm (0.791")	1.5 + 0.1mm - 0.0 (0.059 + 0.004" - 0.0)	1.5mm Min (0.060")	1.75 ± 0.1 mm (0.069 ± 0.004 ")	11.5 ± 0.10 mm (0.453 ± 0.004 ")	11.9 mm Max (0.468")	16.0 ± 0.1 mm (0.63 ± 0.004 ")	4.0 ± 0.1 mm (0.157 ± 0.004 ")	2.0 ± 0.1 mm (0.079 ± 0.004 ")	30 mm (1.18")	0.6 mm (0.024")	24.3 mm (0.957")

1. Metric Dimensions Govern—English are in parentheses for reference only.

2. A_0 , B_0 , and K_0 are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min to 0.50 mm max. The component cannot rotate more than 10° within the determined cavity

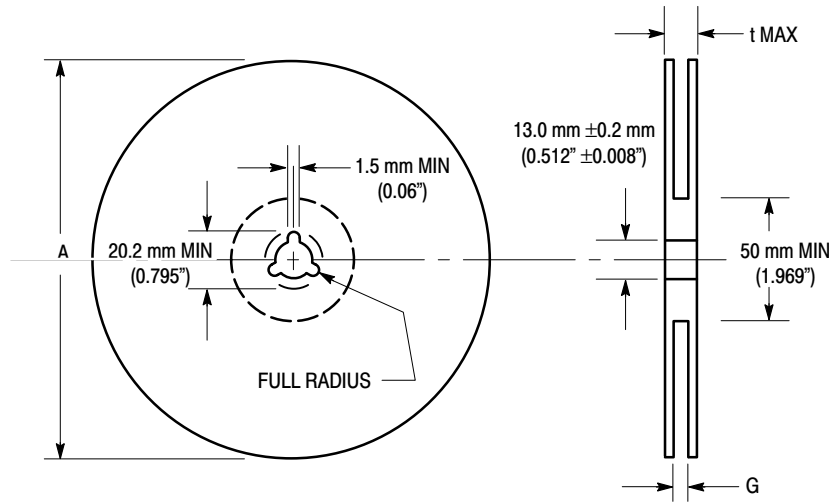


Figure 10. Reel Dimensions

REEL DIMENSIONS

Tape Size	A Max	G	t Max
24 mm	360 mm (14.173")	24.4 mm + 2.0 mm, -0.0 (0.961" + 0.078", -0.00)	30.4 mm (1.197")

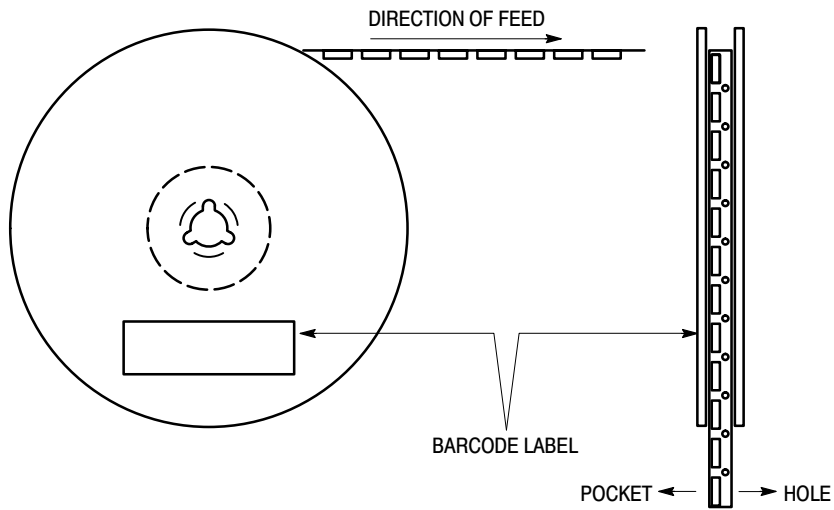


Figure 11. Reel Winding Direction

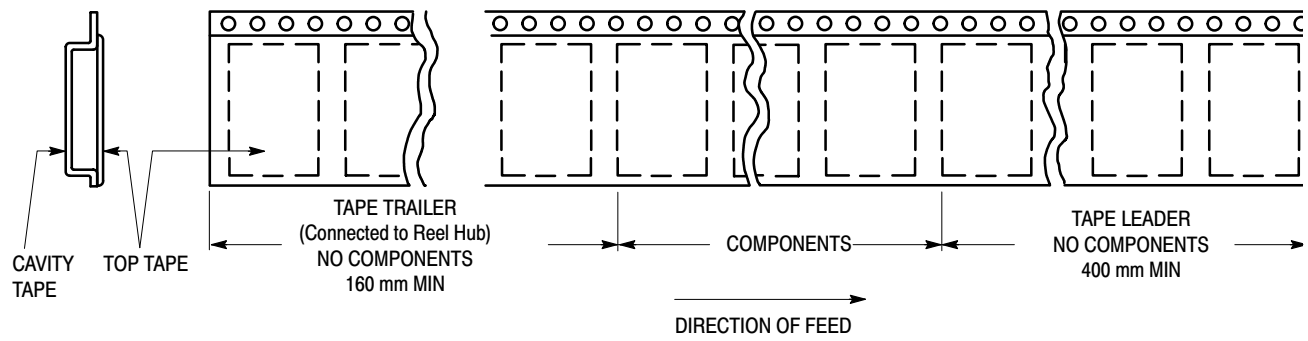


Figure 12. Tape Ends for Finished Goods

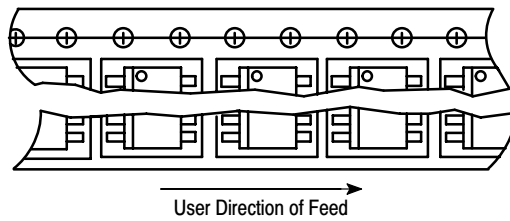
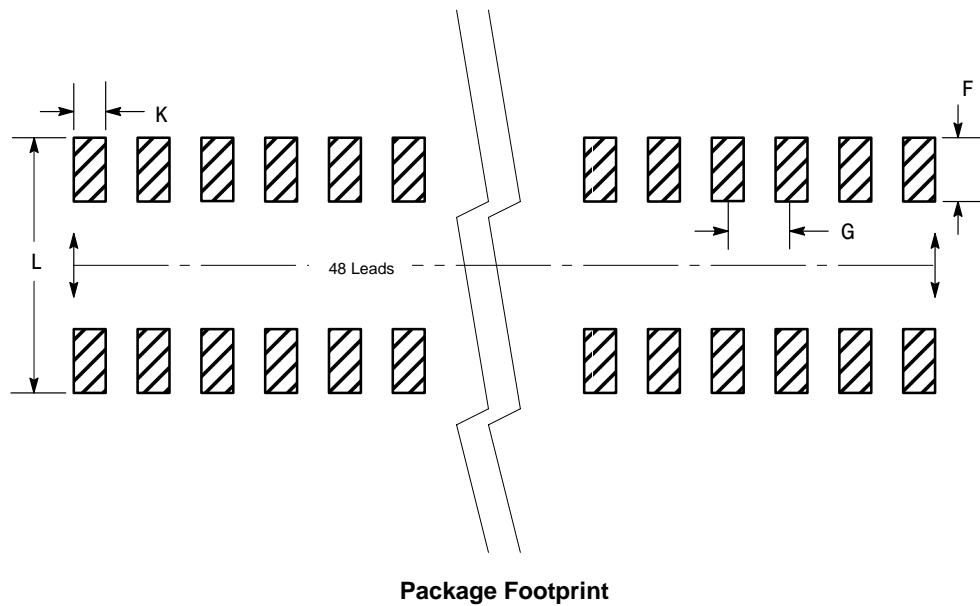


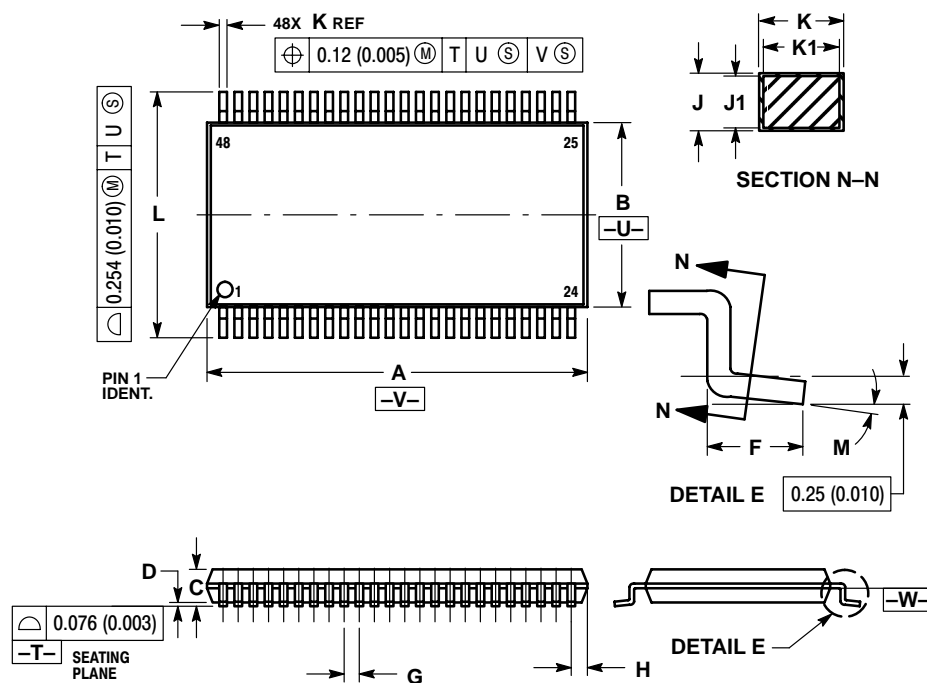
Figure 13. Reel Configuration



Package Footprint

PACKAGE DIMENSIONS

TSSOP
DT SUFFIX
CASE 1201-01
ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.40	12.60	0.488	0.496
B	6.00	6.20	0.236	0.244
C	---	1.10	---	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.50 BSC	0.0197 BSC		
H	0.37	---	0.015	---
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.17	0.27	0.007	0.011
K1	0.17	0.23	0.007	0.009
L	7.95	8.25	0.313	0.325
M	0°	8°	0°	8°

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