AUTOMOTIVE GRADE

CS1124

Dual Variable-Reluctance Sensor Interface IC

Description

The CS1124 is a monolithic integrated circuit designed primarily to condition signals used to monitor rotating parts.

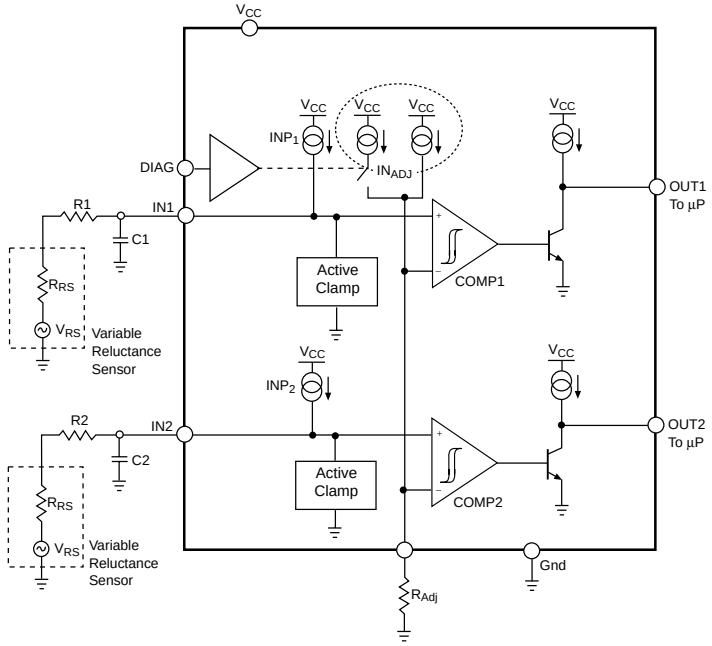
The CS1124 is a dual channel device. Each channel interfaces to a Variable Reluctance Sensor, and monitors the signal produced when a metal object is moved past that sensor. An output is generated that is a comparison of the input voltage and the voltage produced at the IN_{Adj} lead. The resulting square-wave is available at the OUT pin.

When the DIAG pin is high, the reference voltage at IN_{Adj} is increased. This then requires a larger signal at the input to trip the comparator, and provides for a procedure to test for an open sensor.

Absolute Maximum Ratings

Storage Temperature Range ..... –65°C to 150°C
Ambient Operating Temperature ..... –40°C to 125°C
Supply Voltage Range (continuous) ..... –0.3V to 7V
Input Voltage Range (at any input, $R_1 = R_2$ 22k) ..... –250V to 250V
Maximum Junction Temperature ..... 150°C
ESD Capability (Human Body Model) ..... 2 kV
Lead Temperature Soldering
Reflow (SMD styles only) ..... 60 sec. max above 183°C, 230°C peak

Block Diagram

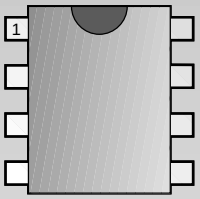


Features

- **Dual Channel Capability**
- **Built-In Test Mode**
- **On-Chip Input Voltage Clamping**
- **Works From 5V Supply**
- **Accurate Built-In Hysteresis**

Package Option

8 Lead SOIC



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Electrical Characteristics: 4.5V < V_{CC} < 5.5V; –40°C < T_A < 125°C; V_{DIAG} = 0; unless otherwise specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ **V_{CC} Supply**					
Operating Current Supply	V_{CC} = 5V			5	mA
■ **Sensor Inputs**					
Input Threshold – Positive	V_{DIAG} = low	135	160	185	mV
	V_{DIAG} = high	135	160	185	mV
Input Threshold – Negative	V_{DIAG} = low	–185	–160	–135	mV
	V_{DIAG} = high	135	160	185	mV
Input Bias Current (INP1, INP2)	V_{IN} = 0.336V	–16	–11	–6	µA
Input Bias Current (DIAG)	V_{DIAG} = 0V			1	µA
Input Bias Current Factor (K_I)	V_{IN} = 0.336V, V_{DIAG} = low		100		% INP
($IN_{ADJ} = INP \times K_I$)	V_{IN} = 0.336V, V_{DIAG} = high	152	155	157	% INP
Bias Current Matching	INP1 or INP2 to IN_{Adj}, V_{IN} = 0.336V	–1	0	1	µA
Input Clamp – Negative	I_{IN} = –50µA	–0.5	–0.25	0	V
	I_{IN} = –12mA	–0.5	–0.30	0	V
Input Clamp – Positive	I_{IN} = +12mA	5	7	9	V
Output Low Voltage	I_{OUT} = 1.6mA		0.2	0.4	V
Output High Voltage	I_{OUT} = –1.6mA	V_{CC} – 0.5	V_{CC} – 0.2		V
Mode Change Time Delay		0		20	µs
Input to Output Delay	I_{OUT} = 1.0mA		1	20	µs
Output Rise Time	C_{LOAD} = 30pF		0.5	2	µs
Output Fall Time	C_{LOAD} = 30pF		0.05	2	µs
Open-Sensor Positive Threshold	V_{DIAG} = high, $R_{IN(Adj)}$ = 40k (Note 1)	29.4	54k	86.9	Ω
■ **Logic Inputs**					
DIAG Input Low Threshold				$0.2 \times V_{CC}$	V
DIAG Input High Threshold		$0.7 \times V_{CC}$			V
DIAG Input Resistance	$V_{IN} = 0.3 \times V_{CC}$, V_{CC} = 5.0V	8k	22k	70k	Ω
	$V_{IN} = V_{CC}$, V_{CC} = 5.0V	8k	22k	70k	Ω

Note 1: This parameter is guaranteed by design, but not parametrically tested in production.

Package Pin Description

PACKAGE PIN#	PIN SYMBOL	FUNCTION
8 Lead So Narrow		
1	IN_{Adj}	External resistor to ground that sets the trip levels of both channels. Functions for both diagnostic and normal mode.
2	IN1	Input to channel 1.
3	IN2	Input to channel 2.
4	Gnd	Ground.
5	DIAG	Diagnostic mode switch. Normal mode is low.
6	OUT2	Output of channel 2.
7	OUT1	Output of channel 1.
8	V_{CC}	Positive 5 volt supply input.

Theory of Operation

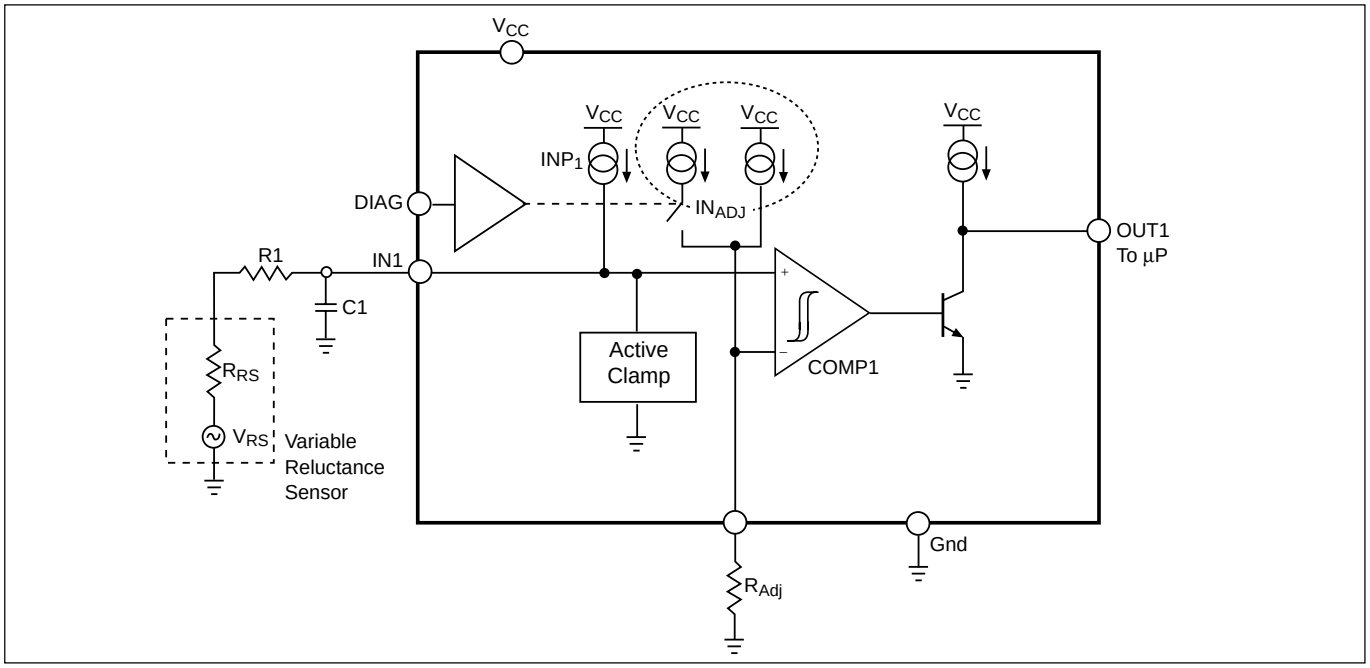


Figure 1: CS1124 Applications Diagram.

Normal Operation

Figure 1 shows one channel of the CS1124 along with the necessary external components. Both channels share the IN_{Adj} pin as the negative input to a comparator. A brief description of the components is as follows:

V_{RS}	Ideal sinusoidal, ground referenced, sensor output - amplitude usually increases with frequency, depending on loading.
R_{RS}	Source impedance of sensor.
R1/R_{Adj}	External resistors for current limiting and biasing.
INP1/IN_{Adj}	Internal current sources that determine trip points via $R1 / R_{Adj}$.
COMP1	Internal comparator with built-in hysteresis set at 160mV.
OUT1	Output 0V - 5V square wave with the same frequency as V_{RS}.

By inspection, the voltage at the (+) and (–) terminals of COMP1 with V_{RS} = 0V are:

$$V^+ = INP1\ (R1 + R_{RS}) \quad (1)$$

$$V^- = IN_{Adj} \times R_{Adj} \quad (2)$$

As V_{RS} begins to rise and fall, it will be superimposed on the DC biased voltage at V^+.

$$V^+ = INP1(R1 + R_{RS}) + V_{RS} \quad (3)$$

to get comparator COMP1 to trip, the following condition is needed:

when crossing in the positive direction,

$$V^+ > V^- + V_{HYS} \quad (4)$$

(V_{HYS} is the built-in hysteresis set to 160mV)

or, when crossing in the negative direction,

$$V^+ < V^- - V_{HYS} \quad (5)$$

Combining equations 2, 3, and 4, we get:

$$INP1(R1 + R_{RS}) + V_{RS} > IN_{Adj} \times R_{Adj} + V_{HYS} \quad (6)$$

therefore,

$$V_{RS\ (+TRP)} > IN_{Adj} \times R_{Adj} - INP1(R1 + R_{RS}) + V_{HYS} \quad (7)$$

It should be evident that tripping on the negative side is:

$$V_{RS\ (-TRP)} < IN_{Adj} \times R_{Adj} - INP1(R1 + R_{RS}) - V_{HYS} \quad (8)$$

in normal mode,

$$INP1 = IN_{Adj} \quad (9)$$

we can now re-write equation (7) as:

$$V_{RS(+TRP)} > INP1(R_{Adj} - R1 - R_{RS}) + V_{HYS} \quad (10)$$

by making

$$R_{Adj} = R1 + R_{RS} \quad (11)$$

you can detect signals with as little amplitude as V_{HYS}. A design example is given in the applications section.

Open Sensor Protection

The CS1124 has a diag pin that when pulled high (5V), will increase the IN_{Adj} current source by roughly 50%.

Equation (7) shows that a larger $V_{RS(+TRP)}$ voltage will be needed to trip comparator COMP1. However, if no V_{RS} signal is present, then we can use equations 1, 2, and 4 (equation 5 does not apply in this mode) to get:

$$INP1(R1 + R_{RS}) > INP1 \times K_I \times R_{Adj} + V_{HYS} \quad (12)$$

Theory of Operation: continued

since R_{RS} is the only unknown variable we can solve for R_{RS},

$$R_{RS} = \frac{INP1 \times K_I \times R_{Adj} + V_{HYS}}{INP1} - R1 \quad (13)$$

Equation (13) shows that if the output switches states when entering the diag mode with $V_{RS} = 0$, the sensor impedance must be greater than the above calculated value. This can be very useful in diagnosing intermittent sensor.

Input Protection

As shown in Figure 1, an active clamp is provided on each input to limit the voltage on the input pin and prevent substrate current injection. The clamp is specified to handle ±12mA. This puts an upper limit on the amplitude of the sensor output. For example,

if R1 = 20k,

then $V_{RS(MAX)} = 20k \times 12mA = 240V$.

Therefore, the $V_{RS(pk-pk)}$ voltage can be as high as 480V.

The CS1124 will *typically* run at a frequency up to 1.8MHz if the input signal does not activate the positive or negative input clamps. Frequency performance will be lower when the positive or negative clamps are active. *Typical* performance will be up to a frequency of 680kHz with the clamps active.

Circuit Description

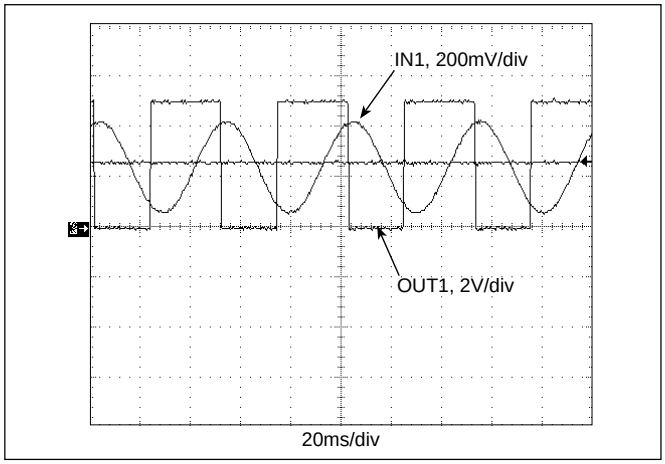


Figure 2: Minimum Threshold Operation.

Figure 2 shows the part operating near the minimum input thresholds. As the sin wave input threshold is increased, the low side clamps become active (Figure 3). Increasing the amplitude further (Figure 4), the high-side clamp becomes active. These internal clamps allow for voltages up to –250V and 250V on the sensor side of the setup (with R1 = R2 = 22k) (reference the diagram on the front page).

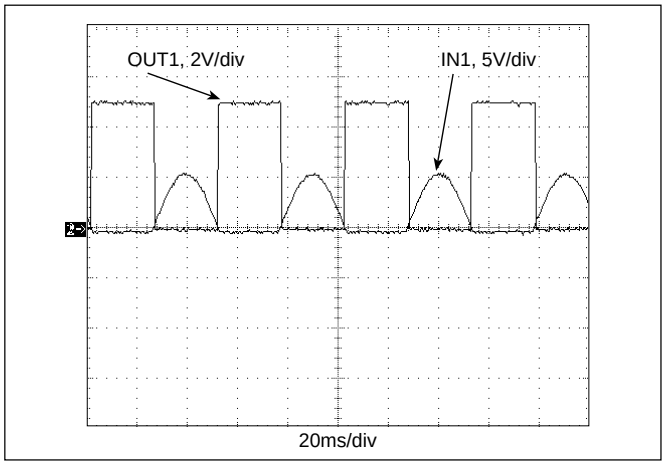


Figure 3: Low-Side Clamp.

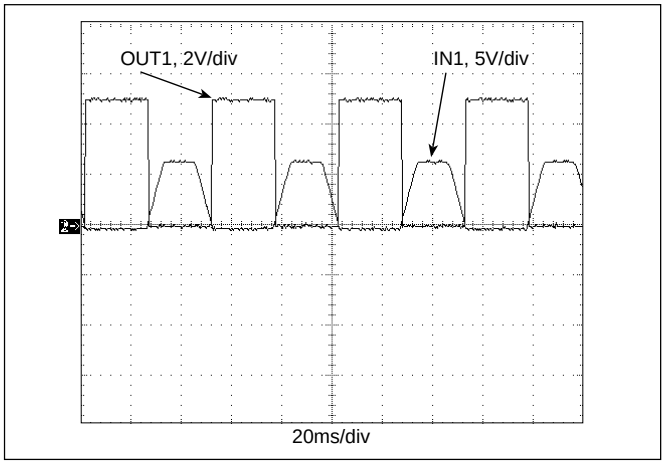


Figure 4: Low- and High-Side Clamps.

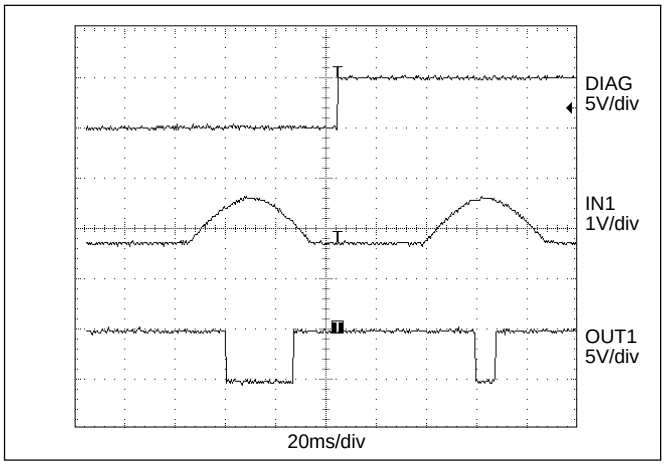


Figure 5: Diagnostic Operation.

Figure 5 shows the effect using the diagnostic (DIAG) function has on the circuit. The input threshold (negative) is switched from a threshold of –160mV to +160mV when DIAG goes from a low to a high. There is no hysteresis when DIAG is high.

Referring to Figure 1, the following will be a design example given these system requirements:

R_{RS} = 1.5kΩ (>12kΩ is considered open)

$V_{RS(MAX)} = 120V_{pk}$

$V_{RS(MIN)} = 250mV_{pk}$

F_{VRs} = 10kHz @ $V_{RS(MIN)} = 40V_{pk-pk}$

1. Determine tradeoff between R1 value and power rating. (use 1/2 watt package)

$$P_D = \frac{\left(\frac{120}{\sqrt{2}}\right)^2}{R1} < 1/2W$$

Set R1 = 15k

(the clamp current will then be 120/15k = 8mA, which is less than the 12mA limit)

2. Determine R_{Adj}

Set R_{Adj} as close to R1 + R_{RS} as possible.
Therefore, R_{Adj} = 17k

3. Determine $V_{RS(+TRP)}$ using equation (7).

$$V_{RS(+TRP)} = 11\mu A \times 17k - 11\mu A(15k + 1.5k) + 160mV$$

$V_{RS(+TRP)}$ = 166mV typical (easily meets 250mV minimum)

4. Calculate worst case $V_{RS(+TRP)}$

Examination of equation (7) and the spec reveals the worst case trip voltage will occur when:

V_{HYS} = 180mV R1 = 14.25k (5% low)
IN_{Adj} = 16µA R_{Adj} = 17.85k (5% High)
INP1 = 15µA

$V_{RS(+TRP)MAX}$ = 16µA(17.85k) – 15µA(14.25k + 1.5k) + 180mV
= 229mV,

which is still less than the 250mV minimum amplitude of the input.

5. Calculate C1 for low pass filtering

Since the sensor guarantees $40V_{pk-pk}$ @ 10kHz, a low pass filter using R1 and C1 can be used to eliminate high frequency noise without affecting system performance.

$$\text{Gain Reduction} = \frac{0.29V}{20V} = 0.0145 = -36.7dB$$

Therefore, a cut-off frequency, f_c, of 145Hz could be used.

$$C1 \le \frac{1}{2\pi f_c R1} \le 0.07\mu F$$

Set C1 = 0.047µF

6. Calculate the minimum R_{RS} that will be indicated as an open circuit. (DIAG = 5V)

Rearranging equation (7) gives

$$R_{RS} = \frac{V_{HYS} + INP1 \times K_I \times R_{Adj} - V_{RS(+TRP)}}{INP1} - R1$$

But, V_{RS} = 0 during this test, so it drops out.

Using the following as worst case Low and High:

	Worst Case Low (R_{RS})	Worst Case High (R_{RS})
IN_{Adj}	23.6µA = 15µA × 1.57	10.7µA = 7µA × 1.53
R_{Adj}	16.15k	17.85k
V_{HYS}	135mV	185mV
INP1	16µA	6µA
R1	15.75k	14.25k
K_I	1.57	1.53

$$R_{RS} = \frac{135mV + 23.6\mu A \times 16.15k}{16\mu A} - 15.75k = 16.5k$$

Therefore,

$R_{RS(MIN)}$ = 16.5k (meets 12k system spec)

and,

$$R_{RS(MAX)} = \frac{185mV + 10.7\mu A \times (17.85k)}{6\mu A} - 14.25k = 48.4k$$

Package Specification

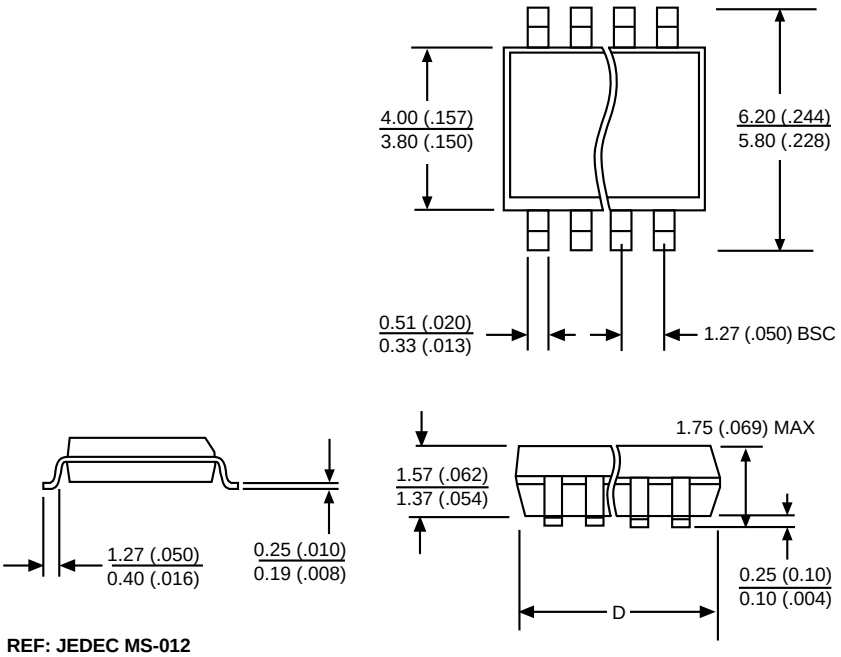
PACKAGE DIMENSIONS IN mm (INCHES)

Lead Count	D			
	Metric		English	
	Max	Min	Max	Min
8 Lead SO Narrow	5.00	4.80	.197	.189

PACKAGE THERMAL DATA

Thermal Data		8 Lead SO Narrow	
$R_{\Theta JC}$	typ	45	°C/W
$R_{\Theta JA}$	typ	165	°C/W

Surface Mount Narrow Body (D); 150 mil wide



REF: JEDEC MS-012

Ordering Information

Part Number	Description
CS1124YD8	8 Lead SO Narrow
CS1124YDR8	8 Lead SO Narrow *(tape & reel)*

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